AN INHERENTLY LINEAR CMOS MULTIPLIER

Ying Dong, Sumit Bagga, Wouter A. Serdijn

Electronics Research Laboratory, Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS)
Delft University of Technology, Delft, the Netherlands
Email: {Y.Dong-ET; s.bagga; w.a.serdijn}@ewi.tudelft.nl

ABSTRACT

This paper presents a linear multiplier that can be fully implemented in CMOS technology. The circuit implements the function of mathematical multiplication for the two input signals. Since this multiplier is not a conventional mixer, some unconventional methods were use, such as, to realize the function of multiplication, a translinear loop is implemented, which is based on the exponential relation of a PN-diode in CMOS technology, while the other CMOS transistors working in strong inversion only provide gain. The targeted IC process was IBM's 0.18 μm BiCMOS SiGe. The multiplier works up to 10 GHz and can be used for high frequency applications such as ultra-wideband autocorrelation receivers.

Keywords*:* translinear loop, exponential relation, linearity, high frequency, linear multiplier, UWB, CMOS.

1. INTRODUCTION

In an autocorrelation receiver [1], the pulses are received in series. After removing the interference and amplification, the signal is distributed into two paths. To achieve the maximal correlation and to avoid the error caused by pulse distortion, the received waveform is multiplied with the previously received waveform. Since they have been transferred via the same path, they are supposed to be distorted in the same way. Hence the correlation still holds. As can be seen from Figure 1, the receiver setup realizes the function of:

$$y(t) = \int_{t1}^{t2} g(t)g(t-\tau_d)dt = \pm\int_{t1}^{t2} g^2(t)dt$$

where g(t) is the received pulse, y(t) is the output signal of the autocorrelation receiver, τd is the delay time and t1, t2 are the integration start and stop time, respectively. From the expression given above, it is clear that there are three functional blocks in the receiver. These are the multiplier, the time delay and the integrator.

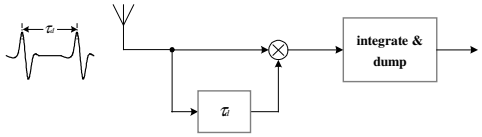

Figure 1 Autocorrelation receiver architecture

For ir-UWB applications, all the functional blocks in Figure 1 are required to operate at gigahertz frequencies. This high frequency and large bandwidth prerequisites make the implementation of the multiplier extremely challenging.

The multiplier employed here is different from a switching mixer that is normally used in high frequency systems. Instead, the linear multiplier is realizing the function of mathematical multiplication of the two input signals. If the input signals are x and y, then the output signal should be z=x*y. In order to work properly in an autocorrelation receiver designed for the (3.1-10.6) GHz bandwidth, the multiplier at least needs to work properly up to 10.6 GHz.

The function of linear multiplication is normally realized by a translinear loop [2]. Traditionally, in a translinear loop, only active exponential devices are used, e.g. bipolar transistors, MOS transistors in weak inversion [3] or lateral bipolar transistors that can be found in any standard CMOS technology [4]. For high frequency applications, the performances of MOS transistors in weak inversion and lateral bipolar transistors in CMOS are clearly not good enough. Although circuits based on bipolar translinear loops can fulfill these frequency requirements, they are not compatible with CMOS IC technology.

A new topology to implement a linear multiplier in standard CMOS IC technology is proposed here. It is based on the exponential I-V relation of a PN-diode, whereas CMOS transistors are used to provide gain [4]. In this way a CMOS multiplier with high linearity and high frequency response is realized. Also, the use is not limited

to a linear multiplier. With the concept of emulating a bipolar cell in CMOS technology, any translinear loop can be implemented in CMOS technology.

2. EMULATED BIPOLAR TRANSISTOR IN CMOS

Any bipolar translinear circuit is based on two fundamental characteristics of a bipolar transistor. One is the exponential relation between voltage and current of a base-emitter junction while the other is its transconductance gain. Since the exponential relation is characteristic for any PN-junction, it also holds for a PN-diode that is available in CMOS technology. As far as the gain is concerned, CMOS and bipolar transistors are more or less similar. Their transfer can be considered to be a non-linear transconductance.

The idea of an emulated bipolar cell is depicted in Figure 2. The nullor in the graph is an abstract concept of any ideal amplifier. It is an amplifier whose chain-matrix contains only zeros [6]. Hence, all its transfer parameters are infinite. For finite output signals, the input voltage and current of a nullor thus equal zero. The PN-diode in the feedback loop senses the current at the output and accordingly generates a voltage drop across the input terminals. This current and voltage-drop follow the exponential relation of a diode. From Figure 1, it holds:

$$U_{in} = U_d \; ; \; I_d = I_s \exp(U_d / U_T) \; .$$

Based on these, it is easy to derive that:

$$I_{out} = I_s \exp(U_{in} / U_T) \qquad (1)$$

Equation (1) shows that the exponential I-V relation of a bipolar transistor also holds for the input voltage and output current of this emulated bipolar cell. This proves the concept of an emulated bipolar cell theoretically.

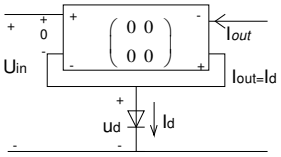

Figure 2 Emulated bipolar cell principle

The simplest way to implement the nullor is to use a single gain stage (see Figure 3a). We can implement a single gain stage with either a common-source stage or a differential pair.

In Figure 3b, curve A is the result for a bipolar transistor; curve B is for a differential input pair and curve C is for a CS stage. It can be seen that curve B follows curve A quite well while there is a big difference between curve C and curve A. This happens because when the gate-source voltage of a single CS stage is not high enough, the transistor enters the weak inversion region. In weak inversion, the transistor itself also has an exponential voltage-current relation, which explains why the slope of curve C is almost half the slope of curve A. At the same time, the input voltage of the differential pair is supposed to be small as the two transistors work symmetrically.

Still, for a differential input pair, the exponential range in Figure 3b is not large enough. Especially at higher V_{be}, the maximal current it can achieve is lower than 1 mA. Therefore, we have to try a two-stage nullor implementation, as more loop gain is required.

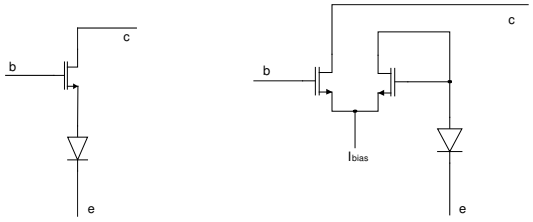

Figure 3a: A single stage nullor implementation (left) CS stage, (right) differential pair

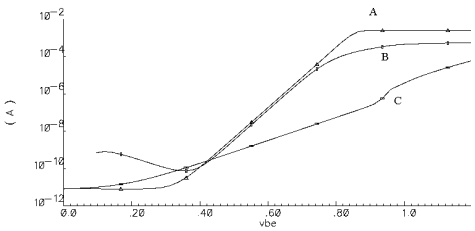

Figure 3b: V-I relationship for a bipolar transistor (curve A) and the emulated bipolar transistor with a differential pair (curve B) and a single CS stage (curve C)

The nullor in Figure 2 can be implemented with a two-stage amplifier comprising a differential pair and a common-source stage, as shown in Figure 4 (only its signal diagram is shown). The simulated Gummel plot of this emulated bipolar cell with its two-stage nullor implementation is shown in Figure 4 along with the simulated Gummel plots of a single bipolar transistor and the emulated bipolar cell with a nullor.

With the emulated bipolar cell, it is possible to implement any bipolar translinear circuit in CMOS technology.

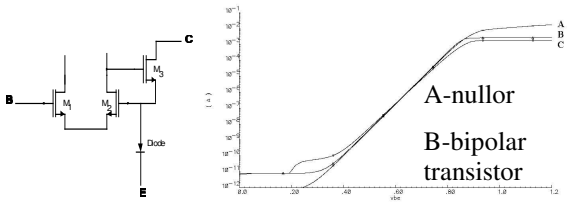

Figure 4: (left) Emulated bipolar cell implementation (only signal diagram is shown) and; (right) Simulated Gummel plot

3.CMOS LINEAR MULTIPLIER CIRCUIT

A very well known and widely used bipolar translinear circuit to realize the multiplication function is the "six-pack" four-quadrant multiplier. It is shown in Figure 5 [2]. It realizes the function $i_0=2i_1i_2/I_1$. As shown in the circuit, transistors *Q5* and *Q6* are diode connected and can be safely replaced by a single PN-diode, while the emulated bipolar cell depicted in Figure 1 can replace any of the transistors *Q1* through *Q4*. The resulting CMOS circuit is shown in Figure 5. This circuit also realizes the function $i_0=2i_1i_2/I_1$. With proper interfacing circuitry, this CMOS multiplier can be used in a voltage multiplier as well.

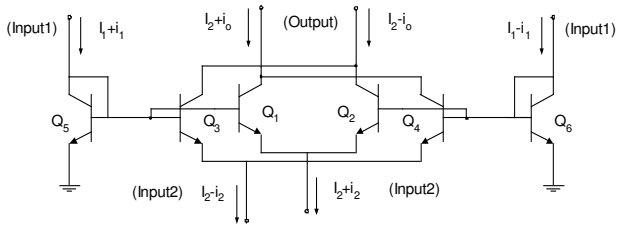

Figure 5: Bipolar "six-pack" four-quadrant multiplier

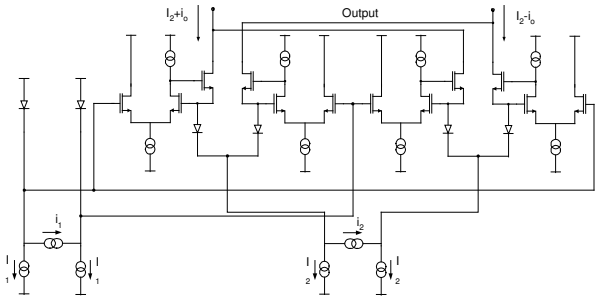

Figure 6: CMOS "six-pack" four-quadrant multiplier with emulated bipolar cells

4. SIMULATION RESULTS

The circuit in Figure 6 has been simulated using transistor and diode models of the 0.18 µm CMOS SiGe-Gate IBM IC process. Figure 7 shows the output of the bipolar circuit and the CMOS circuit when i_1 equals a 100 µA (pp) sine wave at 1 GHz and i_2 equals a 50µA (pp) sine wave at 10 GHz. Simulation results show that the CMOS linear multiplier works properly, albeit that its amplitude at the output is somewhat smaller than the output of the bipolar circuit. This is due to the offset at the input of the two-stage implementation of the nullor in the emulated bipolar cell. This results in a gain error. Adding more gain stages to the nullor, thereby enhancing the loop gain, or improving the symmetry of the nullor will improve the performance even further.

To check the high-frequency response, the frequencies of the two input signals were set to be 9 GHz and 10 GHz respectively. The frequency components of the output signal are shown in Figure 8. It shows that except the desired output signals (5.281 µA for 1 GHz and 5.086 µA for 19 GHz), all the other harmonics are comparatively small. This implies that the linearity of the CMOS multiply circuit is very good.

The CMOS linear multiplier shown in Figure 6 has been designed to operate from a supply voltage of 1.8V, with its biasing currents I_1 and I_2 set to be 500 µA and 100 µA, and 2 mA for each differential pair in the emulated bipolar cells. The current consumption for this CMOS linear multiplier is 9.2 mA while its power consumption is 16.56 mW. As the multiplier has two differential inputs and their signal paths are different, the total harmonic distortion (THD) has two different values. Both of the inputs are set to be a 100 µA (pp) sine wave, when i_1 is at 9.5 GHz and i_2 is at 10 GHz, the THD equals –36 dB; when i_1 is at 10 GHz and i_2 is at 9.5 GHz, the THD equals –61 dB.

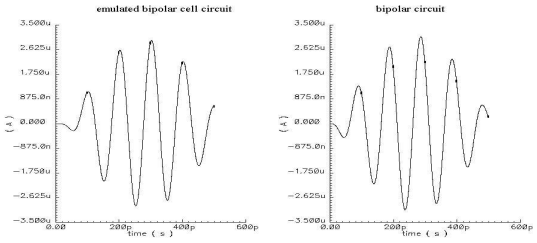

Figure 7: Simulation result for circuit with emulated bipolar cells and bipolar transistors

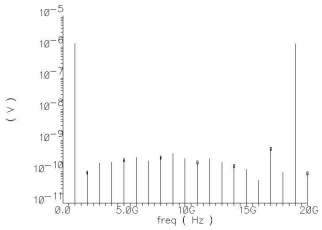

Figure 8: Fourier transform of the output signals

5. CONCLUSION

A linear multiplier suitable for implementation in standard CMOS technology is presented. The circuit uses an emulated bipolar cell, consisting of a PN-diode and CMOS transistors, to implement a "six-pack" four-quadrant multiplier as the core circuit. Simulation results show that the multiplier works up to at least 10 GHz. It can thus be used for high-frequency applications such as ultra-wideband autocorrelation receivers. Moreover this multiplier demonstrates that by proper arranging of emulated bipolar cells, it is possible to implement also other bipolar translinear circuits in CMOS technology.

ACKNOWLEDGEMENTS

This work is a part of the AIRLINK project of Delft University of Technology (www.airlink.tudelft.nl) and

partially sponsored by the Ministry of Economical Affairs under the Dutch Initiative “Freeband”.

6. REFERENCES

[1] R.T. Hoctor and H.W. Tomlinson, “Delay-Hopped Transmitted-Reference RF Communications,” *Proceedings of the IEEE Conference on Ultra Wideband Systems and Technologies*, pp. 265-270, May 2002

[2] B. Gilbert, “Translinear Circuits: A Proposed Classification,” Electronics Letters, Vol. 11., No.1, pp. 14-16, 1975.

[3] Eric A. Vittoz, “MOS Transistors Operated in the Lateral Bipolar Mode and Their Application in CMOS Technology,” IEEE Journal of Solid-State Circuits, Vol. Sc-a8, No.3, June 1983.

[4] Geoffrey D. Duerden, Gordon W. Roberts, and M. Jamal Deen, “The Development of Bipolar Log Domain Filters in a Standard CMOS Process,” in Proc. IEEE Int. Symp. Circuits and Systems, vol. 1, pp. 145-148, May 2001.

[5] Sandro A. P. Haddad, Wouter A. Serdijn, “High-Frequency Dynamic Translinear and Log-domain Circuits in CMOS Technology,” in Proc. IEEE Int. Symp. Circuit and Systems, vol. 3, pp. 313-316, May 2002.

[6] C.J.M. Verhoeven, A. van Staveren, G.L.E. Monna, M.H.L. Kouwenhoven and E. Yildiz “Structured Electronic Design-Negative-Feedback Amplifiers,” Kluwer Academic Publishers, 2003.