from (8a) and (8b). For any input common mode voltage (V_C), the bias currents for the n- and p-type differential pairs are given by

$$I_{bn}(V_C) = I_n(V_C) + \begin{cases} 3[I_n(V_C) - I_p(V_C)], & I_n(V_C) > I_p(V_C) \\ 0, & \text{otherwise} \end{cases} \tag{8a}$$

$$I_{bp}(V_C) = I_p(V_C) + \begin{cases} 3[I_p(V_C) - I_n(V_C)], & I_p(V_C) > I_n(V_C) \\ 0, & \text{otherwise} \end{cases} \tag{8b}$$

where $I_n(V_C)$ and $I_p(V_C)$ are the drain currents of the tail current sources formed by MBN and MBP, as a function of the input common mode voltage V_C, for the n- and p- type differential pairs, respectively. Assuming MBN and MBP supplies equal amounts of drain current (I_b), when they are in saturation region, the equations above become the following:

1) When only the n-type pair is on (i.e., V_C close to V_{DD})

$$I_{bn}(V_C) = 4I_n(V_C) = 4I_b, \quad I_{bp}(V_C) = 0 \tag{9a}$$

2) When only the p-type pair is on (i.e., V_C close to V_{SS})

$$I_{bn}(V_C) = 0, \quad I_{bp}(V_C) = 4I_p(V_C) = 4I_b \tag{9b}$$

3) When both pairs are on (i.e., V_C at mid supply range)

$$I_{bn}(V_C) = I_{bp}(V_C) = I_b \tag{9c}$$

Hence, total transconductance g_m has a value of $2\sqrt{2\beta I_b}$ for the cases above, if $\beta_n = \beta_p = \beta$.

In Fig. 5, transistors MNC1 and MNC2, and MPC1 and MPC2 detect the input common mode voltage and allow transistors M11 and M5 to replicate the bias currents $I_n(V_C)$ and $I_p(V_C)$, respectively. Transistors M1 through M4 and M7 through M10 implement the current subtractions $3(I_n(V_C) - I_p(V_C))$ and $3(I_p(V_C) - I_n(V_C))$, respectively. These currents are added to bias currents at the common source points of the differential pairs.

The measurement results of the rail-to-rail input stage are given in Fig. 6 for a supply voltage of 2 V. About 15% increase in g_m occurs during transition regions where one pair is partially on, while the other pair is fully on.

IV. Conclusion

Some of the issues facing the analog designers in implementing low voltage circuits have been discussed. Possible solutions to a variety of problems are investigated. These solutions include the use of regulated cascode circuits for implementing low voltage current mirrors and linear transconductors, lateral BJT's for low noise design, and reducing threshold voltage by forward biased bulk-source operation. Two different circuits demonstrating the usefulness of these techniques have been presented. The results have supported with experimental data.

References

[1] C. Hu, "Future CMOS scaling and reliability," *Proc. IEEE*, vol. 81, pp. 682–689, May 1993.

[2] B. Davari, R. H. Dennard, and G. G. Shaidi, "CMOS scaling for high performance and low power: The next ten years," *Proc. IEEE*, vol. 83, pp. 595–606, Apr. 1995.

[3] R. G. H. Eschauzier, R. Hogervorst, and J. H. Huijsing, "A programmable 1.5 V CMOS class-AB operational amplifier with hybrid nested miller compensation for 120 dB gain and 6 MHz UGF," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1497–1504, Dec. 1994.

[4] P. C. Yu and H. S. Lee, "A high-swing 2-V CMOS operational amplifier with replica amp gain enhancement," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1265–1272, Dec. 1993.

[5] E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE J. Solid-State Circuits*, vol. 25, pp. 289–298, Feb. 1990.

[6] T. Kobayashi and T. Sakurai, "Self-adjusting threshold-voltage scheme (SATS) for low-voltage high-speed operation," in *Proc. IEEE CICC '94*, 1994, pp. 12.3.1–12.3.4.

[7] E. A. Vittoz, "MOS transistors operated in the lateral bipolar mode and their application in CMOS technology," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 273–279, Apr. 1983.

[8] R. Hogervorst, R. J. Wiegerink. P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-g_m rail-to-rail input stage," in *Proc. ISCAS*, 1992, pp. 2876–2879.

Application of the Back Gate in MOS Weak Inversion Translinear Circuits

Jan Mulder, Albert C. van der Woerd, Wouter A. Serdijn, and Arthur H. M. van Roermund

***Abstract*—Though the MOS transistor is a four-terminal device, it is most often used as a three-terminal device. Therefore, a large number of possible MOS circuits are overlooked. In this brief, the four-terminal point of view is elaborated with respect to MOS weak inversion translinear circuits, a class of circuits naturally very suitable for low-voltage and low-power applications. Some new circuits are described which sometimes are more suitable for low-voltage applications than bipolar translinear networks performing the same function. It is also shown that, using the back gate, translinear networks can be derived which cannot be realized with bipolar transistors. These network topologies increase the possibilities offered by translinear technology. As an example, measurement results of a low input-voltage current mirror and a $\sin(x)$-circuit are shown.**

I. Introduction

The first translinear circuits were designed using bipolar transistors [1]. However, MOS transistors in weak inversion are also suitable for this type of circuits because of the almost exponential relation between the gate-source voltage and the drain current in this region [2].

Weak inversion translinear circuits have two fundamental advantages over bipolar translinear circuits. First, there is the absence of base current, which is a major source of errors in most bipolar designs and also causes noise.

Second, the MOS transistor is a four-terminal device. In subthreshold, the relation between the bulk-source voltage and the drain current

Manuscript received February 15, 1995; revised July 2, 1995.

The authors are with the Electronics Research Laboratory, Department of Electrical Engineering, Technical University of Delft, Delft 2628 CD, The Netherlands.

IEEE Log Number 9415059.

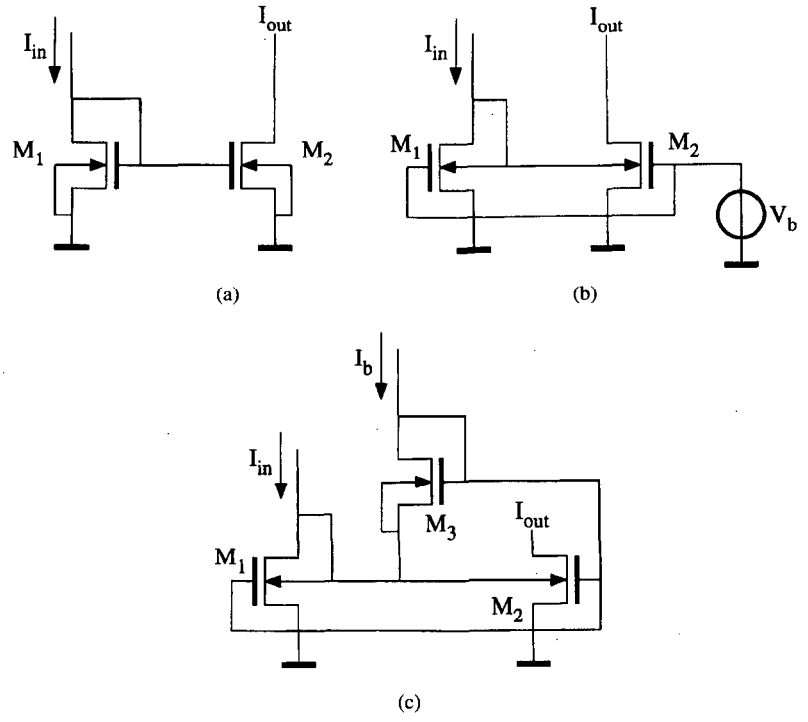

Fig. 1. (a) Conventional current mirror. (b) Bulk current-mirror. (c) Improved bulk current-mirror.

is also exponential. A simple model for the drain current of an MOS transistor in saturation is given by [3]

$$I_{\mathrm{DS}} = I_0 e^{V_{\mathrm{GS}}/\kappa U_T} e^{\left(1-\frac{1}{\kappa}\right)V_{\mathrm{BS}}/U_T} \tag{1}$$

where I_0 is the zero-bias current, V_{GS} and V_{BS} are the gate-source and bulk-source voltage, $U_T = kT/q$ is the thermal voltage and κ is the subthreshold slope. As shown in this article, the use of the bulk terminal as a second gate, or back gate, enables us to design translinear circuits that are not possible when using bipolar transistors. For the circuits described in this article, bandwidth is supposed to be less relevant and will be treated only briefly. The noise characteristics still have to be examined.

In Section II, some important aspects of bipolar translinear networks are summarized. In Section III, we will first treat the use of the back gate in the current mirror. In Section IV, less trivial translinear circuits will be treated. Some MOS topologies are described which sometimes are more suitable for low-voltage designs. Section V describes some MOS topologies which are not covered by the equations describing bipolar translinear networks. Measurements on a $\sin(x)$-circuit are treated in Section VI.

II. Bipolar Translinear Networks

In searching for new MOS translinear circuits, knowledge of the possibilities of bipolar translinear circuits is necessary. Much research in this area has been performed in [1], [4]. For the sake of brevity, we resort to a short and incomplete outline only. In [4], the investigation is restricted for reasons of complexity, to circuits containing one loop of at most eight transistors or two loops of at most seven transistors. Under these restrictions, 26 possible topologies remain, each described by one of only four equation structures

$$f_1 f_2 \cdots f_n = g_1 g_2 \cdots g_n \qquad n = 2, 3 \text{ or } 4 \tag{2}$$

$$f_1 f_2 = g_1 g_2 = h_1 h_2 \tag{3}$$

$$\frac{f_1}{f_2} = \frac{g_1}{g_2} = \frac{h_1}{h_2} \tag{4}$$

$$\frac{f_1 f_2}{f_3} = \frac{g_1 g_2}{g_3} = h \tag{5}$$

where f_i, g_i and h_i represent the collector currents, which are linear combinations of the input and output currents. The first equation structure (2) applies to one-loop circuits, (3) to (5) describe two-loop circuits.

A simple way to design a MOS translinear circuit is to translate a bipolar circuit directly to its MOS equivalent, replacing the base-emitter junctions by gate-source voltages and connecting the substrate terminal of each MOS transistor to its source. Using this approach, the back gate is not exploited and therefore a class of new circuits is ruled out in advance.

III. Bulk Current-Mirror

To demonstrate the usefulness of the back gate, we start with an examination of the current mirror, a trivial translinear circuit. In the conventional current mirror the input current I_{in} forces the gate voltage, while the back gate is connected to the source, see Fig. 1(a). However, it is equally possible to bias the gates on a constant voltage and use the back gate to mirror the input current, as shown in Fig. 1(b). The input voltage of the bulk current-mirror is lower than the gate-source voltage of the conventional current mirror and therefore the bulk mirror might be useful for low-voltage applications.

The measured and ideal output current of the bulk current mirror are shown in Fig. 2. The gates are biased at 350 mV. The operating range of the bulk mirror is more than two decades. For low input currents, the bulk voltage becomes less than 100 mV. Therefore, the input transistor transits into its linear region, causing a deviation from

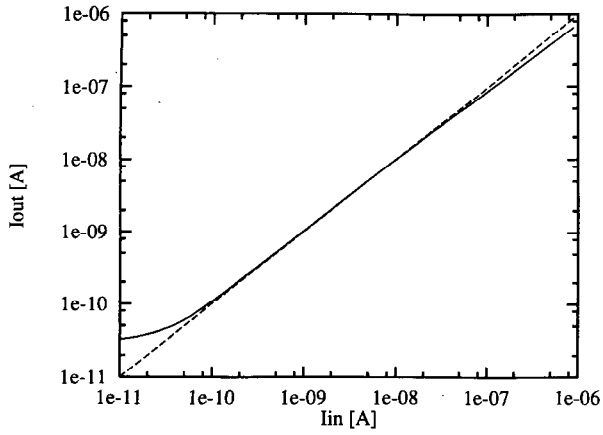

Fig. 2. Measured (—) and ideal (– –) output current of the bulk current-mirror, $W/L = 108/7\mu m/\mu m$.

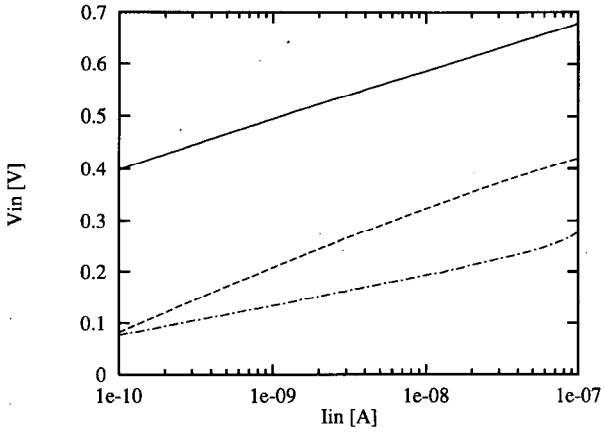

Fig. 3. Measured input voltages of the conventional mirror (—), the bulk mirror (– –) and the improved bulk mirror (– · –).

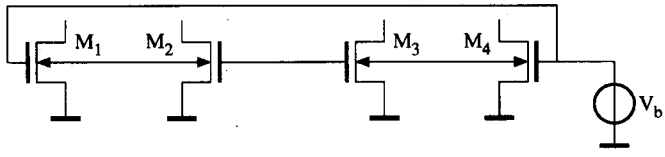

Fig. 4. Translinear loop of gate-bulk voltages.

the ideal transfer function. The bulk-source junction is biased slightly forward causing some leakage current. For high input currents, the bulk voltage becomes about 400 mV and the leakage current is no longer negligible with respect to the input signal.

The main disadvantage of the bulk mirror is the small input current range with respect to a conventional current mirror. First, this is caused by the relatively small input voltage range of about 300 mV. Second, the slope of the $V_{BS} - \ln I_{DS}$ characteristic is usually about twice as steep as the slope of the $V_{GS} - \ln I_{DS}$ plot. The second effect can be canceled out by driving the gate as well as the back gate, connecting them by a voltage source, as is shown in Fig. 1(c), where M_3 is a simple realization of the voltage source. The current I_b through M_3 is added to I_{in} and therefore I_b has to be much smaller than I_{in}. Another possibility is to compensate for I_b by subtracting I_b from I_{out}. The slope of V_{in} versus $\ln I_{in}$ of this mirror is the same as the slope of a bipolar current mirror, which is 59 mV/decade, as shown by the input voltage measurements in Fig. 3.

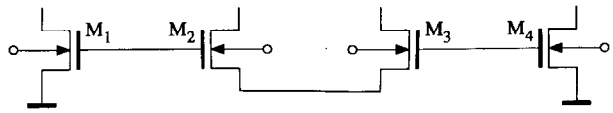

Fig. 5. Loop in up-down topology with floating back gates.

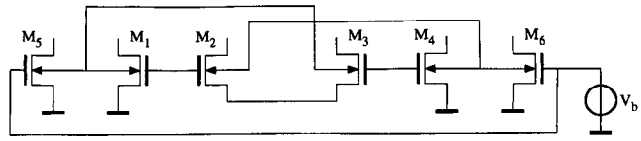

Fig. 6. Circuit realizing equation structure (7).

The bandwidth of the bulk current mirror is about four times lower than the bandwidth of a conventional mirror. Both the input resistance and the input capacitance are about two times larger. Thus, the price paid for low-voltage operation is a reduction of bandwidth.

IV. MOS Translinear Topologies Described by "Bipolar" Equations

In less trivial translinear circuits, the use of the back gate also leads to the development of new circuits. A four-transistor loop in up-down topology is shown in Fig. 4. Instead of the usual loop of gate-source voltages, this loop consists of gate-bulk voltages. Using (1), we find that the circuit is described by (2) with $n = 2$. The topology of Fig. 4 is thus characterized by an equation which also describes a bipolar four-transistor translinear network. However, it is quite different from the corresponding bipolar circuit. All sources of the MOS transistors are connected to the same voltage, which is an advantage in a low-voltage low-power environment. In contrast to bipolar circuits, the MOS circuit needs one gate or bulk voltage to be biased. In theory, this can be done without power consumption, since the gate and back gate draw no current. In Fig. 4, a gate voltage is biased. An example of the circuit is found in [5], where it is used in the feedback path of an amplifier to realize a $\sqrt{x}$-function. There, a bulk voltage is biased.

With networks containing two loops of gate-bulk voltages, the "bipolar" equation structures (4) and (5) can also be realized with all sources grounded; (3) cannot be realized by a circuit with all sources on ground potential.

In summary, the use of the back gate enlarges the number of translinear topologies. With respect to the 26 bipolar topologies, these new topologies might be more suitable for low-voltage low-power applications.

V. Additional Translinear Equation Structures

The circuits treated in the previous section and described by one of the known "bipolar" equation structures (2), (4), or (5) are not the only results of the use of the back gate; as shown in this section, new equation structures can be realized using all four terminals of the MOS transistors.

In Fig. 5, a four-transistor gate-source loop is depicted in an up-down topology. The back gates have not been connected yet. Applying (1), it can be derived that the loop satisfies

$$\frac{I_1 I_3}{I_2 I_4} = \exp\left(\frac{V_{BS1} - V_{BS2} + V_{BS3} - V_{BS4}}{\eta U_T}\right) \tag{6}$$

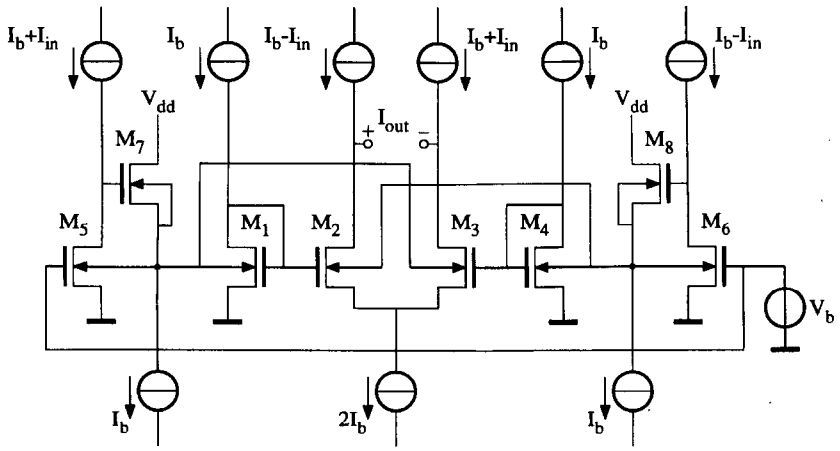

Fig. 7. Sin(x)-circuit, $W/L = 108/7\mu\text{m}/\mu\text{m}$.

where $1/\eta = 1-1/\kappa$, see (1). The source voltages of M_1 and M_4 and of M_2 and M_3 are the same. As a consequence, they cancel out. Now, it is also possible to "add" the back gate voltages of M_1 and M_3 and of M_2 and M_4 simply by connecting them.

Next, if the back gates of M_1 and M_4 are connected to the back gates of two supplementary MOS transistors M_5 and M_6 with equal gate voltage, a theoretically process- and temperature-independent transfer is obtained. The resulting fundamental topology, depicted in Fig. 6, is described by an equation structure containing two squared currents

$$\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2}{I_6^2}. \tag{7}$$

This equation structure is different from the basic "bipolar" equations (2)–(5). The topology of Fig. 6 actually consists of two loops of gate-bulk voltages. The first loop is formed by M_1, M_2, M_6, and M_5. The second by M_3, M_4, M_6, and M_5.

A more complex equation structure with four squared currents can be obtained by inserting a bulk-connected pair between the gates of M_5 and M_6 in Fig. 6, grounding the sources of these two extra transistors. The resulting topology is described by

$$\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2 I_7^2}{I_6^2 I_8^2}. \tag{8}$$

An equation structure with two cubed currents is also possible, starting with a loop of six gate-source voltages in up-down configuration, as in Fig. 5. This topology is described by

$$\frac{I_1 I_3 I_5}{I_2 I_4 I_6} = \frac{I_7^3}{I_8^3}. \tag{9}$$

As a conclusion, using the back gate in MOS translinear circuits, new equation structures are realized, even within the limit of at most eight transistors. These additional equations increase the number of possible translinear solutions for the realization of a given function and might result in a more area-efficient realization because of their higher functional complexity. An application of the new equation (7) and some measurement results are described in the next section.

VI. Applications and Measurements

A possible application of the general topology shown in Fig. 6 is a differential sine shaper. The sine function can be approximated by a rational function [1]

$$\sin \pi x \approx \frac{x - x^3}{1 + x^2}. \tag{10}$$

Another way of writing this sine approximation is the implicit decomposition [4]

$$\frac{1 + z + x}{1 - z - x} = \frac{(1 + x)^2}{(1 - x)^2} \tag{11}$$

where z represents the output. This decomposition can easily be fitted on equation structure (7) by choosing $I_2 = I_b - I_{\text{out}} - I_{\text{in}}$, $I_3 = I_b + I_{\text{out}} + I_{\text{in}}$, $I_5 = I_b + I_{\text{in}}$, $I_6 = I_b - I_{\text{in}}$, and $I_1 = I_4$. The sine shaped output current is obtained by $2I_{\text{out}} = I_3 - I_2 - 2I_{\text{in}}$.

The circuit is depicted in Fig. 7. A breadboard version of the circuit was built to verify experimentally the results of the previous section. M_7 and M_8 are two simple floating voltage sources, which are used to keep M_3 and M_4 in saturation for bulk voltages of less than 100 mV. The supply voltages are $\pm$ 1 V. The mismatch is quite large due to the breadboard realization. The average drain current mismatch is about 9%. As a consequence, the influence of the restricted validity of the simple drain current model (1) cannot be measured.

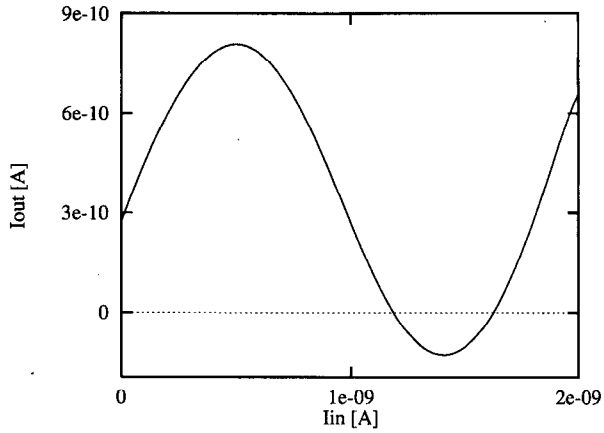

Fig. 8. Measured output current of the sin(x)-circuit.

The measured output current is shown in Fig. 8. Simple current mirrors are used to supply the currents to the actual $\sin(x)$-circuit. The gates of M_5 and M_6 in Fig. 7 are biased at 350 mV, the bias current I_b is 1 nA and the input current I_{in} varies from 0 to 2 nA. The drains of M_2 and M_3 are loaded by two 500 mV voltage sources. Despite the rather large mismatch the result is quite reasonable.

The application of the general topology shown in Fig. 6 is not restricted to the example treated in this section. Many other functions will fit on the topology, which in fact is the main strength of translinear technology.

VII. Conclusion

Regarding the MOS transistor as a four-terminal device with a front and a back gate, translinear circuits were described which in some situations are more suitable for low-voltage applications. Also, it has been shown that the equations describing bipolar translinear circuits are not sufficient to describe all possible MOS translinear networks as well. Additional equation structures have been derived, which enlarge the number of possible translinear designs for a function to be realized, and might result in more area-efficient implementations. Measurements were performed which verify the theory, although they suffer from rather large mismatch of the transistors due to the breadboard realization. As a consequence, the influence on the circuit of the inaccuracy of the simple subthreshold model, which was used in the calculations, could not be measured. The measurements do show that the influence must be rather small. Further research on this point, both empirical and theoretical, will be performed.

References

[1] B. Gilbert, "Translinear circuits: A proposed classification," *Electron. Lett.*, vol. 11, pp. 14–16, Jan. 1975.

[2] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.

[3] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. SC-12, pp. 224–231, Mar. 1977.

[4] E. Seevinck, *Analysis and Synthesis of Translinear Integrated Circuits*. New York: Elsevier, 1988.

[5] M. V. D. Gevel and J. C. Kuenen, "$\sqrt{x}$ Circuit based on a novel, back-gate-using multiplier," *Electron. Lett.*, vol. 30, pp. 183–184, Mar. 1994.

A Very Low Frequency, Micropower, Low Voltage CMOS Oscillator for Noncardiac Pacemakers

Changku Hwang, Steven Bibyk, Mohammed Ismail, and Brian Lohiser

***Abstract*—One of the most power consuming components of a modern noncardiac pacemaker is the oscillator circuitry. This brief details the design of a micropower, low voltage, low frequency oscillator consisting of CMOS devices operating in subthreshold. Since the frequency of a typical oscillator is proportional to Current/Capacitance, the operation of the transistors in the subthreshold region allows the size of the capacitance to be reduced significantly in addition to decreasing the quiescent power consumption. The proposed prototype oscillator was fabricated in a 2 μm n-well CMOS process and occupies 0.281 mm^2 including a 100 pf capacitor which takes 77.8% (0.219 mm^2) of the total area. Experimental results show a frequency of oscillation as low as 0.3 Hz and a power consumption of around 0.24 μW at 0.3 Hz to 0.3 μW at 100 Hz with a 2 V supply voltage.**

I. Introduction

Recently, there has been considerable interest in developing experimental pacemakers for chronic testing of laryngeal nerves [1]. The difficulty in using cardiac pacemakers for these tests is the different parameters and potential closed loop control mechanisms that are needed for laryngeal studies. Thus, this brief describes the initial development of a set of CMOS VLSI circuits for noncardiac pacing. The main focus here is on the oscillator circuitry which must operate at a very low frequency.

The modern noncardiac pacemaker must also be compact and long-lived to be implanted into the human body. By reducing the size of the capacitance and decreasing the quiescent power consumption (and hence the number of batteries required), these constraints can be attained. There are also many other applications which require a low voltage, low power oscillator as low voltage designs rapidly become more prevalent.

Since the oscillator is the primary driving element in the entire circuit, it must be designed to minimize power consumption. In this brief, we have designed a CMOS oscillator operating in the subthreshold region in which the drain current of a MOS transistor is expressed as [2]–[5]

$$I = \left(\frac{W}{L}\right)_i I_{DO} e^{\frac{(V_{gs}-V_T)}{nU_t}} \tag{1}$$

where $I_{DO} = \frac{2K(nU_t)^2}{e^2}$, $U_t = \frac{kt}{q}$, and n are reverse voltage saturation current, thermal voltage, and slope factor, respectively and $K = \mu C_{OX}$.

As stated, two advantages are simultaneously achieved by doing so; first, the power consumption is significantly decreased, and second, the area of the capacitor (which is inversely related to the frequency)

Manuscript received April 5, 1995; revised July 12, 1995. This work was supported in part by the Cleveland Clinic Foundation, Cleveland, OH. This paper was recommended by Guest Editors A. Rodríguez-Vázquez and E. Sánchez-Sinencio.

The authors are with the Solid-State Microelectronics Laboratory, Department of Electrical Engineering, The Ohio State University, Columbus, OH 43210 USA.

IEEE Log Number 9415060.