An RF Energy Harvesting and Power Management Unit Operating over -24 to +15 dBm Input Range

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***Abstract*—This paper presents the design and measurement of an RF energy harvesting and power management unit that operates across a wide range of available input power, from -24 to +15 dBm. The system comprises an adaptive impedance matching network, a single-stage cross-coupled differential-drive rectifier, a start-up charge pump, an adaptive buck-boost converter, a maximum power point tracking (MPPT) circuit and a control loop to regulate the load voltage. The MPPT circuit controls the switching frequency of the buck-boost converter and configures the impedance matching network, optimizing the interfaces between the rectifier and antenna and between the rectifier and the storage capacitor, guaranteeing that the power is being harvested at maximum efficiency. To boost the rectifier output, to accumulate energy in the storage capacitor and to provide energy to the load, a single-inductor buck-boost converter that has two inputs and three outputs is used. Circuit techniques that reduce the power consumption of the control circuits and that allow for adapting the interfaces between the antenna, the rectifier and the load are presented. The peak harvesting efficiency of the system is 40.2%, when presented with an RF source of -9.1 dBm available power and 403.5 MHz frequency.**

***Index Terms*—RF energy harvesting, DC-DC converter, maximum power point tracking, impedance matching.**

I. Introduction

ENERGY harvesting is an enabling technology for powering devices that are difficult or inconvenient to access with wires, such as devices in IoT, biomedical or several industrial applications. The advantages of radio-frequency (RF) energy harvesting is the ubiquity of RF signals in urban environments and their ability to reach environments in which other sources of energy (sunlight, vibrations, temperature gradients, etc.) are not present. However, RF signals may present low power density and therefore require power converting circuits that are efficient at low power levels. At the same time, when a dedicated RF power transmitter is used, a large available power may be presented to the RF energy harvester (RFEH) and if it is not designed to accommodate such power levels the extra energy will be wasted.

The available power P_{av} presented at the terminals of the RFEH antenna may vary due to factors such as antenna alignment, distance from the source, and network traffic [1], [2]. The value of P_{av} is hard to predict in practice, so RFEHs are commonly designed to achieve high sensitivity, in order to enable new applications [3]–[5]. However, if no adaptability is present, such designs present a large reduction in power conversion efficiency (PCE) as soon as P_{av} becomes large, as we will discuss in this paper.

To understand the variation of PCE with P_{av}, each block of the RFEH and the interfaces between them must be analyzed. The main blocks that compose an RFEH are: the impedance matching network, which performs the conjugate matching of the rectifier impedance to the antenna impedance; the rectifier, which converts the RF signal into a DC voltage; and the DC-DC converter, which is not strictly necessary in an RFEH but can boost the rectifier output voltage and at the same time present an optimum load to it, working as a power matching interface between the rectifier and the load.

This paper presents an RFEH and power management unit that harvests energy from a wide available power range and presents high sensitivity. We analyze each of the aforementioned blocks and show how their efficiency and their impedances, either in the RF or DC domain, change with P_{av}, how they affect the PCE, and how to make them adaptive to such variation. In order to introduce adaptability to the circuits while maintaining high power conversion efficiency and high sensitivity, new circuit techniques are introduced. The novel circuits presented in this paper are: a low-power, compact input power estimation circuit employed in the maximum power point tracking (MPPT) circuit, configurable power switches employed in the DC-DC converter, and a high-speed low-power zero current detector also employed in the DC-DC converter. Furthermore, the designed system employs an adaptive impedance matching network and a method of regulating the load voltage while performing energy harvesting using a single power inductor.

The system is designed in a standard $0.18\,\mu\mathrm{m}$ CMOS technology and the target frequency of the RF input is $403.5\,\mathrm{MHz}$, the center frequency of the MICS band, suitable for biomedical devices. In Section II, the system architecture is introduced. The impedance matching and rectifier are presented in Section III. In Section IV, the circuits employed in a dual-input triple-output buck-boost converter are presented, which serves simultaneously as a boost converter and a voltage regulator. The MPPT circuit is discussed in Section V. The measurement results are discussed in Section VI. Finally, concluding remarks are presented in Section VII.

II. System Description

The system block diagram is presented in Fig. 1. As mentioned, the system's goal is to convert the RF power received by the antenna (modelled as a voltage source V_{ant} in series

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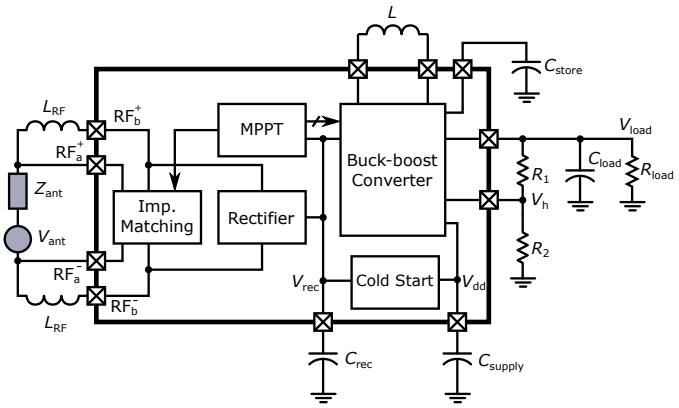

Fig. 1. Simplified system block diagram.

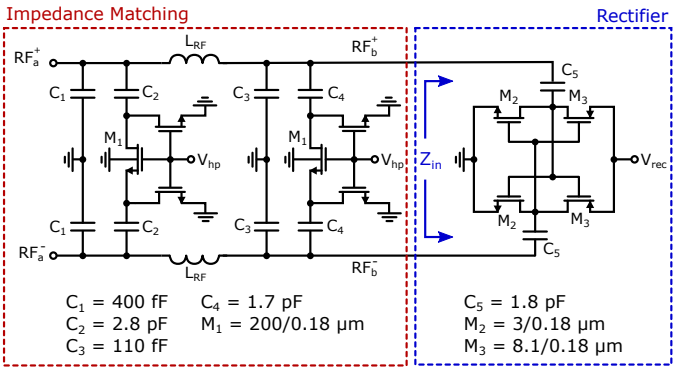

Fig. 2. Adaptive impedance matching and rectifier circuit schematics.

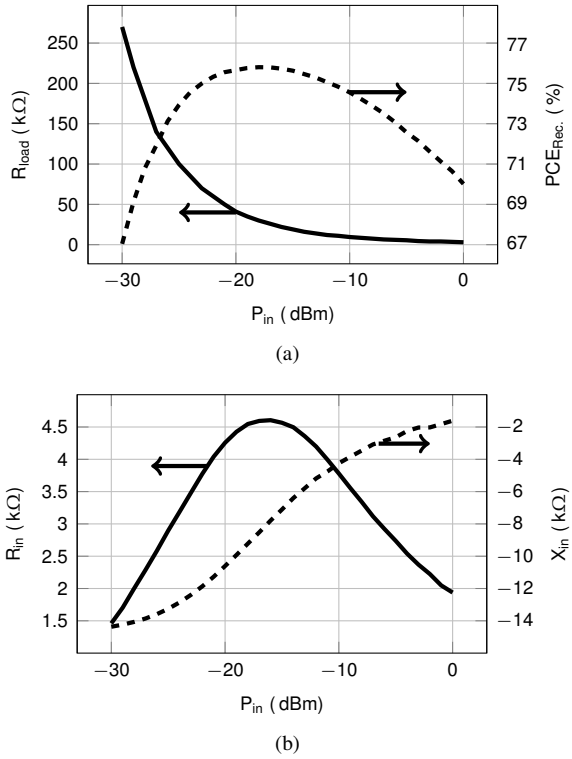

Fig. 3. Rectifier response to input power variation: (a) efficiency and optimum load; (b) input impedance (resitance $R_{\rm in}$ and reactance $X_{\rm in}$).

with an impedance $Z_{\rm ant}$) into charge (stored on capacitor $C_{\rm store}$) and to supply the load $R_{\rm load}$ (capacitor $C_{\rm load}$ is used to filter the voltage across $R_{\rm load}$). A single-inductor dual-input triple-output (SIDITO) buck-boost DC-DC converter is used to perform both tasks [6]. It draws energy from the rectifier to charge $C_{\rm store}$ and later draws energy from $C_{\rm store}$ to supply $R_{\rm load}$. If the rectifier can deliver enough power, the energy previously stored in $C_{\rm store}$ is saved and $R_{\rm load}$ is supplied directly from the rectifier. The converter regulates $V_{\rm load}$ by comparing a fraction of it ($V_{\rm h}$) to a reference $V_{\rm ref}$ (not shown in Fig. 1, but generated on chip [7]) and charging capacitor $C_{\rm load}$ when $V_{\rm h} \leq V_{\rm ref}$. Furthermore, the system draws power from capacitor $C_{\rm supply}$ to operate, which is also charged by the DC-DC converter. An additional cold start circuit, a Dickson charge pump [8] driven by a conventional ring oscillator [9] that can operate from input voltages down to $300\,\mathrm{mV}$, is necessary to initially charge $C_{\rm supply}$ when it is fully depleted.

The MPPT block provides control bits to the impedance matching and the buck-boost converter. It maximizes the input power being drawn by the buck-boost converter. By estimating this input power at every step, $P_{\rm av}$ is inferred and the impedance matching is set to the configuration that best suits the source at the moment. Therefore, a single control loop controls both interfaces, simplifying the system design and reducing its power consumption.

III. RF-DC Converter

The rectifier is the least efficient block in the power conversion chain and by reducing the number of rectifier stages it is possible to increase its power conversion efficiency, at constant input power and under penalty of having a lower DC output voltage [10]–[12]. Since a DC-DC converter can be used to boost this voltage with a high efficiency, the use of a single-stage rectifier is a sensible choice. The rectifier topology selected for this work is the cross-coupled differential-drive (CCDD) rectifier [13]. This topology was selected because it has high efficiency and sensitivity [4], [5]. Its circuit schematic is shown in Fig. 2 together with the implemented impedance matching network.

The rectifier impedance and optimum load vary with input power [14]. In Fig. 3 the simulation results of the rectifier show this variation. For each value of the input power $P_{\rm in}$, $R_{\rm load}$ is set to the value that results in the highest power conversion efficiency $\mathrm{PCE_{Rec.}}$, shown in Fig. 3(a), and the input impedance $R_{\rm in}+jX_{\rm in}$ is then extracted in that condition, shown in Fig. 3(b).

Ideally, the impedance of the rectifier should be always matched to the antenna, but since the rectifier impedance changes with the input power, this cannot be achieved with a fixed impedance matching network. To design an adaptive matching network, we employ the capacitor-bank technique in a π-network topology, as presented in Fig. 2. This topology employs switches in the parallel branches in a way that its $V_{\rm GS}$ is large when the switch is on, reducing $R_{\rm ON}$. This is especially important in the high power condition, when the input voltage is high.

The matching is implemented for two cases: high and low $P_{\rm av}$. When $V_{\rm hp}$ is low, switches M_1 are off and the network

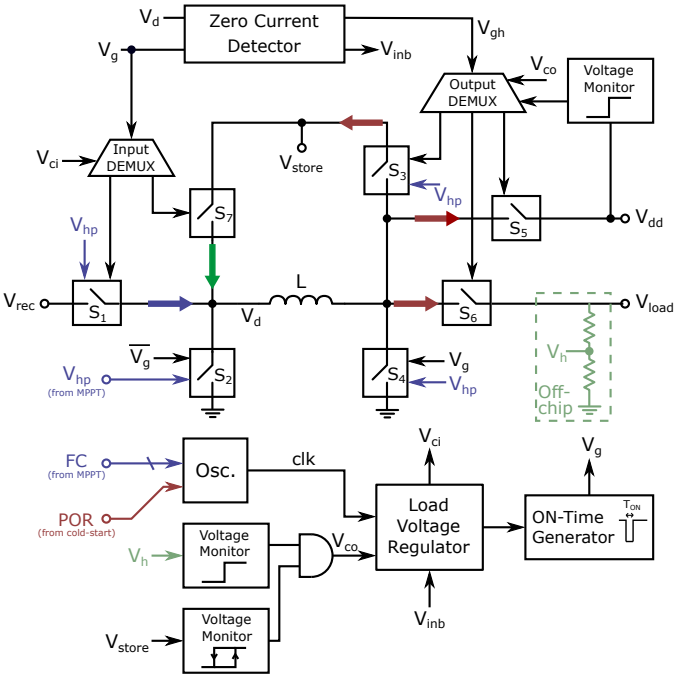

Fig. 4. Block diagram of the buck-boost converter.

is configured for harvesting at low power levels. When $V_{\rm hp}$ is high, the network is in high-power mode. The signal $V_{\rm hp}$ is provided by the MPPT block, discussed in Sec. V. Transistors M_1 are designed to be wide enough in order to keep the quality factor of the capacitors high ($Q > 150$), but not too wide to present large parasitic capacitance.

IV. Buck-Boost Converter

The DC-DC converter presents a load to the rectifier, which can be optimized for a varying $P_{\rm av}$ [15]. Conventionally, an additional converter such as an LDO or buck converter is used to supply and regulate the voltage across the load. In this work, we employ a SIDITO buck-boost converter to perform both tasks. Its block diagram along with its control blocks is presented in Fig. 4.

The two inputs of the converter are the rectifier output node $V_{\rm rec}$ and the storage capacitor node $V_{\rm store}$, which are connected to the power inductor L through switches S_1 and S_7, respectively. The three outputs are $V_{\rm store}$, $V_{\rm dd}$ and $V_{\rm load}$, connected to L through switches S_3, S_5 and S_6, respectively. Inductor L is charged from one of the inputs, when $V_{\rm g}$ is low, for a fixed period $T_{\rm ON}$, the ON time. Subsequently, it is discharged to one of the outputs, which takes a time $T_{\rm OFF}$, the OFF time.

In order to keep the input resistance of the DC-DC converter, as seen from $V_{\rm rec}$, constant, the input current must be independent of the output voltage. Otherwise, the converter must be controlled for a changing output voltage that depends not only on the charging and discharging of the capacitors but also on which output is active. The decoupling of input resistance and output voltage can be performed using the buck-boost converter operating in discontinuous conduction mode

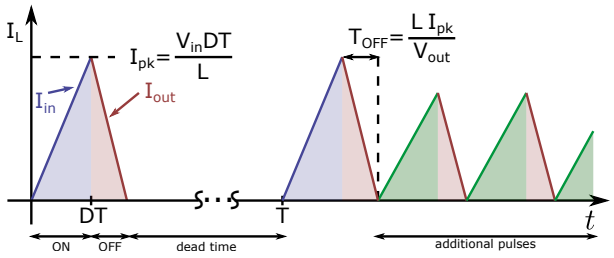

Fig. 5. Example of inductor current, in which $V_{\rm in}$ is either $V_{\rm rec}$ or $V_{\rm store}$ and $V_{\rm out}$ is $V_{\rm store}$, $V_{\rm dd}$ or $V_{\rm load}$, depending on the converter configuration.

(DCM) and open loop. The average input resistance of the buck-boost converter in DCM is given by [16]–[18]:

$$R_{in,avg} = \frac{V_{\rm rec}}{I_{in,avg}} = \frac{2L}{D^2 T}, \tag{1}$$

in which T is the switching period and D is the duty cycle of $T_{\rm ON}$ ($D = T_{\rm ON}/T$). Since $T_{\rm ON}$ and L are kept constant, the input resistance is controlled by changing T.

Once every clock cycle, a current pulse is drawn from $V_{\rm rec}$. After the first pulse, when the inductor current falls to zero, more pulses are drawn from $C_{\rm store}$ when it is necessary to charge the load. Fig. 5 illustrates the inductor current waveform for two different scenarios. In the first scenario, the first current pulse is drawn from $V_{\rm rec}$ and the dead time starts immediately after it. This happens when there is not enough energy in the system (either in $C_{\rm supply}$ or $C_{\rm store}$) or when $V_{\rm load}$ is above the target voltage. In the second cycle, because $V_{\rm load}$ is below the target, more pulses are drawn from $C_{\rm store}$ and directed to $C_{\rm load}$. The dead time starts only when $V_{\rm load}$ is above the target or $V_{\rm store}$ is below a critical level.

During the first current pulse of every clock cycle, once switches S_1 and S_4 are turned off, S_2 and one of the switches S_3, S_5 or S_6 are turned on. If $V_{\rm dd} < 1.8\,{\rm V}$, S_5 is turned on. The charging of $V_{\rm dd}$ has the highest priority. If $V_{\rm dd} > 1.8\,{\rm V}$, switch S_3 is turned on to charge $C_{\rm store}$. If $V_{\rm store}$ has reached $1.8\,{\rm V}$ and $V_{\rm load}$ is below the target level, which can be configured by the selection of R_1 and R_2 shown in Fig. 1, S_6 is turned on. The charging of $V_{\rm load}$ will continue until $V_{\rm store}$ drops below $0.4\,{\rm V}$. This is done to guarantee that there is enough energy to supply the load for a minimum amount of time. The monitoring of $V_{\rm store}$ is performed by a latched comparator that compares $V_{\rm ref}$ to $V_{\rm store}$ or to a divided version of $V_{\rm store}$. Whether the comparator is connected to $V_{\rm store}$ or its divided version is controlled by the comparator's output, which creates a hysteresis. When the current pulse is finished, there will be a rising edge of $V_{\rm inb}$, triggering the load voltage regulator. The regulator first checks if there is still enough energy in $C_{\rm store}$ ($V_{\rm store}$ monitor output is high) and if $V_{\rm load}$ is below the target level ($V_{\rm load}$ monitor output is high). If this is the case, signal $V_{\rm CO}$ is high and the regulator controls the converter to charge the load. Therefore, S_7 and S_4 are turned on for a period equal to $T_{\rm ON}$ and, after they are turned off, the procedure explained above is repeated. Otherwise, if $V_{\rm CO}$ is low, the converter stays in the dead time until the next clock cycle.

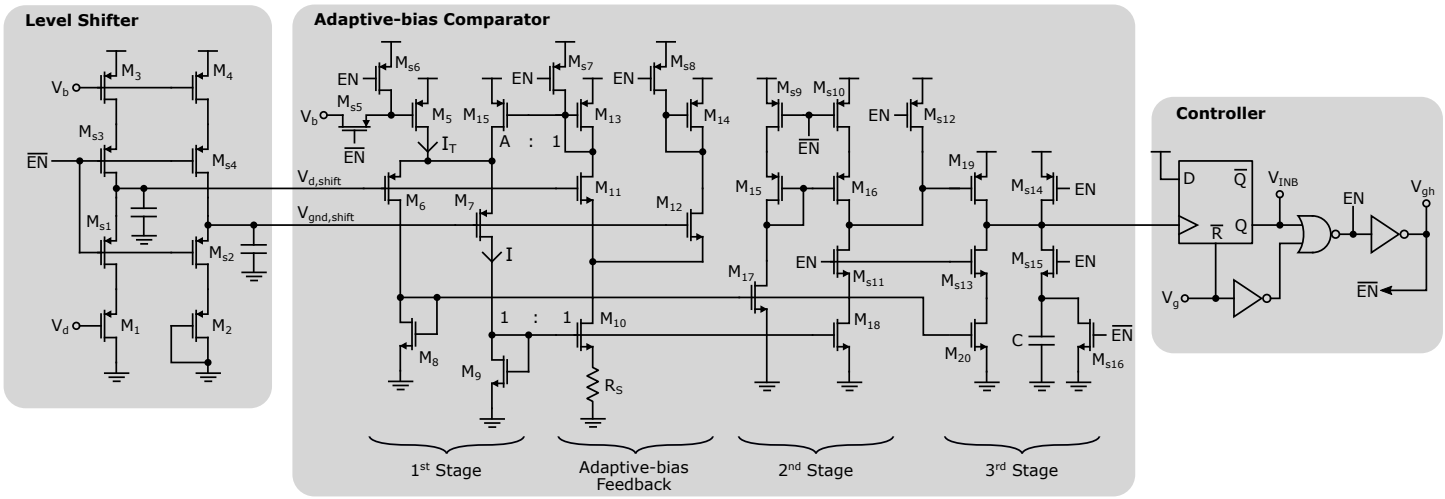

Fig. 6. Zero current detector circuit diagram.

A. Zero Current Detector

When T_{OFF} begins, the zero current detector (ZCD) is activated. Its purpose is to detect when I_{L} falls to zero and then turn off S_3, S_5 or S_6, depending on which one is active at the time, to avoid any inductor reverse current. It does so by comparing V_{d} to zero. The ZCD is composed of a level shifter, a comparator and a switches controller, as shown in Fig. 6.

1) Level shifter: Two source followers, M_1-M_2, are used to shift the ground and V_d voltages by $0.9\,\mathrm{V}$ (half the value of V_{dd}) in order to present input signals that are at an adequate level to the comparator. Transistors M_3-M_4 are current sources and transistors $M_{\mathrm{s}1}$-$M_{\mathrm{s}4}$ are switches that turn off the level shifter and hold the output value when this block is not in use. The output is held to speed up the comparison, since $V_{\mathrm{d,shift}}$ and $V_{\mathrm{gnd,shift}}$ do not have to start from a value that is too far off during the level shifter start-up.

2) Adaptive-bias comparator: A delay in detecting the zero current condition results in energy flowing back to the input, which decreases the converter's PCE. Therefore, the ZCD comparator must have low offset and be fast enough. Considering that the offset can be mitigated by proper transistor dimensioning and trimming, we focus on the comparator speed. The comparator speed increases with its bias current [19]. However, the bias current cannot be increased indefinitely because it impacts the power consumption. To overcome this issue, we introduce an adaptive-bias comparator, the bias current of which changes with its differential input voltage V_{in}. Therefore, when I_{L} is far from zero, V_{in} is large and the comparator bias current is low. When I_{L} comes closer to zero, V_{in} is close to zero as well and the bias current is large. This technique allows for a fast detection while reducing the average power consumption.

The comparator schematic is presented in Fig. 6. It is a three-stage amplifier based on the adaptive-bias amplifier presented in [20]. We introduce a differential pair and a degeneration resistor to the positive feedback loop in order to increase the current feedback factor A, reducing the average power consumption for the same delay.

The comparator's first stage is biased by a fixed current set by M_5 and an adaptive current that flows through M_{15}. The feedback loop that adjusts the bias current is formed by M_{10}-M_{15} and R_{S}. When I_{L} is positive, $V_{\mathrm{d,shift}}$ is below $V_{\mathrm{gnd,shift}}$ and the drain current I of M_7 is low. At this moment, the source voltage of M_{10} is low, so I is effectively mirrored and flows through the differential pair M_{11}-M_{12}. This pair will make the feedback current increase more sharply when V_{in} gets closer to zero. The drain current of M_{11} is multiplied by a factor A and added to the tail current through the current mirror formed by M_{15} and M_{13}. When I_{L} decreases and approaches zero, V_{in} tends to zero as well, making I equal to the half of the bias current. In the case of $R_{\mathrm{S}} = 0\,\Omega$, we can write the following equation:

$$I = \frac{2I_{\mathrm{T}}}{4 - A}. \tag{2}$$

In this case, the system is stable when A is smaller than 4. To achieve a higher A, and decrease the average power consumption, degeneration resistor R_{S} is employed. Considering the influence of this resistor and $I_{\mathrm{T}} \ll 2I$, we can then write I as:

$$I \approx \frac{A^2}{8\mu_{\mathrm{n}} C_{\mathrm{ox}} (W/L)_{10} R_{\mathrm{S}}^2} \left(1 - \frac{2}{\sqrt{A}}\right)^2, \tag{3}$$

which is stable for any value of A. However, in practice, increasing A indefinitely will not lead to less power consumption for the same delay of the converter. This is due to the increase of the parasitic capacitances of the current mirror formed by M_{15} and M_{13}, which become dominant.

To illustrate the advantage of the proposed circuit, Fig. 7 presents the current consumption of three different comparators, labeled C1 to C3. All the comparators are designed to have the same delay. Comparator C1 is designed with $A = 2$, without the differential pair in the feedback loop, and with $R_{\mathrm{S}} = 0\,\Omega$. Comparator C2 has $A = 4$, the differential pair in the feedback loop, and $R_{\mathrm{S}} = 0\,\Omega$. Finally, C3 presents $A = 8$, the differential pair in the feedback loop, and $R_{\mathrm{S}} = 40\,\mathrm{k}\Omega$, As shown in Fig. 7, the addition of the extra differential pair in C2 makes the curve steeper when close to $V_{\mathrm{in}} = 0\,\mathrm{V}$, which

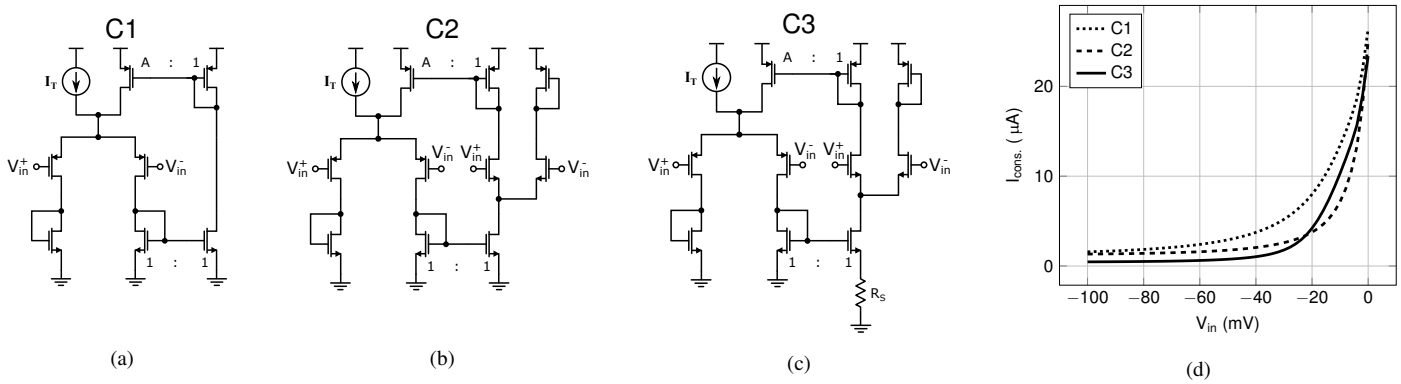

Fig. 7. Comparison of three comparators using different versions of the adaptive-bias technique. The circuits are: (a) simple feedback, (b) differential pain in the feedback loop, and (c) differential pair and source degeneration resistor in the feedback loop. The results of the current consumption of the three comparators, designed to have the same delay, are presented in (d).

saves power. Furthermore, the addition of R_{S}, in C3, allows for the reduction of the tail current when $V_{\mathrm{in}} \ll 0\,\mathrm{V}$, while obtaining the same tail current when $V_{\mathrm{in}} = 0\,\mathrm{V}$.

Transistors M_{s5}-M_{s16} act as switches that turn the comparator on or off when EN is high or low, respectively. They make sure that the current in all branches is zero and that the output voltage is high when the comparator is turned off. During this block's start-up, they initially bring the output of the comparator down by connecting the discharged capacitor C to the output node. Initially, $V_{\mathrm{d,shift}}$ and $V_{\mathrm{gnd,shift}}$ are close to each other as there is a small settling time until they reach their correct values. During this time, the comparator is also starting up and will not be able to bring its output voltage high. When the comparator bias current is high enough, its inputs are already brought further apart ($V_{\mathrm{d,shift}} < V_{\mathrm{gnd,shift}}$). This behavior ensures that the comparator output is always at a known level and that it will always present a rising edge, which is necessary for the correct operation of the switches controller.

3) Switches controller: This block switches the level shifter and the adaptive-bias comparator on and off, and generates signal V_{gh} that controls the output switches (S_3, S_5, and S_6). Furthermore, this block provides signal V_{inb}, which is used in the load voltage regulator block and indicates when there is no current flowing through the inductor.

Fig. 8 shows an example timing diagram of the signals related to the switches controller. The inputs of this block are the ZCD comparator output (V_{c}) and signal V_{g}. When V_{g} drops to logic value '0', T_{ON} begins. At this moment, the flip-flop in the switches controller (see Fig. 6) is cleared, setting V_{inb} to '0' and making sure that the level shifter and the comparator are disabled and that V_{gh} is set to '1'. When V_{g} rises, T_{OFF} begins. The level shifter and the comparator are enabled, initially setting V_{c} to '0' and V_{gh} to '0' (turning on the output power switches). When the inductor current crosses zero, V_{c} rises to '1', setting the flip-flop output to '1', which disables the level shifter and the comparator. At this moment, V_{gh} returns to '1' (turning off the output power switches and preventing negative inductor current) and the ZCD returns to its initial state.

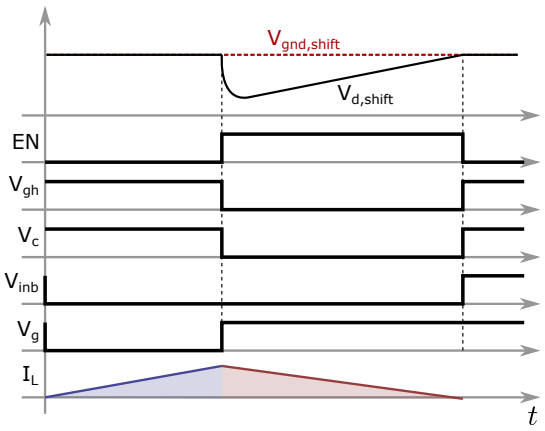

Fig. 8. Timing diagram example of the signals related to the switches controller block.

B. Oscillator, Load Voltage Regulator, and ON-Time Generator

As seen in (1), the DC-DC converter's average input resistance is proportional to its switching frequency. This frequency is set by the relaxation oscillator presented in Fig. 9. The frequency control signal FC is a 9-bit word in thermometer code that controls the oscillator bias current, and it is generated by the MPPT circuit. A comparator with hysteresis compares the voltage across capacitor C_{osc} with $V_{\mathrm{dd}}/2$, controlling whether the current is fed to or drained from C_{osc}. The output of this comparator is the system clock signal, which is used in both the DC-DC converter and the MPPT circuit.

The clock signal generated by the oscillator is processed by the load voltage regulator, which controls which input of the DC-DC converter is active, through signal V_{ci}, and generates signal clk', which is fed to the ON-time generator. Within a clk period, signal clk' contains a first rising edge, which starts a current pulse from input V_{rec}, and additional rising edges while $V_{\mathrm{h}} < V_{\mathrm{ref}}$, which start current pulses for load voltage regulation. To regulate V_{load}, voltage V_{h} is compared to a reference voltage V_{ref} by a latched comparator controlled by V_{g}, which means that the comparison is performed every current pulse. This type of regulation is possible because the

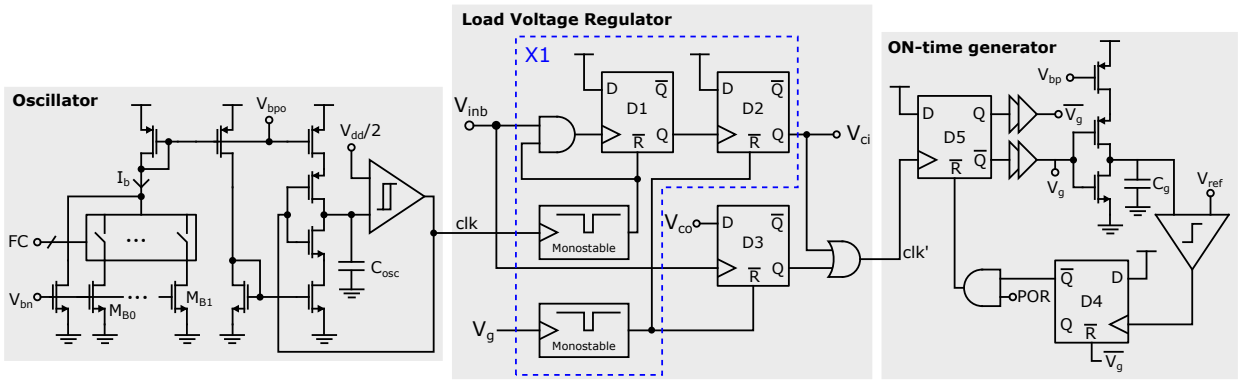

Fig. 9. Oscillator, load voltage regulator, and ON-time generator circuit diagram.

buck-boost converter operating in DCM has a single pole at low frequencies, making the system intrinsically stable [21].

The first current pulse after every clock rising edge comes from $V_{\rm rec}$, in order to keep the energy harvesting rate constant. This means that $V_{\rm ci}$ is '0' only once every clock period and it is '1' during the subsequent pulses within the clock period. However, if a clock rising edge happens and the inductor is being used, the charging cycle must be completed before a new current pulse is drawn from $V_{\rm rec}$. By doing so, it is guaranteed that the inductor current is zero before connecting the inductor to $V_{\rm rec}$ and that the converter's $R_{\rm in}$ is maintained. This behaviour is ensured by sub-circuit X1 in Fig. 9. If there is a current pulse during the clock rising edge ($V_{\rm inb}$ = '0'), it waits for it to be finished. Once the current pulse is finished or if there is no inductor current on the clock rising edge, it sets $V_{\rm ci}$ = '1' and generates a clk′ rising edge. Once the current pulse during which $V_{\rm ci}$ = '1' is finished, $V_{\rm ci}$ is set back to '0'.

If $V_{\rm co}$ is high ($V_{\rm load}$ is below the target), additional current pulses are triggered through flip-flop D3. Once the current through the inductor crosses zero, $V_{\rm inb}$ rises, setting D3 and creating a clk′ rising edge. Since $V_{\rm ci}$ is always '0' when this happens, the current pulse is drawn from $V_{\rm store}$. This circuit creates a loop that stops once $V_{\rm load}$ is above the target voltage ($V_{\rm co}$ is low).

The clk′ rising edge triggers the ON-time generator. This circuit produces a pulse by charging capacitor $C_{\rm g}$ and comparing its voltage to a reference. During start-up, the power-on reset signal, POR, is '0', ensuring that $V_{\rm g}$ is set to '1' and that the DC-DC converter is shut down. When $V_{\rm dd}$ is high enough and the oscillator and the reference generator are working, POR becomes '1' and the ON-time generator is enabled. At every rising edge of the clock, $V_{\rm g}$ is set to '0', allowing the charging of $C_{\rm g}$ through a constant current. When the voltage across $C_{\rm g}$ surpasses $V_{\rm ref}$, the comparator output rises, triggering flip-flop D4, which resets flip-flop D5. This causes $V_{\rm g}$ to return to '1', finishing the ON time.

C. Configurable Switches for Balancing Switching and Conduction Losses

The major contributors to the power losses in a switched-mode converter are the conduction loss $P_{\rm cond}$, the switching loss $P_{\rm sw}$, the shoot-through power loss $P_{\rm sh}$, and the power loss due to the control circuitry static current $P_{\rm q}$ [22]. The total power loss can be approximated by:

$$P_{\rm loss} \approx P_{\rm cond} + P_{\rm sw} + P_{\rm sh} + P_{\rm q}. \tag{4}$$

Considering that $P_{\rm sh}$ is mitigated by careful design and simulation of the power switches, their drivers and their driving signals, and that $P_{\rm q}$ can be scaled down with input power by using circuit techniques such as the ones presented previously in this paper, $P_{\rm loss}$ is minimized by balancing $P_{\rm cond}$ and $P_{\rm sw}$. For a single input power level, the power switches can be designed to this end. When the power varies over a wide range, this balance can be obtained in multiple ways, such as the simultaneous modulation of the switching frequency and pulse width [23], the adaptation of the drivers supply voltage [24] or the dynamic control of the number of transistors in parallel that compose the switches [25]–[27].

The pulse width modulation approach is not convenient in this case, since it adds an extra varying quantity (D) to the equivalent input resistance of the buck-boost converter, as seen from (1). This would complicate the design of the input power estimation circuit in the MPPT (see Section V) and increase the power consumption necessary to perform this task. Varying the supply voltage of the power switches drivers requires additional DC-DC regulators to generate the different voltage levels. A simpler and more power efficient approach is to control the number of transistors in parallel that form the power switches. Fig. 10 presents the schematics of the implemented switches, S_1-S_4. Differently from previous works, the transistor type used in the input switch must be also changed. This is due to the variation of input voltage with respect to the input power. At a low input power level, only an NMOS transistor is used in S_1. At a high input power level, a PMOS transistor is used in parallel to it, reducing the switch ON resistance at a high input voltage level. When the control bit $V_{\rm hp}$ is set to '1', the high power mode is active and all transistors are used in the switches. Otherwise, only $M_{\rm LP}$ is used. Control bit $V_{\rm hp}$ is derived from the MPPT output, since it is associated with the input power level.

Fig. 11 shows the buck-boost converter PCE when using the presented method and how it compares to the same converter using conventional switches. In the figure, the low-power mode (LPM) and high-power mode (HPM) are the modes in which

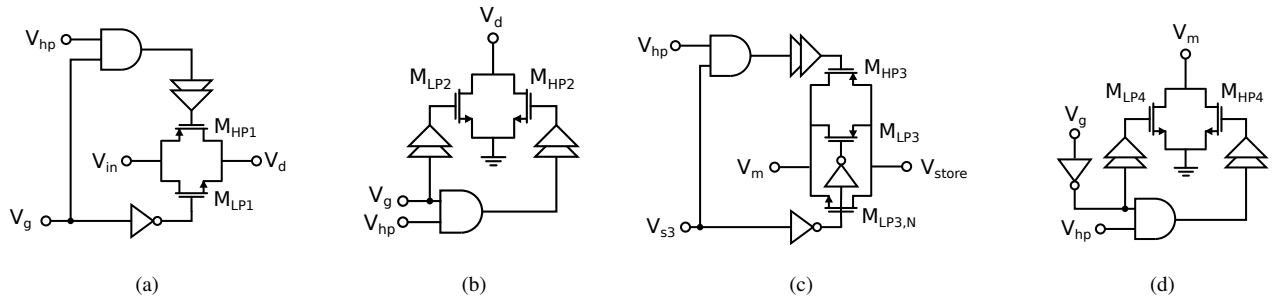

Fig. 10. Circuit schematics of the configurable switches for balancing conduction and switching losses.

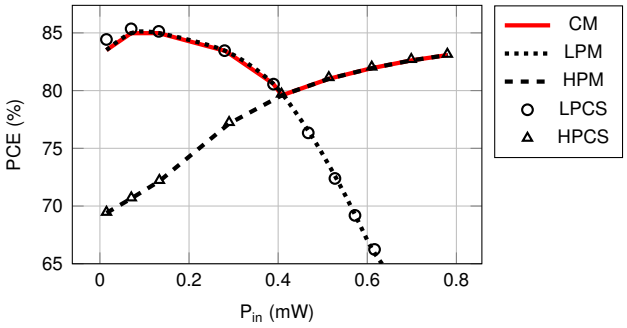

Fig. 11. Simulation results of the low-power mode (LPM) and high-power mode (HPM) of the configurable switches, the combination of both modes (CM), and the converter employing conventional switches (LPCS and HPCS).

the configurable switches are used but $V_{\rm hp}$ is kept constant, either high or low. The combination of both modes (CM) is the desired operation, in which $V_{\rm hp}$ is set to obtain the configuration that presents the highest efficiency. For the sake of comparison, the results for the converter using conventional switches that are either designed for low power (LPCS) or for high power (HPCS) are also presented. In the simulation, the output voltage is set to $1.8\,\mathrm{V}$ and the input voltage is varied from 0.3 to $1.3\,\mathrm{V}$, according to rectifier simulation results. The LPM presents much lower efficiency at higher input power because the input switch is an NMOS transistor. Therefore, the conduction losses increase considerably with the increase of input voltage. The LPCS converter performs slightly better than the LPM converter at low power levels. This is because the LPM converter presents extra losses due to the charging of the output capacitance of $M_{\rm HP}$, which is present even when the transistor is not being switched. The performances of the HPCS and the HPM converters are the same since their parasitics are the same.

Switches S_5-S_7 are not adaptive. Switch S_5 is used to charge the supply capacitor and a small fraction of the total power flows through this switch, so the total PCE is not much influenced by its losses. Switches S_6 and S_7 are used to charge the load, which can present any current. If those switches were to be made adaptive, there are two possible ways of controlling them: measuring the load power to define what configuration is the most suitable, or use control bits from the load system itself (provided that it has information about its power consumption). Making S_6 and S_7 conventional switches does not impact the possibility of supplying a large range of load currents. However, the conversion efficiency will drop for very low or very high load currents.

V. Maximum Power Point Tracking

The MPPT circuit was designed based on the Perturb and Observe algorithm, due to its inherent low power consumption [28]. Its block diagram is presented in Fig. 12. Conventionally, the input power is measured at the beginning of each MPPT cycle and held until the beginning of the next cycle, for comparison. After the power is measured, the MPPT circuits are turned off. The MPPT cycle might be very long to reduce the average power consumption. However, this requires a sample and hold circuit that can hold for a very long time, which dissipates power, or an ADC to hold the value in digital form, which increases the system complexity and area. In this work, to avoid the long hold time, the rectifier output power is sampled one extra time, within a shorter period [29].

In this work, the MPPT cycle is designed to last 4096 clock cycles and in every cycle the MPPT circuit executes the following sequence of events. At first, the DC-DC converter input power is estimated by the power estimation block. Its output is a current that is fed into a current-to-voltage converter and sampled by the sample and hold (S&H) block. A perturbation is then applied, i.e., the oscillator frequency is either increased or decreased (depending on the D-flip-flop output). After 32 clock cycles the input power is estimated once again and it is compared to the previous value by a latched comparator. Then, the analog circuits (including the S&H block) are turned off for the remainder of the MPPT cycle. The number of cycles between the two power estimations is selected to provide enough time for $V_{\rm rec}$ to settle. If the result of the comparison is positive (the input power increased due to the perturbation) the value stored by the flip-flop remains unchanged, otherwise it is inverted. This value goes to the up-down counter, which is activated to introduce the perturbation. The output (FC) of the up-down counter controls the oscillator bias current. Signal $V_{\rm hp}$ is connected to one of the bits of FC. Since the signals that control the blocks of the MPPT circuit are sequential and do not depend on external inputs except for the clock, they are generated by a 12-bit counter and a sequencer circuit.

The power estimation is based on the equation of the input power of the buck-boost converter in DCM, derived from (1).

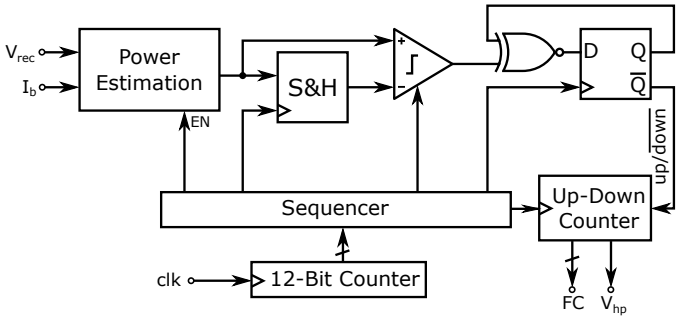

Fig. 12. MPPT block diagram.

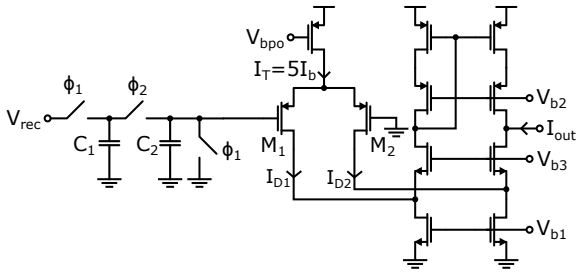

Fig. 13. Rectifier output power estimator schematic.

The switching frequency f_s is proportional to the oscillator bias current I_b, which leads to:

$$P_\mathrm{in} = \frac{V_\mathrm{rec}^2}{R_\mathrm{in}} = V_\mathrm{rec}^2 f_s \frac{T_\mathrm{ON}^2}{2L} \propto V_\mathrm{rec}^2 I_\mathrm{b}. \tag{5}$$

Because the other factors are constant, maximizing $V_\mathrm{rec}^2 I_\mathrm{b}$ leads to the maximization of the input power. The same result is obtained if we maximize the square root of this value, which can be readily obtained using a differential pair in strong inversion.

The power estimation circuit is presented in Fig. 13. The output current I_out is the difference between the drain currents in the differential pair and is given by:

$$I_\mathrm{out} = I_\mathrm{D1} - I_\mathrm{D2} = \sqrt{2K}\sqrt{I_T}V_d, \tag{6}$$

in which $K = \frac{1}{2}\mu C_\mathrm{ox}\frac{W}{L}$, V_d is a fraction of V_rec, and I_T is proportional to I_b. The folded-cascode topology was chosen, because it allows for a high voltage drop across the differential pair, allowing it to operate in saturation over a large range of its bias current.

VI. Measurement Results

The setup presented in Fig. 14 is used in the measurements. The balun is used to generate the differential signal from a single-ended source. Then, an impedance matching PCB is used to emulate the antenna impedance, which is set to $40 + \mathrm{j}100\,\Omega$. This PCB has two traces for each phase of the input signal, each one containing one inductor ($20\,\mathrm{nH}$) and two tunable capacitors (1.5–$3\,\mathrm{pF}$ and 5.5–$30\,\mathrm{pF}$) in a T-match configuration. Each of the traces are tuned separately, using a Vector Network Analyzer (VNA) to verify the output impedance. The output of the impedance matching PCB is connected to the test PCB. A resistive load is connected to the rectifier output and a voltage source V_hp is used to set the impedance matching to either high-power or low-power mode. Fig. 14 also shows a magnified view of the impedance matching part on the test PCB, and its circuit schematic. The inductors L_S were added to compensate for variation in the impedance of the internal capacitors due to process variation and to compensate for additional parasitics of the PCB and discrete components. The value of inductor L_S is $6\,\mathrm{nH}$ (Coilcraft 0805HQ-6N2) and the value of inductor L_RF is $100\,\mathrm{nH}$ (Coilcraft 0805HP-101). The selected inductors have a 0805 footprint and quality factor around 80. The chip was fabricated in a standard $0.18\,\mu\mathrm{m}$ CMOS IC process. The full chip area is $1.05\,\mathrm{mm}^2$ and its active area is $0.2\,\mathrm{mm}^2$.

The power inductor employed in the DC-DC converter has an inductance of $100\,\mu\mathrm{H}$ (TDK MLF2012C101KT). Since this inductance is large, an inductor that presents a small DCR will have a large footprint and will not be suitable for most applications. We selected an inductor that has a larger-than-average DCR ($3.1\,\Omega$), but has a smaller volume than most commercially available inductors (about $3.6\,\mathrm{mm}^3$). The capacitors used in the test PCB are C_rec ($10\,\mathrm{nF}$), C_supply ($22\,\mathrm{nF}$), C_store ($22\,\mu\mathrm{F}$), and C_load ($4.7\,\mu\mathrm{F}$). Other components are resistors R_1 and R_2 (in the order of $\mathrm{M}\Omega$), for setting the target load voltage.

A VNA is used to measure the impedance matching PCB and to assist in tuning its output impedance. With the S-parameter results for the impedance matching PCB we are able to calculate its insertion loss, which is $2.66\,\mathrm{dB}$. The same is done for the balun, which presents a $1.31\,\mathrm{dB}$ insertion loss. The available power P_av is calculated by subtracting both losses from the signal generator power P_RF. The signal frequency is set to $403.5\,\mathrm{MHz}$ and P_RF is swept from -21 to $+19\,\mathrm{dBm}$. In this way, we do not consider the losses of the balun and impedance matching PCB in the measurement results, but we consider the impedance mismatch between the test PCB and the emulated antenna.

By switching V_hp from 0 to $1.8\,\mathrm{V}$, the impedance matching network is switched from the low power (LP) to the high power (HP) setting. Using a resistive load (R_load) at the rectifier output, the available power is swept and the output power is measured to plot the RF-DC PCE. Therefore, two curves are generated for a single R_load. By sweeping R_load and repeating this process for each of its values, the highest RF-DC PCE versus P_av curve is obtained, which is presented in Fig. 15. The MPPT circuit must switch V_hp around the point where the maximum PCE for the HP setting is equal to the maximum PCE for the LP setting. This point changes with process variations and the system can be calibrated by selecting which bit of the FC signal V_hp is connected to. Fig. 16 presents the RF-DC PCE variation as a function of frequency for two cases of P_av: $-21\,\mathrm{dBm}$ and $+10\,\mathrm{dBm}$.

The maximum RF-DC PCE is 58% at $-15\,\mathrm{dBm}$. However, both the DC-DC converter and MPPT introduce losses. Combining the RF-DC with the rest of the system produces the PCE results presented in Fig. 17. The output power provided to charge C_store is considered for the PCE calculation. The power losses for supplying the load are not taken into consideration in this figure, since they vary with the load current. The peak PCE

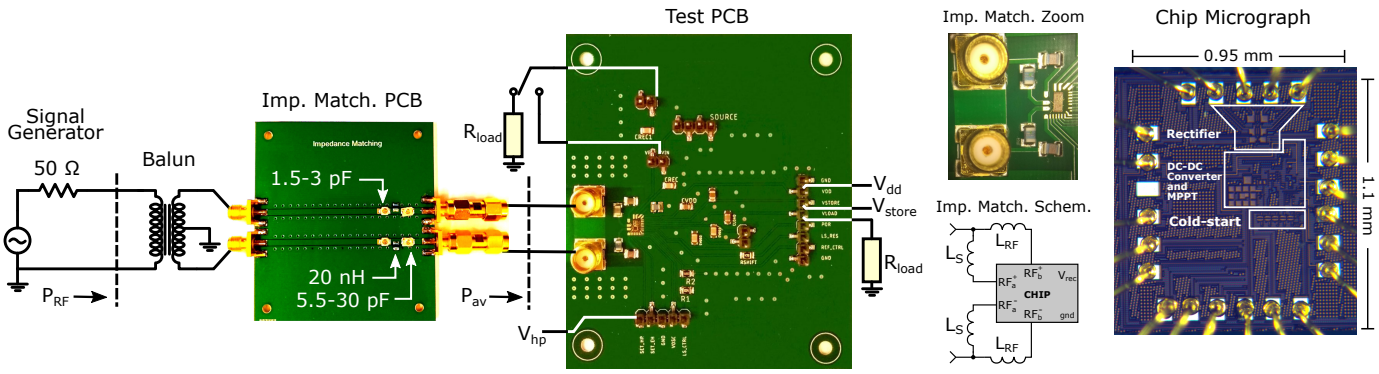

Fig. 14. Measurement setup and chip micrograph. The RF-DC measurement is done by placing the load at the rectifier output. The full system measurement is done by connecting the rectifier output to the DC-DC converter input.

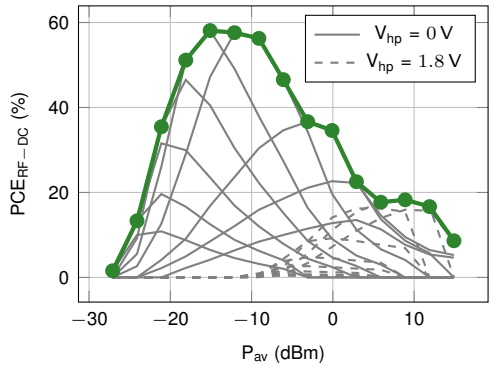

Fig. 15. The highest RF-DC PCE is shown by sweeping R_{load} from 400 kΩ down to 800 Ω and switching V_{hp} between 0 (LP setting) and 1.8 V (HP setting).

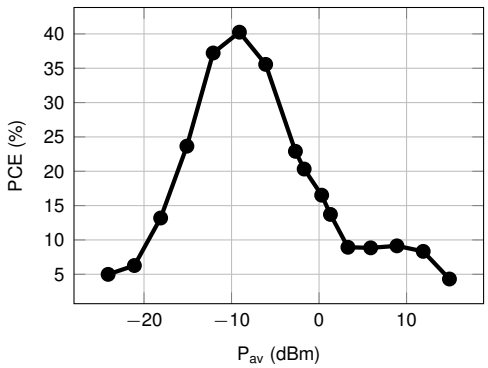

Fig. 17. RFEH power conversion efficiency at 1.8 V output voltage.

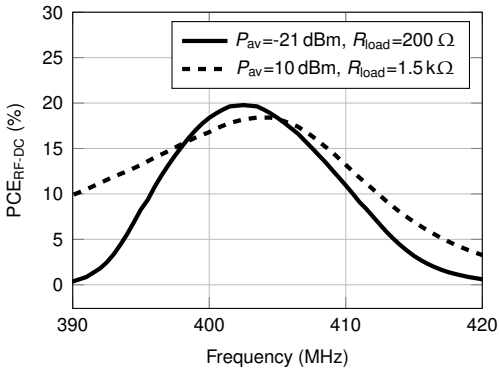

Fig. 16. Variation of the RF-DC PCE with frequency for $P_{\text{av}} = -21$ dBm and $P_{\text{av}} = 10$ dBm.

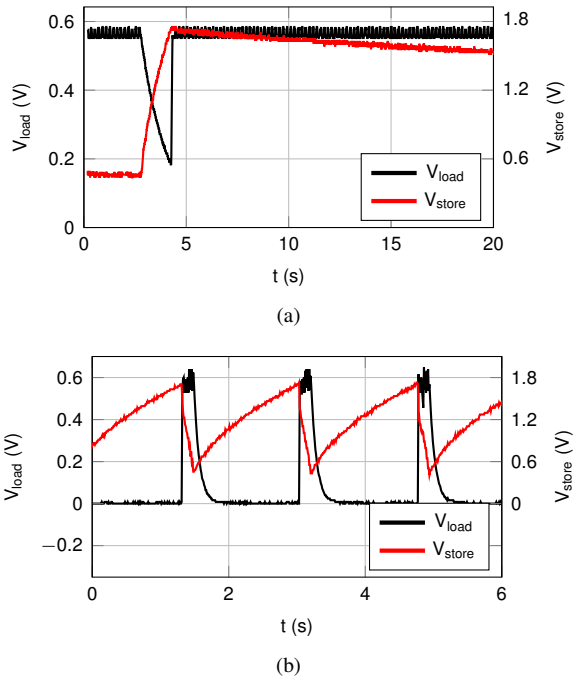

Fig. 18. Load voltage regulation for (a) high R_{load} (200 kΩ) and (b) low R_{load} (3 kΩ).

is 40.2% at $P_{\text{av}} = -9.1$ dBm. For P_{av} above +6 dBm, the impedance matching is switched to HP mode and the output power reaches 1.33 mW at +14.9 dBm (30.9 mW) input.

The load voltage regulation capability is presented in Fig. 18, which shows the transients of the storage capacitor voltage V_{store} and the load voltage V_{load} for different values of R_{load}. The target V_{load} is set at 0.6 V. Once V_{store} reaches 1.8 V, the system stops charging C_{store} and starts charging C_{load}. The system starts recharging C_{store} when V_{store} reaches 0.4 V. In practice, these voltage values change slightly due to

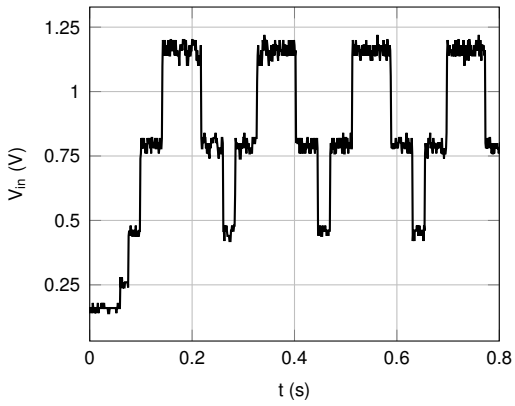

Fig. 19. DC-DC converter input voltage during MPPT operation.

offsets in the voltage reference and comparators. In Fig. 18(a), a high value of R_{load} is used. Once V_{store} reaches the predefined $1.8\,\mathrm{V}$, the system starts charging the load and the voltage V_{store} drops due to leakage. In this scenario, the system is on the edge of having enough power to operate. It cannot charge C_{store} at the same time as it charges the load, but it also does not require additional power from C_{store} to charge the load. Reducing R_{load} leads to the scenario presented in Fig. 18(b). Most of the power delivered to the load comes from C_{store} and the voltage across it drops rapidly to sustain the load voltage.

Fig. 19 shows the DC-DC converter input voltage and illustrates the MPPT functionality. In this scenario, the input power is maximized when the input voltage is approximately $0.8\,\mathrm{V}$. It can be observed that the input voltage moves back and forth around this value. As discussed in Sec. V, this behaviour shows the MPPT checking the power at the switching frequencies that are adjacent to the maximum power point one, which is characteristic of the Perturb and Observe algorithm.

Table I presents the comparison of this work with the state of the art. By using a single stage rectifier and a non-$50\,\Omega$ source, we have shown it is possible to obtain a high sensitivity, high input power range, and competitive peak PCE. Employing a DC-DC converter, we can obtain high output voltages at low available power levels. Moreover, the SIDITO topology allows for the independent control of the load voltage and of the input impedance, isolating the load from the energy harvester.

VII. Conclusions

We have presented the design and measurement of an RFEH and power management unit that operates from -24 to $+15\,\mathrm{dBm}$ of available input power. It is designed to receive power at a center frequency of $403.5\,\mathrm{MHz}$. The system employs adaptive techniques in the impedance matching network and DC-DC converter in order to increase the operating P_{av} range. An MPPT circuit is responsible for controlling the DC-DC converter switching frequency and impedance matching configuration to obtain maximum power transfer. Furthermore, the system employs a single inductor for harvesting (charging C_{store}) and load voltage regulation (charging C_{load}), while keeping its own internal supply (charging C_{supply}). The novel circuit techniques presented in this paper are: a low-power, compact input power estimation circuit, configurable power switches, and a high-speed low-power zero current detector. The peak energy harvesting efficiency is 40.2% at $P_{\mathrm{av}} = -9.1\,\mathrm{dBm}$ and the sensitivity is $-24\,\mathrm{dBm}$ while producing a $1.8\,\mathrm{V}$ output.

Acknowledgments

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TABLE I
COMPARISON TABLE

Reference	This Work	TCAS'19 [30]	JSSC'19 [31]	TCAS'15 [11]	JSSC'17 [32]	JSSC'14 [4]
Technology (nm)	180	130	180	180	180	90
Frequency (MHz)	403.5	900	915	900	900	868
Active Area (mm^2)	0.2	0.06	0.4	0.27	1.08	0.029
Additional System Requirements	External Inductors (100 μH Power Ind.)	Deep N-Well	Ext. Vdd + Loading Control	External Inductors (1 mH Power Ind.)	-	Ext. Micro-Controller
Sensitivity (dBm)	-24 (@ 1.8 V)	-18.7 (@ 1 V)	-17.8** (@ 1 V)	-17 (@ 2 V)	-14.8 (@ 1 V)	-27 (@ 1 V)
Reported Input Power Range (dB)	34 (PCE $>5\%$) 15 (PCE $>20\%$)	18* (PCE $>5\%$) 14.5 (PCE $>40\%$)	25* (PCE $>5\%$) 13 (PCE $>20\%$)	10* (PCE $>30\%$)	19.5* (PCE $>5\%$) 10* (PCE $>20\%$)	15* (PCE $>5\%$) 11* (PCE $>20\%$)
Peak PCE	40.2% (@ 1.8 V, -9.1 dBm)	80.3% (@ 1.1 V, -17 dBm)	34.4%** (@ $+1.3$ dBm)	44.1% (@ 2 V, -12 dBm)	25% (@ -5 dBm)	40% (@ -17 dBm)
System Architecture	CCDD Rectifier + DC-DC Conv.	Modified CCDD Rectifier	Reconfigurable Rectifier	CCDD Rectifier + DC-DC Conv.	Reconfig. Rect. + Load Regulation	CCDD Rectifier
Number of Rectifier Stages	1	3	2 – 12	1	1 – 8	5
DC-DC Converter Architecture	SIDITO Buck-Boost Conv.	-	-	Boost Converter	-	-
Load Regulation Capability	Yes	No	No	No	Yes	No

* Extracted from figures.
** Includes the antenna efficiency (93%).

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