Analysis and Design of a Passive Receiver Front-End Using an Inductive Antenna Impedance

Yao Liu and Wouter A. Serdijn, *Fellow, IEEE*

***Abstract*— This paper presents the analysis and design of a passive front-end (PFE) for low-power receivers. The freedom of the antenna impedance is observed and exploited to propose an inductive-antenna-based PFE. Analytical methods for the desired signal transfer and noise behavior of the proposed PFE are presented to offer insight into the proposed technique and facilitate the design. The analysis suggests that the inductive-antenna-based PFE offers higher voltage gain and lower noise figure than a standard 50 Ω-based PFE does, which is confirmed by simulations. The proposed PFE and a baseband band-pass amplifier are designed in 0.18-μm CMOS technology for the 402–405 MHz band of the IEEE 802.15.6 WBAN standard. Their combination exhibits a passive voltage gain of 11.6 dB, a NF of 14.7 dB, and an in-band IIP3 of 3.6 dBm, while dissipating 1.1 mW from a 1.2 V supply.**

***Index Terms*— Low power receiver, WBAN, WPAN, passive front-end, passive mixer, direct-conversion receiver, passive voltage gain, inductive antenna, band-pass amplifier, dc offset.**

I. Introduction

THE active RF front-end is usually one of the most power-hungry blocks in a low-power short-range receiver. A passive front-end (PFE) (or mixer-first front-end) avoids active low-noise amplifiers (LNAs) or low-noise transconductance amplifiers (LNTAs), and active mixers, and hence can potentially reduce the power consumption of the front-end. Although the PFE features high linearity, flexible frequency programability and baseband impedance upconversion [1]–[4], it suffers from a tight trade-off between power consumption and noise figure (NF). This is because the NF of a passive mixer is often improved by lowering the on-resistance of the switches or increasing the number of non-overlapping phases [5], which are both directly paid by a larger power consumption of the local oscillator (LO) buffers. This tight trade-off might not always be affordable for a low-power short-range receiver with a power budget of only a few milliwatts or even below one milliwatt. A passive amplification network such as a step-up transformer [6], [7] or an LC resonant matching network [8] prior to the passive mixer can effectively relax the power-NF trade-off.

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Y. Liu was with the Section Bioelectronics, Delft University of Technology, 2628CD Delft, The Netherlands. He is now with imec, 3000 Leuven, Belgium (e-mail: yaoliuhust@gmail.com).

W. A. Serdijn is with the Section Bioelectronics, Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, 2628CD Delft, The Netherlands (e-mail: serdijn@ieee.org).

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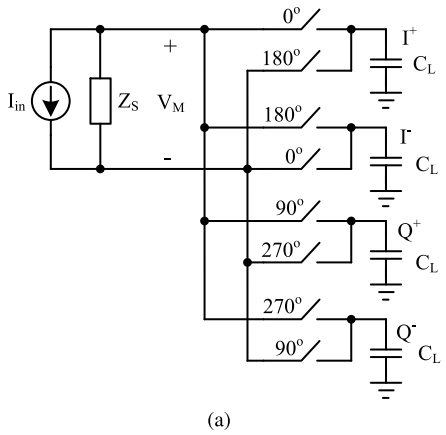
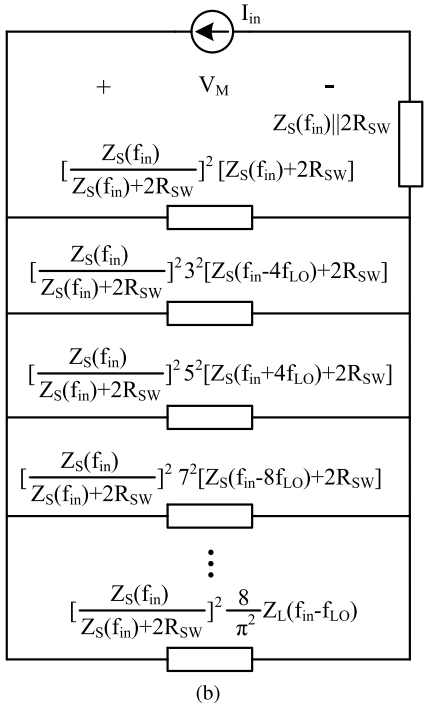
The passive network is often designed under the constraint of a 50 Ω antenna impedance, or even 50 Ω impedance matching. However, it is important to note that 50 Ω is only a traditional value originally meant to give a reasonable compromise between loss and power-handling capability for a coaxial cable with an air dielectric [9]. Also, if the length L between the antenna and the passive network is electrically short (L $< \lambda/10$, λ being the wavelength), the propagation effect in the interface can be neglected as the voltage and current can be considered constant along the connection [10], and hence there is no fundamental reason to use a transmission line in the interface. This, for example, may be the case for integrated circuits (ICs) with on-chip antennas [11] and ICs that are close enough to an off-chip antenna [12]–[14], especially at low frequencies (e.g., λ is as large as 300 mm at 1 GHz in the air). For the electrically-short interface, if the maximum power delivery is not the objective of interest, the impedance matching is no longer necessary [15]. Thus, the freedom of antenna impedance can be fully exercised to optimize the performance parameters of interest for a given application, rather than simply complying with the comfortable 50 Ω standard. An inductive antenna together with a resonant interface proves beneficial for increasing passive voltage gain of an RF energy harvester and an active LNA [12], [15], [16]. This paper incorporates an inductive antenna impedance in a PFE to obtain the same voltage-boosting effect. A 25% duty cycle (as opposed to 50%) quadrature passive mixer is used in the PFE due to its superior voltage gain, NF and linearity [17].

Owing to the time-variant and bidirectional nature of a passive mixer, interfacing an inductive antenna impedance and a passive mixer proves critical and challenging. Moreover, the frequency-dependent impedances preceding the mixer complicate the analysis of voltage gain and noise of the entire front-end. This paper proposes an interfacing technique to improve the passive voltage gain as well as NF of the front-end. Also, the voltage gain and noise behavior of the proposed topology are well analyzed to facilitate the design. The analysis of this paper starts quantitatively with a few assumptions, then qualitatively addresses several important effects. This is the approach that an analog designer might be most familiar with, and it also gives a good compromise between analysis complexity and the validity of outcomes.

This paper is organized as follows. Section II addresses the design challenges of a PFE using an inductive antenna, followed by the proposed PFE as well as the analysis of its voltage gain and noise behavior. The circuit implementation of the proposed front-end and a band-pass baseband amplifier



(a)



(b)

Fig. 1. (a) A 25% duty cycle quadrature passive mixer and (b) its equivalent model in the vicinity of switching frequency f_{LO} [6].

is described in Section III. Measurement results are presented and compared to prior art in Section IV.

II. Proposed Passive Front-End

A 25% duty cycle quadrature passive mixer with an arbitrary source impedance, as shown in Fig. 1(a), can be modeled by the circuitry in Fig. 1(b) in the vicinity of switching frequency f_{LO} [6]. I_{in} and Z_S represent the Norton equivalent of the source. C_L is the baseband capacitor, Z_L is its impedance, R_{SW} is the on-resistance of the switches, and f_{in} is the input RF frequency. This model is utilized to develop analytical methods for our proposed PFE in this section and subsequent sections.

Given an inductive antenna impedance, the simplest approach to extract the maximum voltage is loading the antenna with a resonating capacitance, which usually consists of the intrinsic capacitive input impedance of most circuits (e.g., an energy harvester or an LNA) and an extra

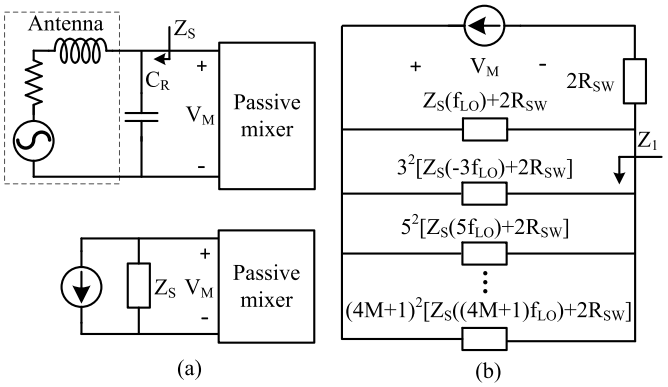


Fig. 2. (a) A front-end consisting of a passive amplification network and a subsequent passive mixer (b) Equivalent circuit of the front-end at f_{LO}.

capacitor [12], [16]. Considering a quadrature passive mixer as the load of the inductive antenna in Fig. 2(a), owing to its bidirectional and time-variant nature, the mixer presents input properties rather different from most linear time-invariant circuits, thereby significantly degrading the voltage gain at the interface. This can be explained with the aid of the model in Fig. 1(b) as follows. First, the complexity of the mixer input impedance demands a few assumptions and conditions before more insight can be given: (1) The inductive antenna is resonant with a capacitor C_R at f_{LO}, and hence $Z_S(f_{LO})$ is a relatively high impedance. (2) If we assume $R_{SW} \ll Z_S(f_{LO})$, then $(1 + 2R_{SW}/Z_S(f_{LO})) = 1$ and $Z_S(f_{in})\|2R_{SW} = 2R_{SW}$. (3) Baseband capacitor C_L presents an infinite impedance at DC. After transforming the Thevenin equivalent into its Norton counterpart as illustrated in Fig. 2(a), a simplified model can be given, as shown in Fig. 2(b). Z_1 is the parallel combination of $(4M+1)^2[Z_S((4M+1)f_{LO})+2R_{SW}]$ $(M \neq 0)$, where $4M+1$ is the harmonic index. In order to maximize the input voltage of the mixer V_M, Z_1 must be sufficiently greater than $Z_S(f_{LO})$. While the bandpass-shaping $Z_S(f)$ presents a large value at f_{LO}, the impedance decreases rapidly as the frequency moves away from f_{LO} (i.e., as $|M|$ increases). $Z_S((4M+1)f_{LO})+2R_{SW}$ is therefore dominated by the $2R_{SW}$ for large value of $|M|$. Thus, the overall effect of the parallel impedances results in a rather low quality factor complex Z_1, thereby considerably reducing the voltage gain at the interface.

The proposed PFE is shown in Fig. 3(a). A series inductance is inserted between the inductive antenna and the mixer to boost the source impedance at harmonics of f_{LO}, thereby presenting a large impedance at the mixer input and maintaining the voltage-boosting effect offered by the antenna and C_R. To explain this more quantitatively, the voltage gain from the antenna to the baseband output of the mixer is analyzed in this section. Furthermore, the noise behavior of the proposed PFE is also analyzed, revealing an improved NF.

A. Voltage Gain

We first make the following assumptions:

1) The inductive antenna impedance is resonant with C_R at f_{LO}, their impedances at f_{LO} are R_A+jX_A and $-jX_A$, respectively. The quality factor of the antenna is $Q_A=X_A/R_A$.

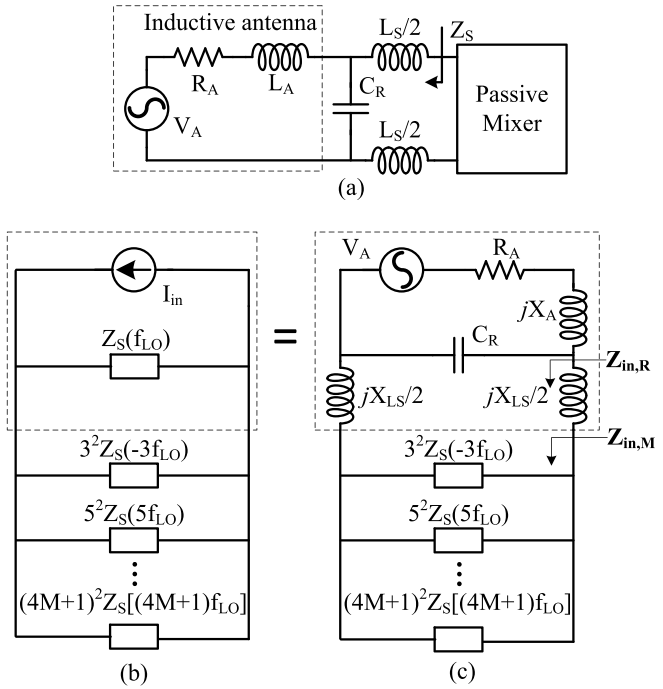


Fig. 3. (a) Proposed PFE, (b) its equivalent model at $f_{LO}$with a Norton source, and (c) a physical source.

2) R_{SW} is assumed to be zero for now, so $(1 + 2R_{SW}/Z_S(f_{LO})) = 1$ and $Z_S(f_{in})\|2R_{SW} = 0$. Also, the voltage gain from the mixer input to the differential baseband output is $\sqrt{2}\pi/4$ due to the absence of the on-resistance [6]. Thus, the analysis of the voltage gain from the antenna to the baseband boils down to that of the voltage amplification at the mixer input, which is determined by the input impedance of the mixer near f_{LO}.
3) We focus on the voltage gain of the zero-IF product. f_{in} is therefore assumed to be equal to f_{LO}.
4) Baseband capacitor C_L presents an infinite impedance at DC.

Under these assumptions, the model in Fig. 1(b) can be simplified into the one shown in Fig. 3(b). Furthermore, I_{in} and $Z_S(f_{LO})$ are transformed back into their physical model to facilitate analysis, as shown in Fig 3(c). The source impedance at f_{LO} and its harmonics can be expressed as:

$$Z_S(Nf_{LO}) = (\frac{X_A}{Q_A} + jNX_A)||(-j\frac{X_A}{N}) + jNX_{LS}, \quad (1)$$

where N is the harmonics index, and X_{LS} is the impedance magnitude of L_S at f_{LO}. The impedance of this R_A-L_A-C_R resonant network becomes dominated by C_R as |N| increases, thus the first term in (1) can be approximated as $-jX_A/N$ for |N| greater or equal to 3. This also suggests that Q_A has little impact on $Z_S(Nf_{LO})$ for |N| greater or equal to 3. Furthermore, we can define the input impedance of the mixer at f_{LO} as:

$$Z_{in,M} = \frac{1}{\sum_{M=-\infty}^{\infty} \frac{1}{(4M+1)^2 Z_S[(4M+1)f_{LO}]}}, \quad (M \neq 0), \quad (2)$$

which is a parallel combination of impedances, as shown in Fig. 3(c). Note that the harmonics index N in (1) is now replaced by 4M+1. $Z_{in,R}$ is the series combination of $Z_{in,M}$ and jX_{LS}. For large values of |4M+1|, impedance term $(4M+1)^2Z_S[(4M+1)f_{LO}]$ can be approximated as:

$$(4M+1)^2 Z_S[(4M+1)f_{LO}] \approx -j(4M+1)X_A + j(4M+1)^3 X_{LS}, \quad (3)$$

which increases approximately proportionally to $(4M+1)^3$. In contrast, in the absence of L_S, (3) is only proportional to (4M+1). More importantly, with R_{SW} taken into account, (3) can be rewritten as:

$$(4M+1)^2 Z_S[(4M+1)f_{LO}] \approx -j(4M+1)X_A + (4M+1)^2 2R_{SW}, \quad (4)$$

indicating that the impedance becomes resistive as |4M+1| increases. Consequently, the total effect presented by the mixer is a low quality factor impedance. The above observation exhibits the main benefit of L_S, i.e., boosting the source impedance at f_{L0} harmonics and hence increasing the mixer input impedance at f_{LO}.

$Z_{in,M}$ can be approximated by a few impedance terms for small values of |4M+1|. We use only the terms of M=−1 and 1 to approximate the input impedance for developing insight, then more terms will be taken into account to provide more precise results. We thus have:

$$Z_{in,M} \approx 3^2 Z_S(-3f_{LO})||5^2 Z_S(5f_{LO}) = -j11.43X_A\frac{(1-8\alpha)(26\alpha-1)}{1-69\alpha}, \quad (5)$$

where $\alpha = X_{LS}/X_A$ is also the inductance ratio of L_S and L_A. We make the following observations here:

1) With improper values of X_A and X_{LS}, one of the parallel impedances in Fig. 3(c) could be zero (or very small). To avoid this, $3^2Z_S(-3f_{LO})$ should be capacitive, i.e., $X_{LS} > 0.125X_A$. In such a condition, terms $3^2Z_S(-3f_{LO})$, $7^2Z_S(-7f_{LO})$... are all capacitive with their magnitudes increasing with harmonic index |4M+1|, while terms $5^2Z_S(5f_{LO})$, $9^2Z_S(9f_{LO})$... are all inductive with their magnitudes increasing with |4M+1|, and the total impedance $Z_{in,M}$ is capacitive.
2) $Z_{in,M}$ increases proportionally to α as indicated by (5). This can be further illustrated by the precisely calculated relationship shown in Fig. 4, with all of the parallel impedances shown in Fig. 3(c) taken into account. Also, due to the high quality nature of the source impedance, the mixer input impedance is mainly capacitive. The approximated $Z_{in,M}$ and $Z_{in,R}$ using Equation (5) are plotted together with the precisely-calculated counterparts in Fig. 3(c), suggesting a good approximation accuracy of Equation (5).

As the combined capacitive impedance of C_R and $Z_{in,R}$ must be resonant with L_A, the question arises how the total desired capacitive impedance should be partitioned between $Z_{in,R}$ and the impedance of C_R, i.e., $Z_{CR} = -jX_{CR}$. Since $Z_{in,R}$ is strongly dependent on the value of L_S, it is desirable to make $Z_{in,R}$ dominate the total impedance, thereby fully utilizing the effect

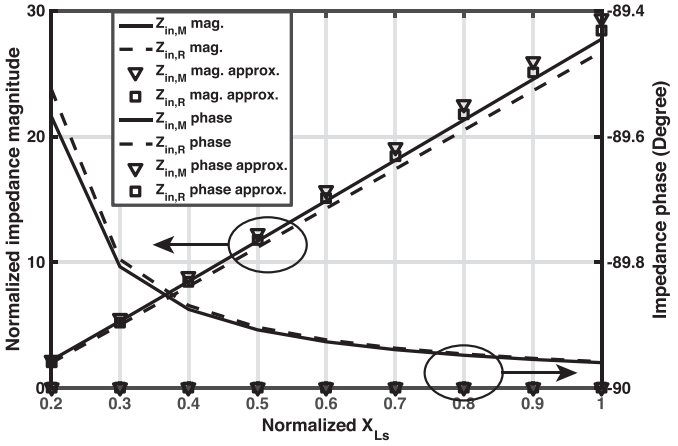


Fig. 4. Precisely-calculated (Equation (2)) and approximated (Equation (5)) $Z_{in,M}$, as well as $Z_{in,R}$, as a function of X_{LS}, with all the magnitudes normalized to X_A. These results are approximately the same for different values of quality factor Q_A though $Q_A = 10$ ($R_A = 10\ \Omega$, $X_A = 100\ \Omega$) has been taken as an example. This is because $Z_S(Nf_{LO})$ has little dependence on Q_A as addressed by Eq. (1), and hence so do $Z_{in,M}$ and $Z_{in,R}$.

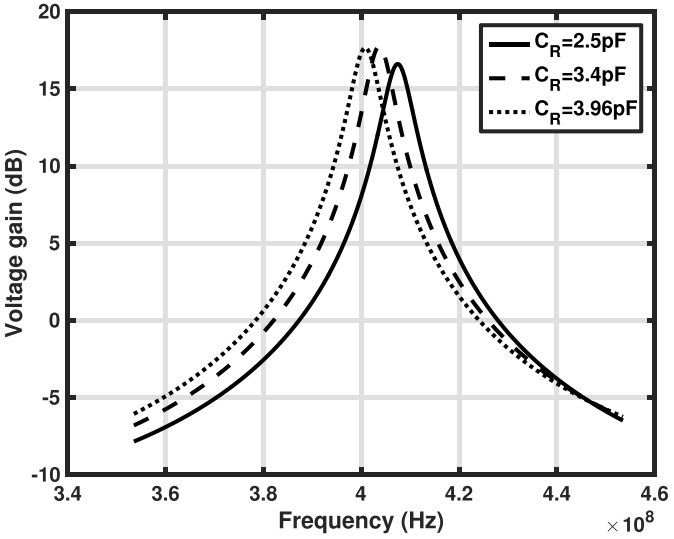


Fig. 5. Voltage transfer function from the antenna source to the mixer input (voltage gain) in the vicinity of f_{LO}. Resonant frequency offset can be compensated for by tuning C_R. We assume the following simulation settings hereafter unless otherwise noted: $R_A = 10\ \Omega$, $X_A = 100\ \Omega$ ($L_A = 39.6$ nH), $X_{LS} = 0.5\ X_A$, $C_R = 3.4$ pF, $C_L = 50$ pF, $f_{LO} = 403.5$ MHz with ideal non-overlapping 25% duty-cycle quadrature signals, and the switch can switch instantaneously between on and off states with a on-resistance of $R_{SW} = 10\ \Omega$.

of L_S. However, the following example shows that the strong dependence of $Z_{in,M}$ upon Z_S renders this infeasible. Suppose X_{CR} is much greater than X_A, e.g., $X_{CR} = 10X_A$, and $L_S = 0.2L_A$. We repeat (1) and (5), resulting in the following impedances:

$$\begin{aligned} Z_{in,R} &\approx 3^2 Z_S(-3f_{LO})||5^2 Z_S(5f_{LO}) + j0.2X_A \\ &= -X_A(3.5 - 48.2j), \end{aligned} \tag{6}$$

$$Z_{CR}||Z_{in,R} = (0.1 - 8.4j)X_A. \tag{7}$$

(6) suggests that $Z_{in,R}$ is a complex high impedance (magnitude is around 5 times X_{CR}), rather than a purely capacitive low impedance (magnitude is much smaller than X_{CR}) as we wished. $Z_{CR}\|Z_{in,R}$ is therefore dominated by X_{CR} as shown by (7), yielding an impedance much higher than the required value of $-jX_A$ for resonance at f_{LO}.

The above example suggests that $-jX_{CR}$ should be chosen around the desired resonance impedance $-jX_A$, and L_S should be sufficient to make $Z_{in,R}$ much greater than $-jX_{CR}$. A practical method to determine the components value is as follows. (1) Choose a sufficient L_S value according to Fig. 4. For example, L_S=0.5L_A offers a $|Z_{in,R}|$ of 11.2X_A. (2) Reduce C_R to compensate for the resonance frequency shift, as illustrated by Fig. 5.

Having developed a good understanding of the mixer's impedance at the switching frequency, we now formulate the voltage conversion gain. $Z_{CR}\|Z_{in,R}$ should be designed to resonate with the antenna impedance R_A+jX_A, as discussed above. Since $Z_{CR}\|Z_{in,R}$ is a capacitive load with a negligible real part if R_{SW} is assumed to be zero, the resonant voltage across C_R is:

$$V_R = Q_A V_A. \tag{8}$$

Considering the impedance ratio of jX_{LS} and $Z_{in,M}$, we get the voltage at the mixer's input:

$$V_{in,M} = \frac{Z_{in,M}}{Z_{in,M} + jX_{LS}} V_R. \tag{9}$$

As indicated by Fig. 4, $Z_{in,M}$ is much greater than jX_{LS}, i.e., the ratio $Z_{in,M}/(Z_{in,M}+jX_{LS})$ only varies from 1.1 to 1.04 if α varies from 0.2 to 1. So the voltage drop across L_S is negligible. The voltage gain from mixer input to mixer output V_{OUT} is $\sqrt{2}\pi/4$, assuming Rsw=0 [6], and hence the conversion gain from V_A to V_{OUT} is:

$$G = \frac{V_{OUT}}{V_A} = Q_A \frac{\sqrt{2}\pi}{4}. \tag{10}$$

Although voltage is a more familiar quantity, the input of an antenna is actually a power quantity. The antenna input power can be transformed into a Thevenin equivalent voltage as [12]:

$$V_A = \sqrt{8 R_A P_{av}}, \tag{11}$$

where P_{av} is the available power of the antenna. Substituting (11) into (10) and expressing Q_A as X_A/R_A, we get the mixer's output voltage as a function of the input power:

$$V_{OUT} = \sqrt{8P_{av}} \frac{X_A}{\sqrt{R_A}} \frac{\sqrt{2}\pi}{4}. \tag{12}$$

The effect of R_A on V_{OUT} is a point of interest. For a given power P_{av}, although reducing R_A decreases V_A, Q_A is increased to a greater extent, thereby increasing V_{OUT}. It is also instructive to contrast (12) with the same quantity of a PFE with the same passive mixer but with a standard 50 Ω antenna impedance (50 Ω-based counterpart). Assuming $R_{SW} = 0$, the voltage at the input of the mixer can be calculated with the aid of the model shown in Fig. 1(b), yielding $V_{in,M} = 8V_A/\pi^2$. Incorporating a voltage gain of $\sqrt{2}\pi/4$ from the input of the mixer to its output and (11), the output voltage is:

$$V_{OUT} = \sqrt{8 \cdot 50 P_{av}} \frac{2\sqrt{2}}{\pi}. \tag{13}$$

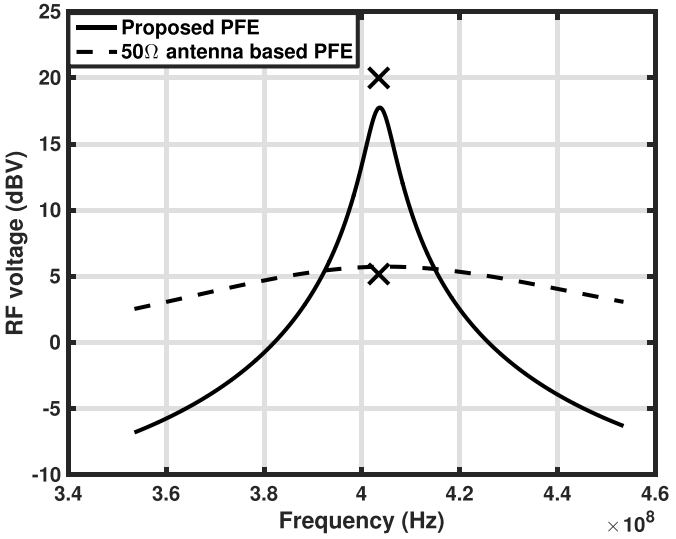


Fig. 6. RF voltage at the mixer input of the proposed PFE and its 50 Ω-based counterpart for a given antenna available power, P_{av} = 10.98 dBm. The approximated RF voltages using Equation (12) and (13) (excluding the conversion gain of $\sqrt{2}\pi/4$ from the switch input to switch output for both) are marked by "X".

The contrast between (12) and (13) summarizes the benefits of the proposed PFE: (1) using an inductive antenna impedance, two extra degrees of freedom, i.e., R_A and X_A are introduced to increase V_{OUT} for a given antenna available power; (2) the intermediate inductance L_S increases the input impedance of the mixer considerably, thereby well maintaining the passive voltage gain offered by the passive network, i.e., Q_A. Considering a PFE with an antenna impedance of (10+j100) Ω, $L_S = 0.5L_A$ and $R_{SW} = 10$ Ω, Fig. 6 demonstrates that the PFE offers 12 dB higher peak RF voltage than its 50 Ω-based counterpart does for the same antenna available power. Note that the simulated 12 dB is smaller than the 14.8 dB difference between the calculated RF voltages using Equation (12) and (13) (excluding the conversion gain of $\sqrt{2}\pi/4$ from the switch input to switch output for both), which are marked as "X" in Fig. 6. This discrepancy primarily arises from the presence of the 10 Ω switch resistance. We elaborate on the effect of the switch resistance in the following section.

B. Effects of Switch On-Resistance

If R_{SW} is assumed to be zero, $Z_{in,M}$ is almost capacitive with a very high quality factor as shown by Fig. 4. The presence of the on-resistance gives rise to the addition of a resistive part to each of the parallel impedances shown in Fig. 3(c) and Equation (2), thereby reducing the quality factor of $Z_{in,M}$. Consequently, the RF voltage gain offered by the passive network is reduced due to the limited quality factor of $Z_{in,M}$. Considering $R_A = 10$ Ω, $L_A = 39.6$ nH ($X_A = 100$ Ω), $L_S = 0.5L_A$ and $C_R = 3.4$ pF (to resonate at 403.5 MHz as indicated by Fig. 5), the calculated $Z_{in,M}$ using Equation (2) and the resulting $Z_{in,R}$ and $Z_{in,R}\|Z_{CR}$ are shown in Table I for several R_{SW} values. The quality factor of the resonance impedance $Z_{in,R}\|Z_{CR}$ decreases with increasing R_{SW}, thereby reducing the passive voltage gain, as shown by the simulation results depicted in Fig. 7. Note that, as R_{SW} increases, the discrepancy between the simulated gain and calculated gain shown in Fig. 7

TABLE I
CALCULATED $Z_{IN,M}$, $Z_{IN,R}$ AND $Z_{IN,R}\|Z_{CR}$ AT LO FREQUENCY AS A FUNCTION OF R_{SW}

R_{SW} (Ω)	10	20	40
$Z_{in,M}(\Omega)$	303-j1027	559-j905	909-j590
$Z_{in,R}(\Omega)$	303-j976	559-j854	909-j539
$Z_{in,R}\|Z_{CR}(\Omega)$	3-j105	6-j106	10-j109

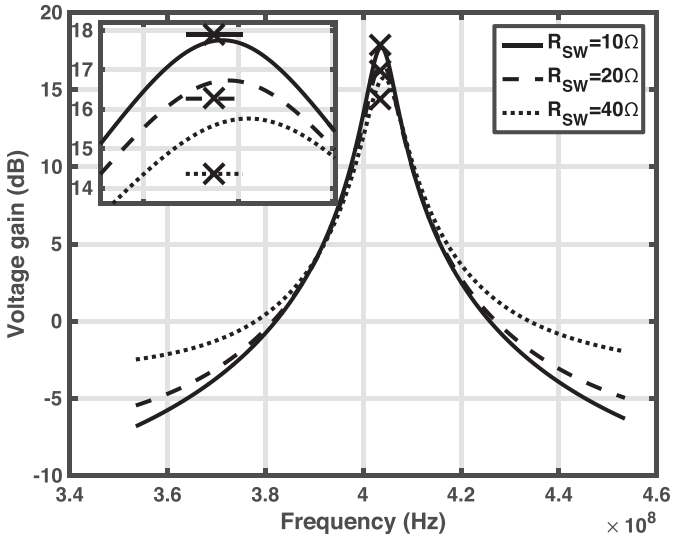


Fig. 7. The effect of R_{SW} on the peak voltage gain of the proposed PFE. The calculated peak gains using the model shown in Fig. 3(c) and the impedances in Table I are marked by "X" and the corresponding line styles.

increases, suggesting the model of Fig. 3(c) becomes less accurate. This is because, the source models (dashed blocks) in Fig. 3(b) and (c) ignore the impedance term $Z_S(f_{in})\|2R_{SW}$ (of the original model shown in Fig. 1(b)) due to the assumption of $R_{SW} = 0$ Ω, and this impedance term becomes more pronounced as R_{SW} increases, thereby causing the discrepancy. Nevertheless, the model shown in Fig. 3(c) incorporates the physical model of the passive network and hence is easier than the mathematical model (shown in Fig. 1(b)) to develop design insight.

This impact of R_{SW} can be compensated for by increasing the quality factor of each parallel element in Fig. 3(c), i.e., increasing L_S. The conversion gain from the input of the mixer to its output is also reduced because of the voltage drop over the switch [6]. However, this effect is negligible for the proposed front-end since Z_S and $Z_{in,M}$ are much greater than R_{SW} in a proper design.

C. Bandwidth

For the same R_{SW} and load capacitance C_L, the proposed front-end presents a narrower bandwidth with respect to its counterpart based on a 50 Ω antenna impedance. We consider the model in Fig. 1(b) for comparing the two topologies. For frequencies further away from f_{LO}, all of the parallel terms $(4M+1)^2[Z_S(f_{in}+4Mf_{LO})+2R_{SW}]$ can be omitted because $Z_L(f_{in}-f_{LO})$ dominates. We also assume $2R_{SW} \ll Z_S(f_{in})$. Thus, in order to compare the input voltage of the mixer in the two topologies, we now only need to compare the equivalent Norton source $I_{in}(f)$. While $I_{in}(f)$ is independent of frequency for the case of a 50 Ω antenna, $I_{in}(f)$ of the

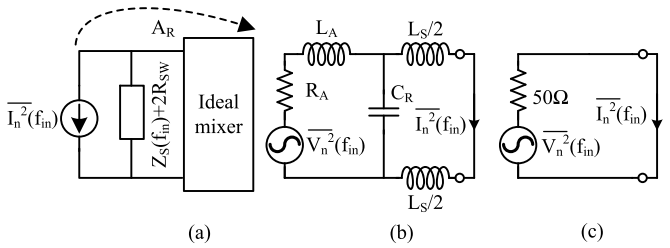


Fig. 8. (a) Representing the input noise and switch noise as a Norton equivalent. (b) Circuitry for finding the Norton noise current source $\overline{I_n^2}(f_{in})$ of the proposed PFE, and (c) its 50 Ω-based counterpart.

proposed topology experiences a third-order (L_A, C_R and L_S) filtering when the physical model in Fig. 3(a) is transformed into its Norton counterpart. The proposed topology therefore offers more suppression at frequencies further away from f_{LO} than the 50 Ω-based counterpart does. In other words, apart from the upconverted filtering effect of C_L, the bandwidth of the proposed topology is also narrowed by the passive network. The difference addressed above is also illustrated by the simulation results shown in Fig 6.

D. Noise Analysis

Noise folding is the main noise degradation mechanism for a passive mixer. The proposed PFE presents interesting reduction of the noise folding effect. We analyze the noise behavior of the proposed PFE with respect to a 50 Ω based PFE. The improvement is demonstrated using a simple and qualitative approach, avoiding exhaustive analysis.

We consider the model shown in Fig. 8(a) for noise analysis. The input noise source and the source impedance are represented in the form of a Norton equivalent, and the switch resistance is merged with the source impedance. For an input noise current around f_{LO}, assume its transimpedance gain to baseband output is A_R. We also have that the noise around the Nth harmonic of f_{LO} (N is an odd integer) folds down with a gain related to A_R, i.e., A_R/N [6], [8]. The relative contribution of the noise folding effect (i.e., NF) can be analyzed by finding the Norton equivalent noise current $\overline{I_n^2}(f_{in})$ around the Nth harmonic of f_{LO}. We use the circuitry in Fig. 8(b) and (c) to do so for the proposed topology and its 50 Ω-based counterpart, respectively. Let's consider a noise voltage source around the Nth harmonic of f_{LO} ($|N|>1$), $\overline{V_n^2}(f_{in})$. The short-circuit noise current and hence the value of the Norton noise current source $\overline{I_n^2}(f_{in})$ in Fig. 8(c) is simply $\overline{V_n^2}(f_{in})/50^2$. In contrast, the R_A-L_A-C_R-L_S network in Fig. 8 (b) provides third-order filtering, and L_S has a high impedance, so $\overline{I_n^2}(f_{in})$ in Fig. 8 (b) is less than the one found in (c), and more importantly decreases with N. Thus, the proposed PFE significantly reduces the noise folding with respect to its 50 Ω-based counterpart, as further evidenced by the simulation results in Fig. 9.

The above noise analysis technique applies to switch thermal noise as well, as illustrated in Fig. 10. $\overline{I_n^2}(f_{in})$ in Fig. 10(b) is a frequency independent current which is determined by the ratio between R_{SW} and 50 Ω. In contrast, since the source impedance in Fig. 10(a) increases with frequency, and is much greater than 50 Ω, $\overline{I_n^2}(f_{in})$ in Fig. 10(a) is much

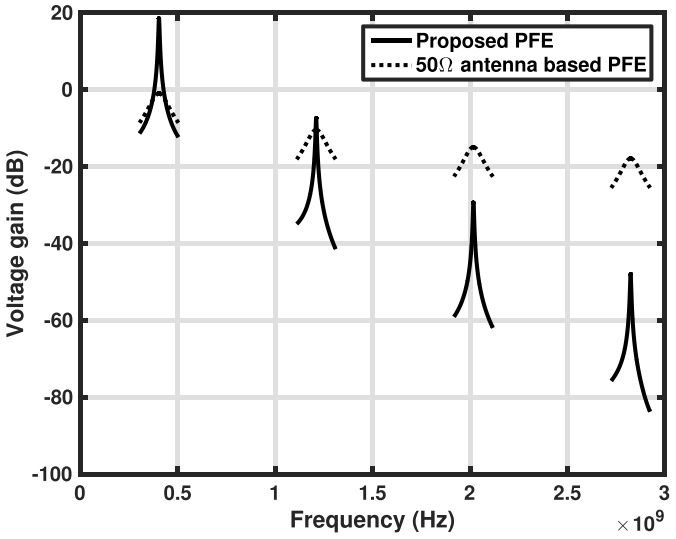


Fig. 9. Desired signal transfer from f_{LO} to baseband and unwanted foldings from $3f_{LO}$, $5f_{LO}$ and $7f_{LO}$ to baseband for the proposed PFE and its 50 Ω-based counterpart.

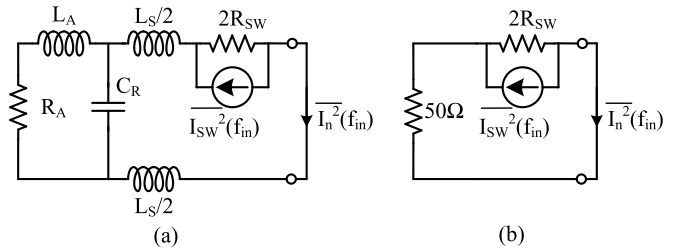


Fig. 10. Circuitry for finding the Norton noise current source $\overline{I_n^2}(f_{in})$ of the switch thermal noise for (a) the proposed PFE, and (b) its 50 Ω-based counterpart.

less than that in Fig. 10(b) and decreases with frequency. Hence, the thermal noise of the switch resistance can also be significantly suppressed by the proposed network in front of the mixer. This allows us to use small size switches to reduce the driving power of clock signals while retaining sufficient NF. The NF comparison of the two topologies is depicted in Fig. 11. Due to the reduction of noise folding, the proposed topology improves NF significantly (around 4.2 dB in the example of Fig. 11).

Although flicker noise contributes much less than thermal noise does in both PFEs, as shown in Fig 11, it appears that the flicker noise behavior of the proposed PFE is more pronounced than that of its 50 Ω-based counterpart. This can be understood with the aid of two popular explanations for the flicker noise mechanism of a passive mixer [18]–[20] as follows. The slowly varying gate-referred flicker noise randomly modulates the commutation instant which is ideally located at the zero crossings of the LO. This modulation results in a train of noise pulses which add to the ideal square-wave commutation waveform, and as a consequence, flicker noise appears at the output [18], [19]. Thus, the output flicker noise is proportional to the amount of input RF current to the passive mixer. As described in Section II-A, for the same output capacitance, the proposed PFE delivers more output voltage than its 50 Ω-based counterpart, indicating that the former also has larger noise current at the input of the switches than

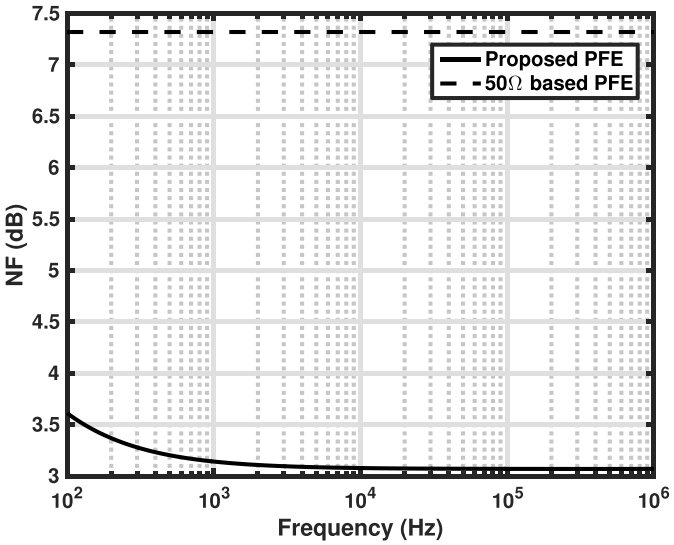


Fig. 11. NF comparison of the proposed PFE and a 50 Ω-based PFE. The switch is implemented by a realistic MOSFET with a R_{SW} around 50 Ω. The driving clock is considered to be noiseless.

the latter, thus more output flicker noise. Another explanation of the flicker noise mechanism is presented in [20], where the current due to the capacitive coupling of the large LO voltage to the drain nodes of the switches is said to be responsible for transferring the switch flicker noise to the output. In the proposed PFE, owing to the high impedance presented by the passive network at the drain nodes of the switches, the large LO voltage produces considerable voltage fluctuations at the drain nodes. These voltage fluctuations give rise to a non-zero-mean current in the channel of the switch, and hence the flicker noise of the switch manifests itself at the output. This effect is much less pronounced in the 50 Ω-based counterpart because 50 Ω is a very small wideband impedance in comparison with the impedance of the proposed passive network. Since the flicker noise of the mixer does not dominate the noise performance of the proposed PFE, we rely on the above two qualitative explanations to develop insight in the design process, thereby avoiding exhaustive analysis.

III. Implementation

A direct-conversion receiver front-end is implemented to verify the results presented in the previous sections. The block diagram of the system is depicted in Fig. 12. An off-chip matching network transforms a standard 50 Ω source impedance into a desired inductive impedance to emulate an inductive antenna. This emulation is less accurate than a real inductive antenna, but it allows us to use standard 50 Ω-based equipment for measuring this proof-of-concept prototype. We elaborate on this point in the subsequent subsection. The passive network incorporates an extra C_R and L_S to offer high voltage gain to a differential quadrature 25% duty cycle passive mixer. The downconverted zero-IF signals are subsequently processed by a band-pass amplifier (BPA) to suppress DC offsets and to define the signal bandwidth. The prototype is designed for the 402-405 MHz frequency band of the IEEE 802.15.6 WBAN standard. Channel bandwidth is 300 kHz.

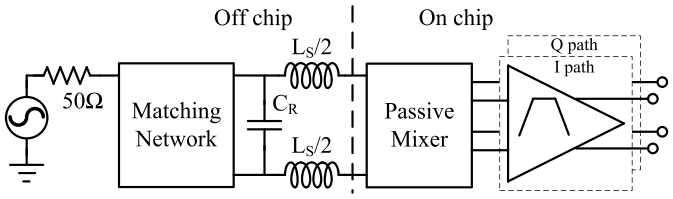


Fig. 12. System diagram of the proposed PFE and a BPA.

A. Passive Network

A well-designed inductive antenna can present a quality factor as high as 74.5 ((4.4+j328) Ω) at 868 MHz [12], offering a remarkable passive voltage gain. Moreover, parasitics (of PCB tracks, ESDs, transistors, etc) can be merged with the resonant capacitance of the antenna, thereby resulting in a very compact interface and hence avoiding passive voltage gain degradation. However, the verification process of an inductive antenna-based system turns out to be complex. For example, in [12], measurements needed to be performed in an anechoic chamber to relatively well control the signal level received by the antenna. For this reason, we use a matching network to emulate the desired antenna impedance in this prototype. Limited quality factors of the employed matching network components limit the possible passive voltage gain and introduce extra noise as well. We aim for a quality factor of 10 in this design.

The impedance transformation network consists of a narrowband 50 Ω/100 Ω balun, a 12 pF capacitor and two 33 nH high quality factor inductors, as shown in Fig. 13. In principle, the ratio of the balun is preferably 1:1 since the 50 Ω source resistance needs to be transformed to a lower value. But a ratio of 1:2 is chosen here due to the availability of the components. The 33 nH inductors have a high quality factor of 74 at 400 MHz. The transformed impedance Z_A is measured and plotted in Fig. 14, presenting (17.4+j171.7) Ω, i.e., a Q of around 10, at 403.5 MHz. L_S is chosen equal to around half of L_A, i.e., 30 nH, sufficiently increasing the input impedance of the mixer. The wideband property of L_S is also critical since it should maintain inductive behavior above f_{LO}, at least upto $3f_{LO}$ or $5f_{LO}$. The self-resonant frequency of the 15 nH inductors is 3.6 GHz, which is sufficiently high for $f_{LO} = 403.5$ MHz. Owing to the strong dependence of the mixer's input impedance upon C_R as addressed in Section II-A, an off-chip capacitance trimmer with a tuning range of 0.65-2.5 pF is used to find an optimal value for C_R during the measurement process.

ESD parasitic capacitances, as well as other off-chip and on-chip capacitances in front of the mixer input, denoted by C_{ESD}, prove problematic as they shunt the inductive source impedance, thereby degrading the desired impedance boosting effect. Utilizing the model shown in Fig. 3(c), the effect of C_{ESD} at f_{LO} can be modeled as a shunt capacitance of $\pi C_{ESD}/4$, as conceptually illustrated in Fig. 15. The impact of this capacitance can be further understood by a numerical example as follows. For $X_A = 171.7$ Ω and $L_S = 0.5L_A$, as a coarse approximation, the mixer input impedance $Z_{in,M}$ is equal to $-j11.2X_A = -j1.9$ kΩ as shown in Fig. 4. While $\pi C_{ESD}/4$ ($C_{ESD} = 218$ fF) presents an impedance of –j2.3 kΩ,

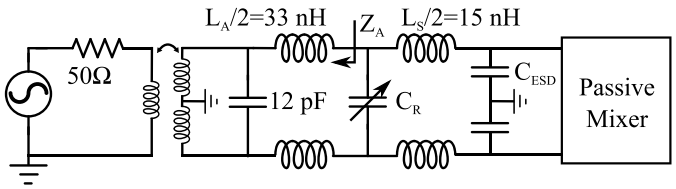


Fig. 13. Implementation of passive network.

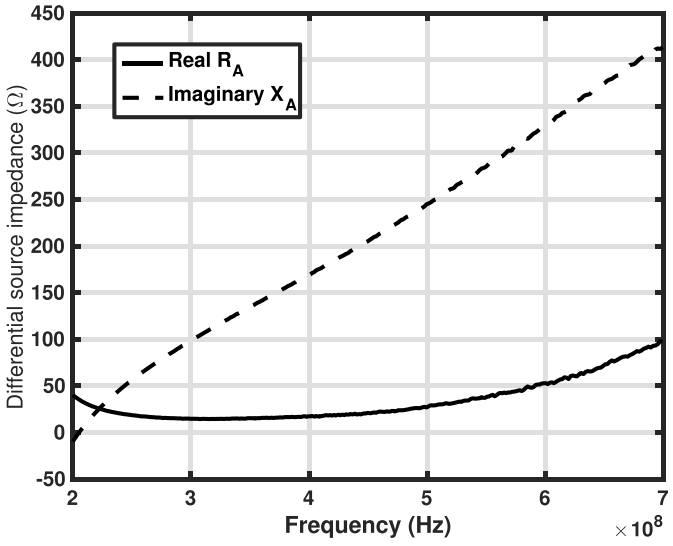


Fig. 14. Measured output impedance of the impedance transformation network.

the overall shunt impedance is degraded to –j1 kΩ, thereby halving the impedance boosted by L_S. This effect limits the improvement offered by L_S.

While several discrete components with large values are used for the sake of verification simplicity in this low frequency prototype, it's important to note that a fully integrated implementation is practical for higher frequencies if a real inductive antenna, e.g., the one reported by [12], is used. We elaborate on this point as follows. (1) For a real inductive antenna, the balun, the 12 pF capacitor and the 33 nH inductor shown in Fig. 13 can be omitted, and the antenna can be directly connected to a chip if L_S is implemented on-chip. Now C_{ESD} serves as a part of the desired resonant capacitance, rather than complicating the design. While the on-chip input capacitance of the mixer still causes the same impedance degradation effect, its value is much smaller than C_{ESD}. Consequently, the impedance boosting effect of L_S can be better maintained, and hence a lower L_S can be chosen for practical on-chip implementation. (2) Moving to higher frequency bands can also reduce the values of L_A and L_S for the same quality factor.

B. 25% Duty Cycle Quadrature Passive Mixer and Clock Generator

A double-balanced quadrature passive mixer driven by a 4-phase 25% duty cycle clock is implemented in 0.18 μm CMOS technology. The circuit diagram of the mixer is shown in Fig. 16(a). Deep N-well NMOS switches (W/L=12 um/0.18 um) are driven by a 1.2 V_{PP} clock, providing an on-resistance R_{SW} of 50 Ω. R_{SW} appears rather

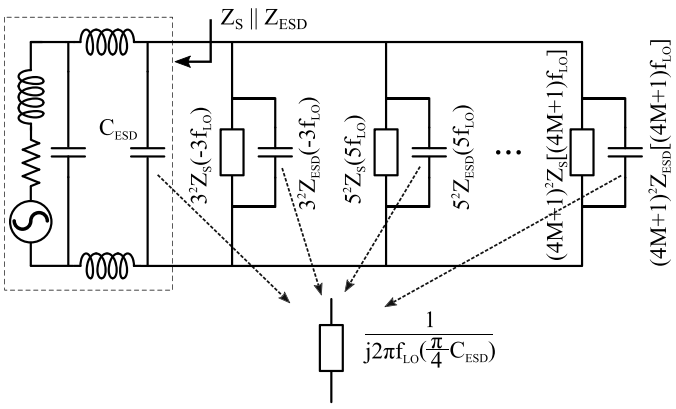


Fig. 15. The impact of C_{ESD} can be modeled as a capacitance of $\pi C_{ESD}/4$ around f_{LO}.

big from a noise perspective but its noise folding effect can be significantly suppressed by the proposed passive network, and hence still meeting the system requirement. Consequently, the power consumption of the clock buffers can be reduced by the small size of the switches. Of course, a relatively big R_{SW} may compromise the mixer's linearity, but it proves to be not a severe issue for this narrow-band low-power receiver. The drain nodes of the switches are biased by the DC feed of the balun, which is grounded to provide maximum gate-source/drain voltage swing over the switches. The source nodes of the switches are ac-coupled to a subsequent on-chip BPA. The load capacitors are MIM (metal-insulator-metal) capacitors of 20 pF.

The 4-phase clock generator is based on [2] and [21] and is shown in Fig. 16(b) and (c). An external $2f_{LO}$ source is converted to a differential signal via an off-chip balun and then AC-coupled to two self-biased buffers. A frequency divide-by-two loop generates a single-ended f_{LO} clock, which is subsequently fed to a shift register to produce the 4-phase f_{LO} clock. 25% duty cycle is obtained by ANDing the shift register's outputs with the $2f_{LO}$ clocks.

C. Band-Pass Amplifier

To reject the DC offset generated by the preceding stage, the baseband amplifier is configured as an ac-coupled band-pass filter, as shown in Fig. 17. The high-pass cutoff frequency f_{HP} is set by R_F and C_F as $1/(2\pi R_F C_F)$. In order to make the inter-symbol-interference (ISI) negligible, f_{HP} must be less than one-thousandth of the symbol rate [22], which is 187.5 Hz in this design. It's impractical to implement such a low f_{HP} by on-chip passive devices. Thus, a pseudo-resistor [23] is employed to realize the big resistance required by f_{HP}, as shown in Fig. 17. As pseudo-resistors suffer from poor linearity, two of them are connected in series to reduce the voltage swing over the constituting transistors. Also, in practice, the nominal value of R_F is much greater than that required for f_{HP}. This moves the frequency range being distorted by the nonlinear R_F below 187.5 Hz, so as to give negligible impact on signal integrity. Unavoidably, the extremely small f_{HP} gives rise to a huge settling time constant, which is always constrained by communication standards. This issue is alleviated here by shunting the pseudo-resistor with a

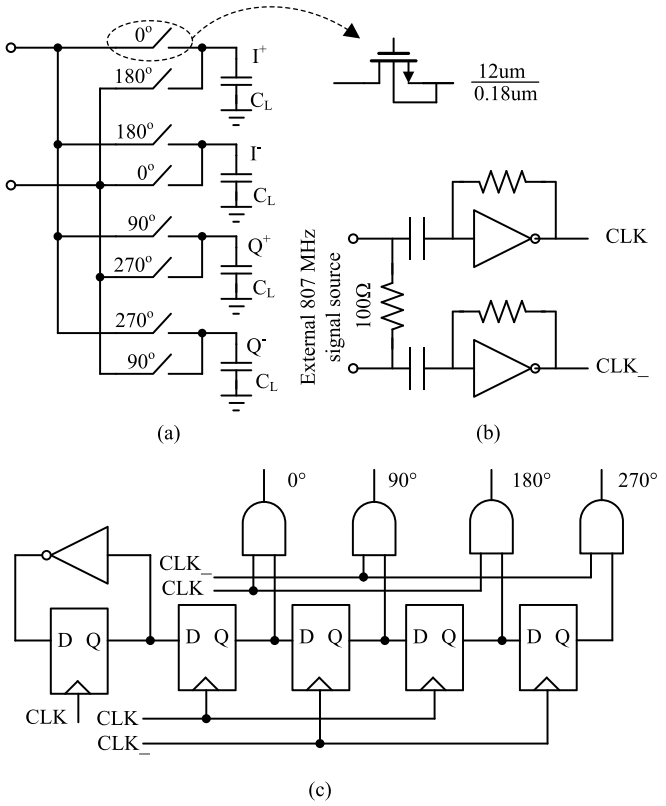


Fig. 16. (a) 4-phase 25% duty cycle clock quadrature passive mixer. (b) Input buffer for external $2f_{LO}$ signal source. (c) 4-phase 25% duty cycle clock generator.

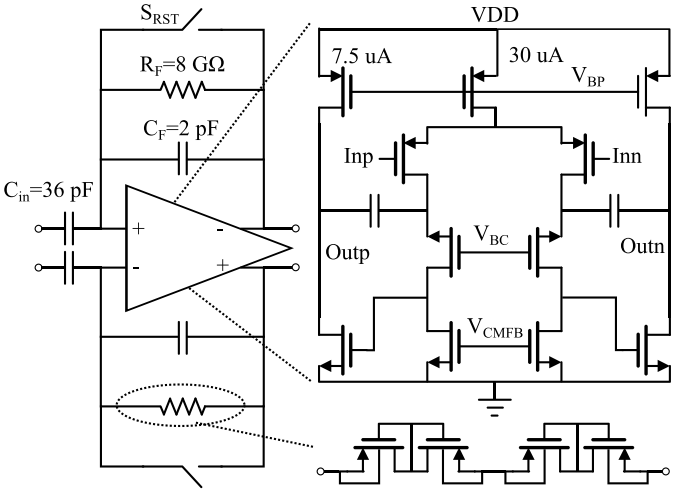


Fig. 17. BPA with feedback pseudo-resistors.

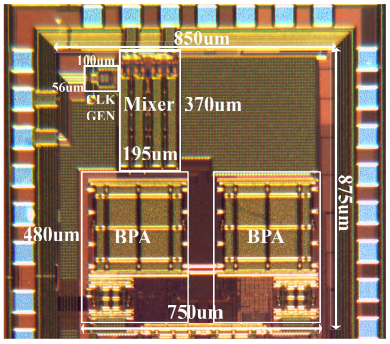


Fig. 18. Die microphotograph.

switch. When the amplifier is re-settling (for example, when the system is switching to another frequency channel), S_{RST} is closed to help the amplifier settle rapidly. After that, S_{RST} is opened to present the desired high-pass cutoff frequency. Considering the trade-off between capacitor size and the complexity of the pseudo-resistors, R_F and C_F are chosen equal to 8 GΩ and 2 pF, respectively, yielding a f_{HP} of 10 Hz. The nonlinear R_F varies from 7.65 GΩ to 8.65 GΩ over the voltage range from −250 mV to 250 mV. The passband gain is set to be 25 dB by the ratio between input capacitor C_{in} and C_F. The low-pass cutoff frequency is designed to be around 250 kHz for a 150 kHz signal bandwidth. The amplifier in Fig. 17 is a fully differential two-stage amplifier with cascode compensation [24], [25]. Transistors are sized in order to optimize the noise performance of the amplifier.

IV. Measurement Results

This passive receiver front-end is fabricated in AMS 0.18 μm CMOS technology with an effective chip area of 0.75 mm^2. A microphotograph of the chip is shown in Fig. 18. The supply voltage is set to 1.2 V for all measurements. An external differential LNA serves as a differential-to-single ended buffer between the output of the on-chip BPA and external measurement equipment.

The performance targets for the passband voltage gain, passband bandwidth, NF and IIP3 are extracted from the system specifications defined in the IEEE 802.15.6 standard as follows. The channel bandwidth of the 402 MHz - 405 MHz band is 300 kHz, so the baseband bandwidth of interest for the measurement is 150 Hz - 150 kHz. The maximum input level is defined as −32 dBm, so the minimum gain is 36 dB if the signal level at the ADC's input needs to reach 4 dBm (i.e., 1 V_{PP}). Low-power short-range radios usually have relaxed requirements on NF and linearity. For instance, Bluetooth Low Energy can tolerate a NF as high as 19 dB for a sensitivity of −80 dBm. For this design, the modulation scheme, sensitivity, symbol rate and bit-error-rate are $\pi/4$-DQPSK, −89 dBm, 187.5 ksps and 10^{-5}, respectively. These design targets are translated into a NF of 18.2 dB. Finally, linearity metric IIP_3 can be calculated for a scenario of −86 dBm desired signal and −76 dBm interference at both adjacent and alternate channels, yielding an IIP_3 of −58.5 dBm for a relative IM3 product of −25 dBc.

The measured downconverted voltage transfer function of the design is shown in Fig. 19. The passband gain is 36.6 dB, while the 3 dB high-pass cutoff and low-pass cutoff frequencies are 7.7Hz and 230 kHz, respectively. The more rapid roll-off that begins around 700 kHz arises from the limited bandwidth of the external LNA, which has a nominal value of 1 MHz. Considering the on-chip BPA has a simulated voltage gain of 25 dB, the voltage gain of the passive RF front-end is 11.6 dB. Using a source impedance that is equal to the measured impedance shown in Fig. 14, i.e., (17.4+j171.4) Ω at 403.5 MHz, post-layout simulations show a passive voltage gain of 12.7 dB, which consists of a −4.6 dB gain of the impedance transformation from 50 Ω to 17.4 Ω, and a

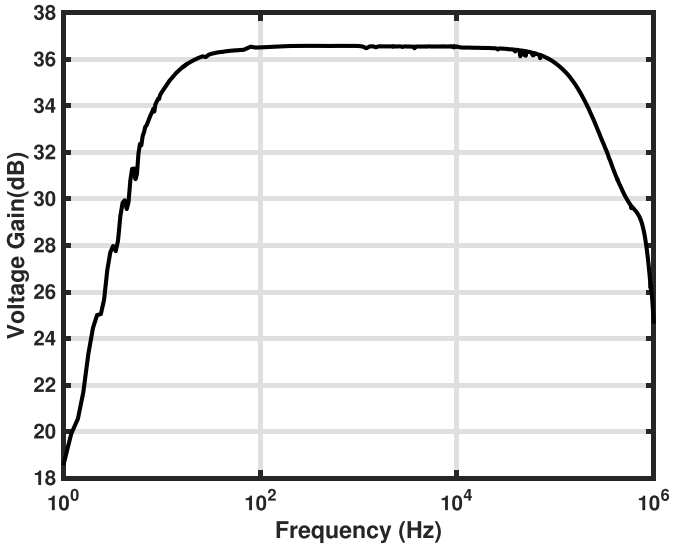


Fig. 19. Measured downconverted frequency response from RF input to the output of the on-chip BPA.

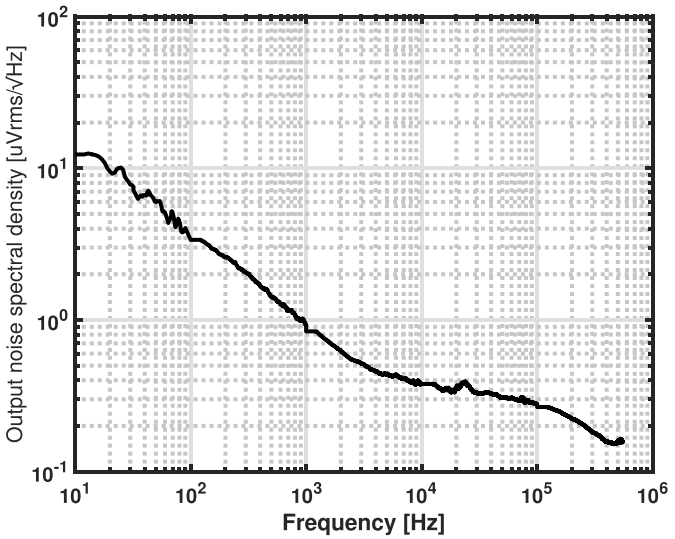


Fig. 20. Output noise density at the on-chip BPA output for a 50 Ω noise source.

subsequent 17.3 dB gain to the mixer output. The 1.1 dB discrepancy between the measured gain and the simulated gain mainly comes from the insertion loss of the off-chip balun (<1.5 dB) [26]. The −4.6 dB voltage attenuation introduced by the step-down impedance transformation may raise questions over the effectiveness of using a source resistance smaller than 50 Ω. This is explained by Equation (12) and its following description. Given that a 25% duty cycle quadrature passive mixer with a 50 Ω resistive source provides a theoretical gain of only −0.9 dB [5], the measurement confirms the enhanced gain provided by the passive network.

The output noise spectral density of the chip with a 50 Ω noise source is shown in Fig. 20. The input-referred integrated noise power over 150 Hz - 150 kHz is 3.68 pV^2_{rms}, yielding an integrated NF of 14.7 dB for a 50 Ω noise source. The spectrum is dominated by the flicker noise up to a frequency of approximately 5 kHz. After that, thermal noise becomes dominant and starts decreasing with frequency around 100 kHz due to the low-pass behavior of the on-chip BPA. Post-layout simulations using the measured (17.4+j171.4) Ω source impedance show that the passive mixer exhibits a NF of 3.8 dB, and the BPA-input-referred integrated noise power of the on-chip BPA is 30 pV^2_{rms}. Using the measured 11.6 dB gain, the two noise results are translated into an overall NF of 12.8 dB, which is 1.9 dB different from the measured 14.7 dB. Several effects could account for the 1.9 dB discrepancy. For example, the loss of the off-chip balun and matching components, the modeling inaccuracies of the off-chip components, and the noise of the external clock and power supply are all possible noise sources. The measured NF is 3.5 dB lower than the NF target of the entire receiver chain, thereby being able to accommodate other noises, as well as distortion, offset, etc. The 14.7 dB NF is dominated by the noise of the on-chip BPA, rather than the passive mixer. It's actually more optimum to partition the noise budget such that the mixer dominates the overall NF since the power consumption of LO buffers can then be reduced. In this proof-of-concept design, the noise performance of the mixer is over-designed.

Linearity metric IIP_3 is usually expressed as an input-referred power quantity for a 50 Ω power-matching scenario. However, the proposed passive network is not power-matched to a 50 Ω signal generator since it aims to maximize voltage gain, rather than power gain. Thus, the input signal level is specified by a voltage quantity. The measured nonlinear behavior of the proposed design is shown in Fig. 21, indicating an in-band IIP_3 of 20.6 dBV. This is equal to 3.6 dBm for a 50 Ω resistance which is a more familiar way of reporting, although the translation is not rigorous. An IIP_3 of 3.6 dBm is much higher that the design target of −58.5 dBm, thus leaving sufficient margin for subsequent stages.

Table II summarizes the performance of the proposed PFE and compares it with several recent low-power receivers as well as two high-performance receivers. Performance benchmarking is done from the following three perspectives.

First of all, [1] and [6] report a 25% duty cycle quadrature passive mixer with a standard 50 Ω interface and with a step-up transformer, respectively. This work has a passive voltage gain of 11.6 dB, which is close to the state-of-the-art of 12 dB achieved in [6] and much higher than the −0.9 dB theoretical limit of the 50 Ω based counterpart [1], [5]. The 11.6 dB passive voltage gain is higher than the 7.2 dB of [7], which is also provided by a step-up transformer. [1] and [6] target much-better performance specifications than the rest designs of the table do and also consume much more power. Hence, we do not benchmark other performance parameters such as NF and IIP_3 against [1] and [6].

Secondly, NF, IIP_3 and power consumption of the proposed design are compared with that of the rest low-power solutions using either PFEs or active front-ends (AFEs). Compared with the AFEs presented in [27] and [28], the proposed PFE has higher NF (the difference ≤1.5 dB) but does not spend any power on active LNAs and mixers, and hence consumes much less overall power than the active counterparts, i.e., 1.1 mW with respect to 1.3 mW of [27] (without any clock circuitry and baseband stages) and 2.7 mW of [28]. Moreover, the IIP_3 of the proposed design is better than that of [27] and [28]

TABLE II
PERFORMANCE COMPARISON

	TCAS-I '15 [27]	TCAS-I '13 [28]	TCAS-I '15 [29]	ISSCC '09 [1]	JSSC '15 [6]	TMTT '13 [7]	RFIC '16 [30]	This work
Application and topology	Low-power active-front-end RX			High-performance passive-front-end RX		Low-power passive-front-end RX		
Integration level	RX FE	RX FE	RX	RX FE	RX	TRX	RX FE + Energy harvester	RX FE
Frequency (GHz)	0.4	0.4	2.4	0.2 - 2.0	5.1 - 5.9	2.4	0.9	0.4
Source	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	Inductive
Technology (nm)	180	130	65	65	65	130	180	180
Passive voltage gain (dB)	-*			-0.9**	12	7.2	N/A	11.6
Passive mixer R_{SW} (Ω)	-			5	57	N/A	N/A	50
NF (dB)	13.2	13.6	28	6.5	5.3	16.1	18.5	14.7
In-band IIP_3 (dBm)	-17***	3	[-14.5, -35]	11	2.6	-2.9	N/A	3.6
Power (mW)	1.3	2.7	0.9	67	11.6	1.1	0.53	1.1
LNA	0.94	N/A	-	-	-			
Mixer	0.36	0	0.18	-	0			
Multi-phase CLK GEN + CLK buffers	-	N/A	0.46 (excl. CLK GEN)	-	1.6	0.4	N/A	0.93
Baseband (zero-IF or IF) stages	-	N/A	0.13	-	10	0.23	N/A	0.16
Others (PLL, ADC, etc)	-	-	0.1	-	0	0.46	-	-
Area/Active core (mm^2)	1.6 / N/A	N/A / 0.12	2 / 0.9	-	N/A / 0.2	2.1 / N/A	5.3 / 1	0.75 / 0.44
Off-chip components	Yes	No	No	No	No	No	Yes	Yes

* Not applicable
** The theoretical conversion gains of a 50 based double-balanced passive mixer with a 4-phases driving clock and an 8-phases driving clock are -0.9 dB and -0.2 dB, respectively [5].
*** Calculated from the reported P_{1dB} of -26.6 dBm by IIP_3=P_{1dB}+9.6 (dB).

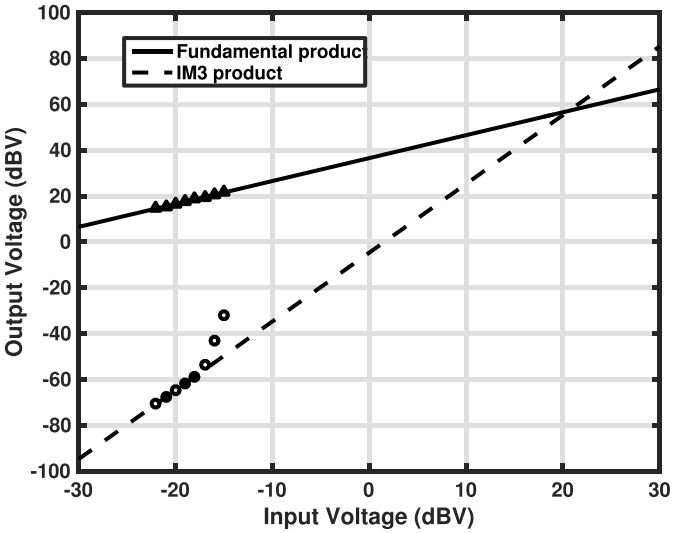


Fig. 21. In-band IIP_3 measurement. Two input tones are located at 10 kHz and 20 kHz offset frequencies, respectively.

due to the passive nature of the mixer. The AFE presented in [29] consumes a bit less power than the proposed design, but has much worse NF and IIP3. The proposed PFE has 6.5 dB higher IIP_3 and 1.4 dB better NF than the PFE presented in [7], while consuming 0.47 mW more power for the same circuit blocks. The PFE presented in [30] has 3.8 dB higher NF and consumes half the power of this work. In summary, the proposed design has better performance than the three AFEs and similar performance to the two PFEs.

Finally, it should be noted that the price paid for the benefits of the proposed technique is the bulky off-chip passive network. However, as discussed in Section III-A, the off-chip implementation is chosen for the sake of verification simplicity in this low-frequency prototype, and a fully integrated implementation (excluding the inductive antenna) is also feasible.

V. CONCLUSION

This paper presents the analysis and design of a PFE using an inductive antenna impedance. The inductive antenna impedance introduces two extra degrees of freedom, i.e., R_A and X_A, to increase the downconverted voltage of the front-end for a given antenna available power. The analysis of the proposed inductive-antenna-based PFE suggests that the PFE offers higher voltage gain and lower NF than a standard 50 Ω-based PFE does. The proposed PFE and a baseband band-pass amplifier are designed in 0.18 μm CMOS technology for the 402-405 MHz band of the IEEE 802.15.6 WBAN standard. The implementation has a passive voltage gain of 11.6 dB, which is close to the state-of-the-art of 12 dB. The NF, IIP_3 and power consumption of the proposed design is better than or similar to several recent low-power active front-ends and passive front-ends.

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Yao Liu was born in China in 1987. He received the M.Sc. and B.Sc. degrees in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2011, respectively, and the Ph.D. degree from the Delft University of Technology in 2017. In 2016, he joined imec, Leuven, Belgium, as an RF designer. His current research interests include analog IC design for wireless communications.

Wouter A. Serdijn (M'98–SM'08–F'11) was born in Zoetermeer, The Netherlands, in 1966. He received the M.Sc. (*cum laude*) and Ph.D. degrees from the Delft University of Technology, Delft, The Netherlands, in 1989 and 1994, respectively. He is currently a Full Professor in bioelectronics with the Delft University of Technology, where he heads the Section Bioelectronics, and also a Visiting Honorary Professor with the Analog and Biomedical Electronics Group, University College London.

His research interests include integrated biomedical circuits and systems for biosignal conditioning and detection, neuroprosthetics, transcutaneous wireless communication, power management, and energy harvesting as applied in, such as, hearing instruments, cardiac pacemakers, cochlear implants, neurostimulators, portable, wearable, implantable and injectable medical devices, and electroceuticals.

He teaches circuit theory, analog integrated circuit design, analog CMOS filter design, active implantable biomedical microsystems, and bioelectronics. He is a co-editor and a co-author of 10 books, 8 book chapters, 3 patents, and over 300 scientific publications and presentations. He received the Electrical Engineering Best Teacher Award in 2001, 2004, and 2015.

Dr. Serdijn has served, a.o., as the General Co-Chair of the IEEE ISCAS 2015 and the IEEE BioCAS 2013, the Technical Program Chair of the IEEE BioCAS 2010 and the IEEE ISCAS in 2010, 2012, and 2014, a member of the Board of Governors of the IEEE Circuits and Systems Society from 2006 to 2011, the Chair of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society and the Steering Committee of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and as the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I: REGULAR PAPERS from 2010 to 2011.

He is an IEEE Distinguished Lecturer and an mentor of the IEEE. In 2016, he received the IEEE Circuits and Systems Meritorious Service Award.