An Autonomous Wireless Sensor Node with Asynchronous ECG Monitoring in 0.18μm CMOS

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***Abstract*—The design of a 13.56MHz/402MHz autonomous wireless sensor node with asynchronous ECG monitoring for near field communication is presented. The sensor node consists of an RF energy harvester (RFEH), a power management unit, an ECG readout, a data encoder and an RF backscattering transmitter. The energy harvester supplies the system with 1.25 V and offers a power conversion efficiency of 19 % from a -13 dBm RF source at 13.56 MHz. The power management unit regulates the output voltage of the RFEH to supply the ECG readout with V_{ECG} = 0.95 V and the data encoder with V_{DE} = 0.65 V. The ECG readout comprises an analog front-end (low noise amplifier and programmable voltage to current converter) and an asynchronous level crossing ADC with 8 bits resolution. The ADC output is encoded by a pulse generator that drives a backscattering transmitter at 402 MHz. The total power consumption of the sensor node circuitry is 9.7 μW for a data rate of 90 kb/s and a heart rate of 70 bpm. The chip has been designed in a 0.18μm CMOS process and shows superior RF input power sensitivity and lower power consumption when compared to previous works.**

***Index Terms*—Autonomous, ECG, wireless, asynchronous, MICS, ISM, WSN, battery-less, BAN.**

I. Introduction

Low power sensor node design has become an important research topic since remote measurement of physical quantities became very attractive to the industry, especially for medical applications that implement the concept of Wireless Body Area Networks (WBAN). However, it is also known that the power consumption and battery lifetime of today's solutions limit the wider use of wireless sensor nodes in such networks.

Many wireless sensor nodes are designed to be autonomous or increase battery life-time [1]–[7]. As an example [5] presents a design that relies on a hybrid energy harvesting solution with external energy storage devices and power gating techniques to bring the power consumption to an average of tens of micro-watts. Although promising, previously designed systems use synchronous sampling and synchronous data transmission [8]–[12], and thereby consume power even when there is no or little sensor activity. A possible solution to minimize power consumption is the use of asynchronous sensor architectures that sample and transmit data only when an event is detected. An event-driven sensor consumes minimal power unless an event is detected. Therefore, on average, it consumes less power than state of the art synchronous systems. In addition, lower average data rate is required for data transmission due to the nature of the data conversion applied to the asynchronous system. The challenge to design an event-driven sensor is the very low power consumption of the circuits while keeping high linearity. Secondly, also the data transmission must be asynchronous, which makes data encoding more difficult to implement.

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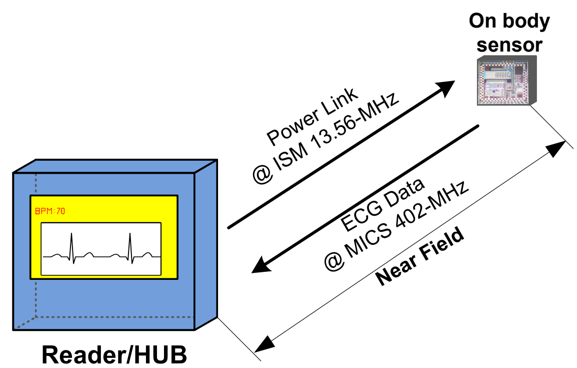

Fig. 1: Diagram of communication between a hub and a sensor.

This paper presents the design of asynchronous ECG monitoring and data transmission that reduces the circuitry power consumption of the sensor node (below 10 μW) [13], [14] without the use of power gating and requiring neither external energy storage devices nor a crystal as a time reference. The autonomous wireless sensor utilizes near field communication and is designed in 0.18μm CMOS IC technology with a sensitivity of -13 dBm (at 13.56 MHz), asynchronous 8-bit ECG readout and backscattering data transmission at 402 MHz.

The paper is organized as follows. In Section II the autonomous wireless sensor with ECG monitoring is presented. Section III presents the experimental results and comparison with the state of the art. Conclusions are drawn in Section IV.

II. Autonomous Wireless ECG Sensor Design

This section presents the proposed autonomous wireless sensor with ECG monitoring and describes the main circuits of the system. The designed sensor is suitable for star network topologies since this topology allows near field direct communication from the sensor to the hub while the hub provides power to the sensor, as depicted in Fig. 1.

The sensor node, which is remotely powered by the hub, is a peripheral device of the network that sends data to the hub

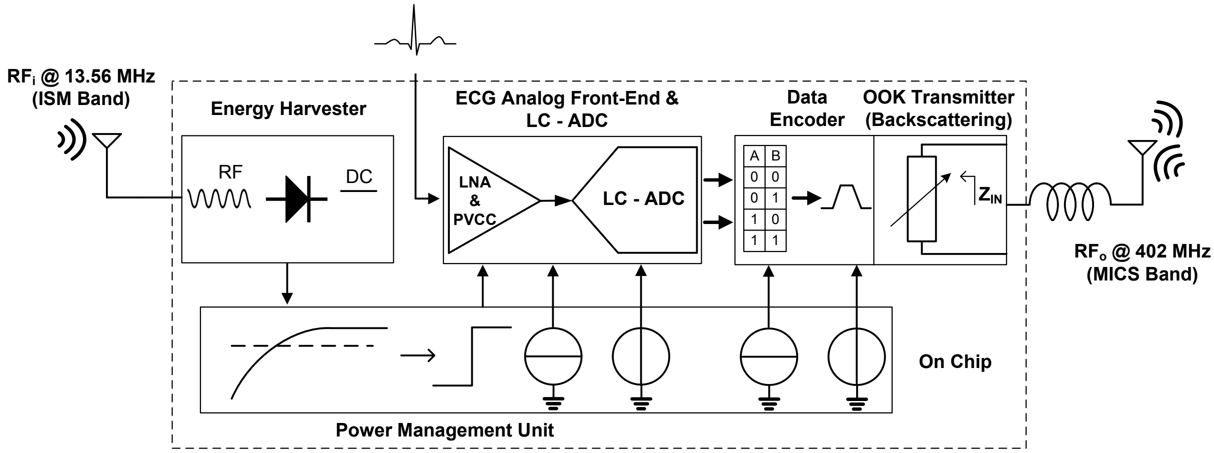

Fig. 2: Block diagram of the MICS/ISM band ECG sensor node.

at the detection of an event. The data processing and memory allocation will be done by the hub. Therefore, the sensor node can operate from very little power.

As it does not require a battery, the designed sensor IC suits disposable devices with low cost for cardiology applications where the user wears the disposable sensor and one uses the mobile hub to measure ECG periodically. In this application the sensor does not require far-field communication since the user can place the receiver close enough to the disposable sensor to read data and after usage the sensor can be discarded.

The 13.56 MHz ISM signal is used to power the IC since in this band it is allowed to transmit high levels of power. However, the 13.56 MHz ISM band does not allow a bandwidth greater than 13 kHz, which is not enough for the application at hand. In addition, in the ISM band the interference might be very strong since the maximum EIRP is roughly 2 W. On the other hand, the 402 MHz MICS band allows broader band data transmission (>1 MHz) if the signal is transmitted 25 dB below the maximum MICS EIRP thus below 25 uW.

Fig. 2 shows the block diagram of the MICS/ISM band sensor node that comprises a passive RF energy harvester (RFEH), a power management unit for voltage regulation and bias current generation, an 8-bit analog front-end (AFE) with a level-crossing sampling ADC for ECG data acquisition, a serial pulse encoder and a passive on-off keying (OOK) MICS-band transmitter. The dual-band feature allows for simultaneous backscattering data transmission and energy harvesting. The sensor node employs no duty-cycling/gating techniques and requires only three external components: two antennas (similar to previous works) and an on-PCB tuning inductor designed for 402MHz. No external crystal, resonator or storage capacitor is required, which enhances system integration.

The sensor node design presented in this paper illustrates that asynchronous operation results in a system with 35 % lower data rate and a 41 % lower power consumption than state of the art synchronous system designs.

A. RF Energy Harvesting and Power Management

The theoretical model and analysis of the RF energy harvester designed in this work have been presented in [15]. Fig. 3 shows the block diagram of the designed RFEH that comprises a passive voltage boosting network and an orthogonally switching charge pump rectifier (OS-CPR). The circuit diagram of the boosting network and on-chip OS-CPR are shown in Fig. 4(a) and Fig. 4(b).

To adequately drive the OS-CPR, the boosting network delivers large swing control (V_{b+} and V_{b-}) and energy signals (V_{r+} and V_{r-}). The resonant circuit of the boosting network is modeled by the self-inductance of the antenna, L_A (9.5 μH), its series resistance, R_A (12 Ω), and capacitance $C_{V,T}$ (14 pF), which is the sum of the on-chip tuning capacitance (C_D and C_B) and input capacitance of the rectifier ($C_{R,T}$). An inductive choke L_C provides a DC short at the input terminals of the rectifier to ensure a zero DC offset error at the input of the OS-CPR. In the boosting network design there is a trade-off between the value of $C_{V,T}$ and L_A. If L_A is made too large to increase voltage gain, $C_{V,T}$ has to be very small. In such a case, the resonance frequency will be too sensitive to the rectifier input capacitance that changes with the load and input power. Moreover, increasing the value of L_A requires an inductor physically bigger and consequently has a bigger R_A, which limits the voltage gain of the boosting network.

The rectifier circuitry (of a single stage) is made up of PMOS transistors as voltage-controlled switches (M_1 and M_2) and capacitors for AC coupling (C_C) and energy storage (C_{R1} and C_{R2}). Table I shows the component values of the designed RFEH, in which the RFEH input impedance of the chip is roughly (16 - j815) Ω.

Fig. 5 shows the various waveforms in the charge pump rectifier. Each stage has two different DC voltage levels (V_{CR1} and V_{CR2}) and AC voltages that are provided by the boosting

TABLE I: RFEH Component Values

Device	Value	Device	Value
C_B	7.5 pF	C_{DC}	≃90 fF
C_D	19.5 pF	R_{DC}	350 kΩ
$C_{R,T}$	≃17 pF	C_{R1}, C_{R2}	9.7 pF
C_C	9 pF	M_1, M_2	750/0.2

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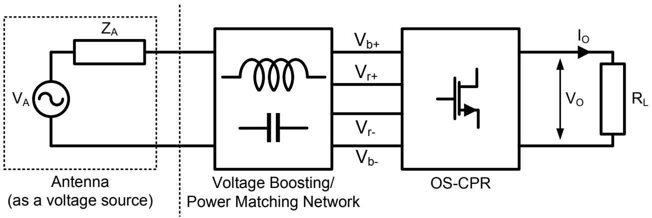
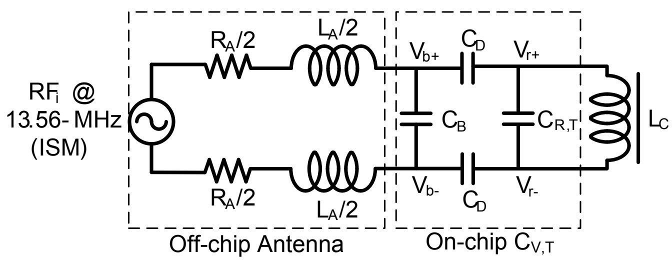


Fig. 3: Block diagram of the RF energy harvester [15].

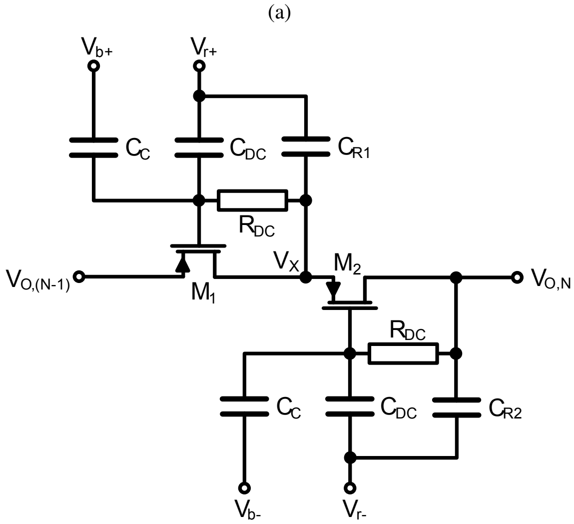
network. Due to DC voltage differences within the stage, the transistors may conduct current in the backward direction in the phase they should be turned off. Known as flow-back current this effect reduces the efficiency of the rectifier. To reduce the flow-back current, parasitic capacitances $\mathrm{C_{DC}}$ and resistors $\mathrm{R_{DC}}$ set the DC voltages $\mathrm{V_{CR1}}$ and $\mathrm{V_{CR2}}$ at the gate of $\mathrm{M_1}$ and $\mathrm{M_2}$, respectively, to guarantee that drain and source potentials are smaller than the gate potential in the off phase.

The design procedure of the RFEH is [15]:

1) Calculate the self-inductance ($\mathrm{L_A} = \mathrm{R_A}Q\omega^{-1}$) and tuning capacitance ($\mathrm{C_{V,T}} = (\omega^2 \mathrm{L_A})^{-1}$) of the boosting network.
2) Calculate the voltage swings of the rectifier ($\mathrm{V_r}$) and control signals ($\mathrm{V_b}$).
3) Determine the number of stages (N).
4) Determine the aspect ratios (W/L) of transistors $\mathrm{M_1}$ and $\mathrm{M_2}$ from the model.
5) Determine $\mathrm{C_C}$, which has to be bigger than the gate-source capacitance of $\mathrm{M_1}$ and $\mathrm{M_2}$.
6) For minimum ripple, calculate $\mathrm{C_{R1}}$ and $\mathrm{C_{R2}}$.
7) Run PSS, PAC simulations or transient with dfft analysis.
8) Fine-tune $\mathrm{C_{V,T}}$ and/or the OS-CPR component values for frequency optimization.
9) Repeat steps 3-8 for optimization.



(a)



(b)

Fig. 4: Circuit diagram of (a) boosting network and (b) a single stage of the on-chip rectifier in the RFEH [15].

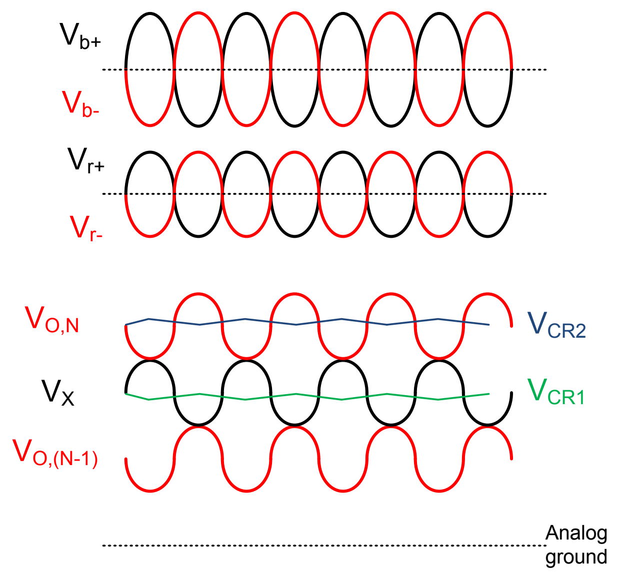


Fig. 5: Waveforms of the OS-CPR integrated in the RFEH.

From -13 dBm 13.56 MHz input RF power, the output of the 5-stage OS-CPR sets the power supply voltage ($\mathrm{V_{DC}} = \mathrm{V_{O,N}}$) of the sensor node at 1.25 V for a resistive load of 110 kΩ with 19 % power conversion efficiency. The RFEH shows similar behavior when connected to the equivalent resistance of the sensor circuitry, which is about 150 kΩ.

The all CMOS-based, subthreshold operated power management unit is shown in Fig. 6. It includes voltage ($\mathrm{V_{REF}}$) and current ($\mathrm{I_{REF}}$) references and two linear voltage regulators that supply the ECG analog front-end ($\mathrm{V_{ECG}}$) and the asynchronous data encoder ($\mathrm{V_{DE}}$). Proper selection of R1, R2 and N sets temperature-independent voltage reference $\mathrm{V_{REF}}$ at 0.54 V, which is derived by combining PTAT and CTAT voltages $\mathrm{V_{R2}}$ and $\mathrm{V_{GS,4}}$, respectively. Current reference $\mathrm{I_{REF}}$ (10 nA) is required for circuits in the ECG AFE and transmitter. Regulated voltages $\mathrm{V_{ECG}}$ and $\mathrm{V_{DE}}$ vary $\leq$13 % for 8 dB (-9±4 dBm) change in input power. All power supplies are filtered using on-chip decoupling capacitors.

B. Analog Front-End and Level-Crossing ADC

In Fig. 7, the ECG monitoring front-end comprises a fully-differential low noise amplifier (LNA), a programmable voltage-to-current converter (PVCC) and a current-mode level-crossing analog-to-digital converter (LC-ADC). The sparse ECG signal with long periods of low frequency variation requires the LC-ADC to hold the comparison window for a long time (hundreds of ms). Therefore the LC-ADC in the

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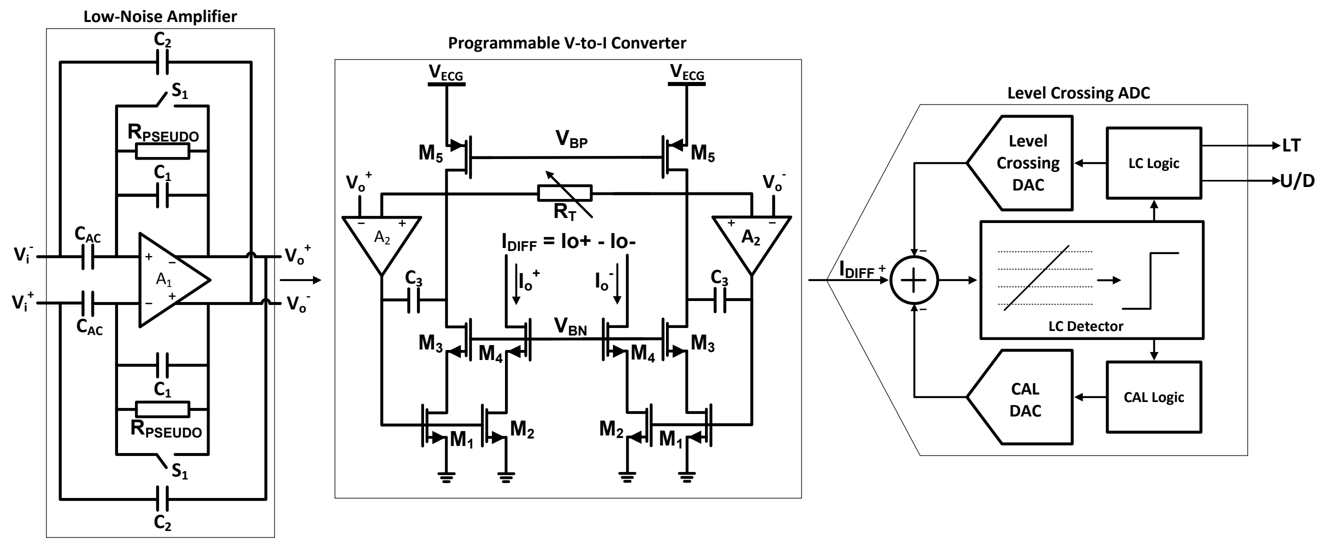

Fig. 7: Circuit diagram of the ECG monitoring analog front-end.

proposed AFE operates in the current domain instead of the charge domain [16].

The LNA is configured as a band-pass filter with a voltage gain (C_{AC}/C_1) of 34 dB from 0.06 Hz to 950 Hz. Pseudo-resistor R_{PSEUDO} and negative feedback capacitor C_1 set the lower cutoff frequency, and the voltage gain and bandwidth of op-amp A_1 set the upper cutoff frequency. For a 6 mVpp input signal, the input referred noise and total harmonic distortion (THD) values are 3.77 μVrms and 0.15 %, respectively. Switches S_1 set the input common-mode voltage at start-up. To increase the input impedance, a positive feedback loop (via capacitor C_2) is introduced. The PVCC is a fully differential programmable gain (2 μA/V to 16 μA/V) transconductance (voltage-to-current) amplifier. Its output current is fed into the LC-ADC.

The LC-ADC employs two complementary DACs. The level-crossing DAC adjusts the comparison window after each conversion by adding/subtracting current at the input node of the level-crossing (LC) detector. The calibration DAC (CAL DAC) cancels any DC offset during system reset. The residue current is fed to the level-crossing detector, which outputs a pulse in the case of a level crossing. Unlike uniform sampling, the level-transition (LT) and UP/DOWN (U/D) pulse sequences are generated only when an input signal crosses a predefined threshold level as illustrated in Fig. 8.

The ECG readout circuits include two RC oscillators on the chip for generating a synchronous clock signal to calibrate the offset of the two DACs, respectively. The oscillators are only enabled for calibration during reset. The offset calibration is a typical foreground calibration that is enabled during system startup or manual resetting. The entire ECG front-end achieves a measured SNDR of around 48 dB when we apply a 6 mVpp sinusoidal input signal at the input of the LNA. More details on the ECG monitoring front-end are provided in [16].

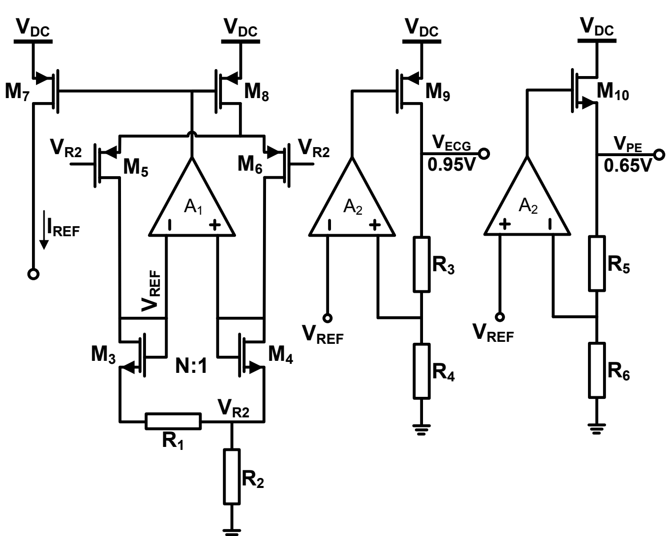

Fig. 6: Circuit diagram of the power management unit.

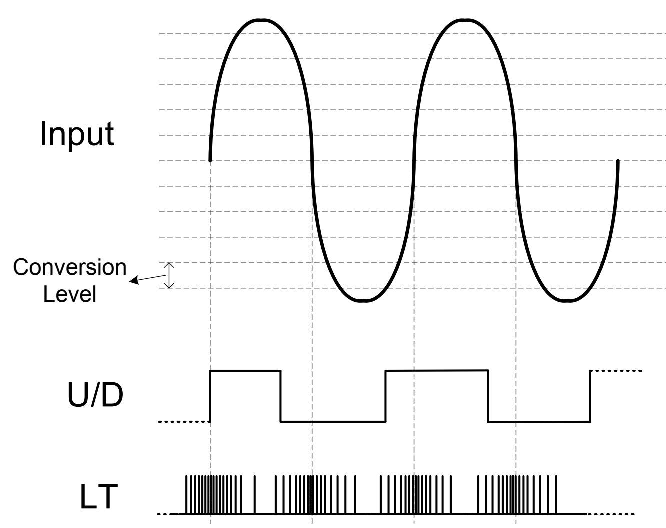

Fig. 8: Input and output signals of the level-crossing ADC.

C. Asynchronous Data Transmission

The level-crossing ADC provides two binary signals (LT and U/D) that are both fed to the low-power data transmitter. As the transmitter is powered by an RF energy harvester, to minimize power consumption, the data transmission is only enabled when ADC data conversion is active [17]. The 2-output bits of the ADC are combined and transmitted simultaneously, otherwise information would be lost. Employing pulse duration modulation (PDM), the 2-bit data stream is combined to generate pulses with different time duration for upward conversion and downward conversion. This means that the transmitter produces a pulse when LT indicates a conversion and U/D defines the duration of this pulse. In this way the 2-bit information can be embedded in a single pulse. Fig. 9 presents the circuit diagram of the transmitter that includes a digital pulse encoder and a backscattering network. The pulses are generated by comparing LT to $\overline{\mathrm{LT}}$, the latter being the complement of LT delayed by six cascaded current starved inverters. The delay time is set by U/D that makes the pulses longer when it is set to 1.

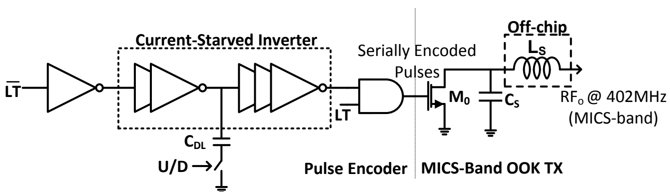

Fig. 9: Circuit diagram of the asynchronous transmitter.

The delay is defined by the current drawn in the inverters and capacitor $\mathrm{C_{DL}}$. For U/D equal to 1 (upward level crossing) $\mathrm{C_{DL}}$ is connected to ground, thus the pulse width is longer. For U/D equal to 0 (downward level crossing) $\mathrm{C_{DL}}$ is disconnected from ground, thus the duration of the pulses is shorter. Fig. 10 shows the waveforms of the low-power pulse encoder: the pulse duration is $\mathrm{t_U}$ for upward conversion and $\mathrm{t_D}$ for downward conversion. In the circuit designed for backscattering data transmission, the pulsed signal modulates the 402MHz RF signal received in the LC network, implementing ON-OFF-Keying modulation through transistor $\mathrm{M_0}$ (see Fig. 9). The values of $\mathrm{L_S}$ and $\mathrm{C_S}$ are 32 nH and 4.9 pF, respectively.

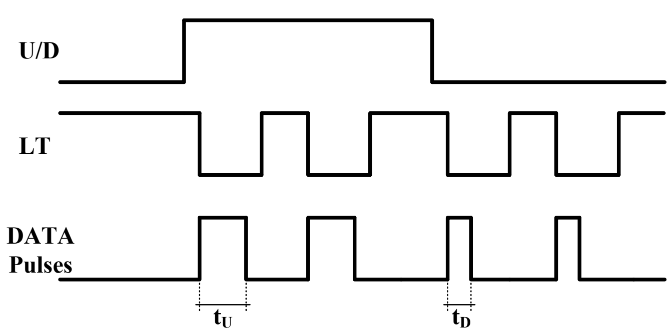

Fig. 10: Waveforms of the asynchronous encoder.

Fig. 11 shows the power distribution, in percentage, of the blocks in the designed sensor node.

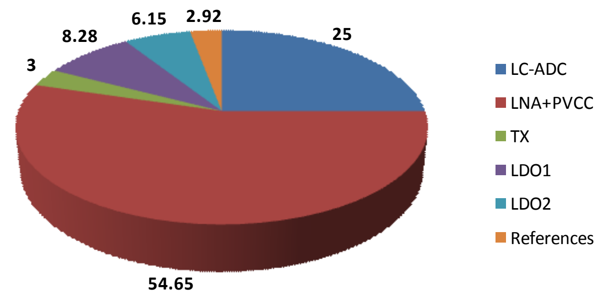

Fig. 11: Power consumption per block in percentage.

III. Experimental Results

Realized in low-cost 0.18μm CMOS IC technology, the ISM/MICS-band autonomous wireless sensor node with the asynchronous 8-bit ECG AFE occupies 1.9 x 2.0 mm^2 and is shown in Fig. 12. The sensor node is mounted on a double-sided, FR-4 laminate substrate with a high quality factor coil (antenna) etched on the back plate (see Fig. 13). The physical and electrical properties of the customized antenna coil are presented in Table II. The coil is modeled using ADS Momentum. At 13.56 MHz, the measured real and imaginary impedance components of the antenna coil are 12.7 Ω and 810 Ω, respectively. Simulation and measurement results show less than 5 % discrepancy.

The energy harvester operates over a large range of resistive loads (0.1 MΩ to 0.82 MΩ). Defined as the ratio of the electrical power delivered to the load and the power received by the antenna, the power conversion efficiency (PCE) equals 19 % for a 110 kΩ load at -13 dBm input power ($\mathrm{P_{IN}}$), as shown in Fig. 14. The input power has been calibrated using a Power Network Analyzer (PNA). The two ports of the PNA

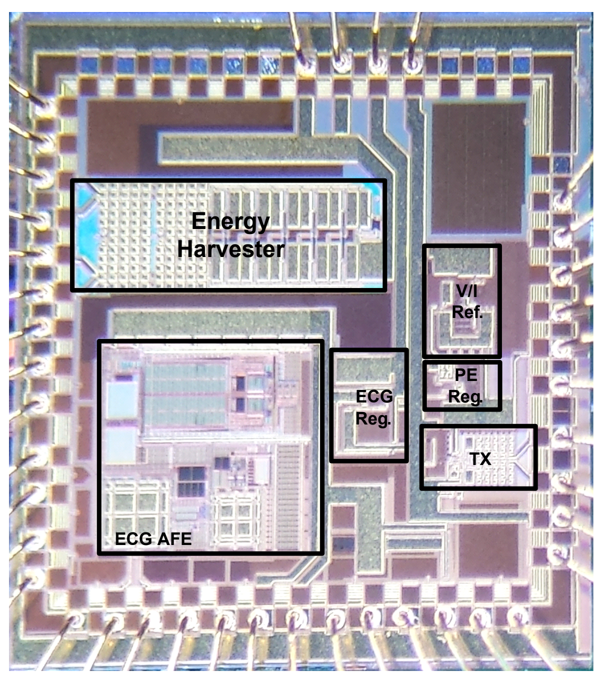

Fig. 12: Chip micrograph of the autonomous ECG wireless sensor node.

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were connected to two aligned coils, being the same coils used in the chip test, separated by a distance of 20 cm. After measuring the scattering parameters, the data was inserted in a transformer model to calculate the coupling coefficient. With the coupling coefficient, it is possible to calculate the power received by the antenna taking into account the chip input impedance that is (16 - j815) Ω.

Fig. 15 shows the ECG front-end supply voltage (V_{ECG}) and the data encoder supply voltage (V_{DE}) as a function of the input power demonstrating that both supply voltages vary less than 13 % for -13 dBm $\leq P_{IN} \leq -5$ dBm.

The measured low noise amplifier gain and SNDR of the ECG monitoring front-end over frequency are presented in Fig. 16 and Fig. 17, respectively. The plot proves the performance of the ECG front-end with 34 dB gain from 0.06 Hz to 950 Hz and 48 dB SNDR for an input voltage of 6 mV. The LC-ADC has both magnitude resolution and time resolution. As time resolution is included in the measurement, the overall SNDR is degraded compared to the standalone LNA SNDR.

Fig. 18 shows the link margin of the system. The link margin is measured using a commercial antenna from YAGEO (Phycomp part no. CAN4313 121 200431B). Since the transmitter is realized with backscattering, if a reader (hub) transmits the maximum allowed EIRP in the 402-MHz MICS band (-16 dBm), at a distance of 20 cm between the reader and the sensor and using the receiver as presented in this manuscript, reliable detection of the signal is still feasible. The reader receives a power of roughly -76 dBm and an LNA with about 50 dB gain is required to be able to cover distances up to 20 cm. For longer distances the received power is too low, < -80 dBm, and thus a more sensitive envelope detector would be necessary or the LNA would need more than 50 dB of gain. For an EIRP of 2 W at 13.56 MHz, the sensor node can be placed at a distance

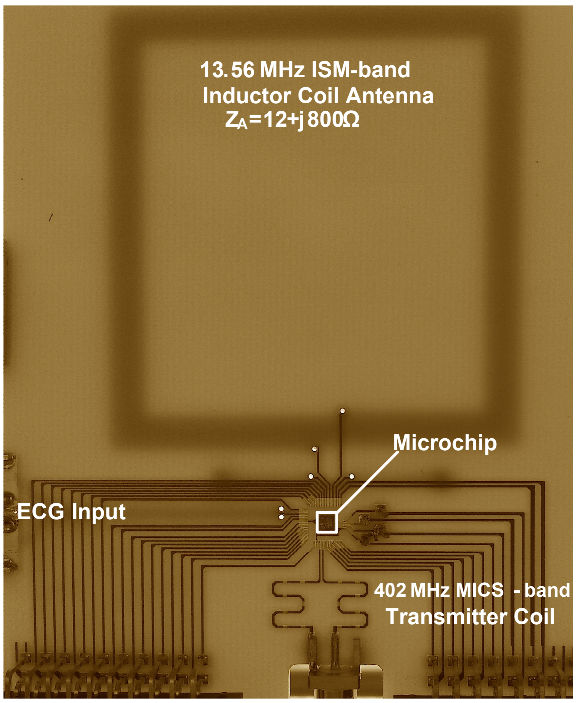


Fig. 13: FR-4 PCB for sensor node test.

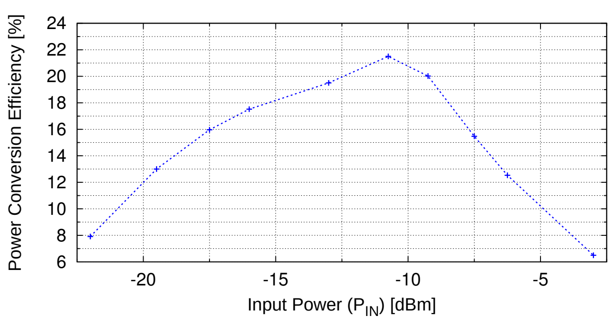


Fig. 14: Measured RFEH power conversion efficiency as a function of input power for a 110 kΩ load.

TABLE II: Physical and electrical properties of the antenna

Physical	1/2 oz. 1.55 mm	Electrical	@13.56 MHz
Outer dim. (mm^2)	56 x 50	L_A (μH)	9.5
Inner dim. (mm^2)	48 x 42	R_A (Ω)	12
Trace width (mm)	0.25	C_A (pF)	2.4
Trace space (mm)	0.25	f_{SR} (MHz)	33
No. of turns	8	Q-Factor	67

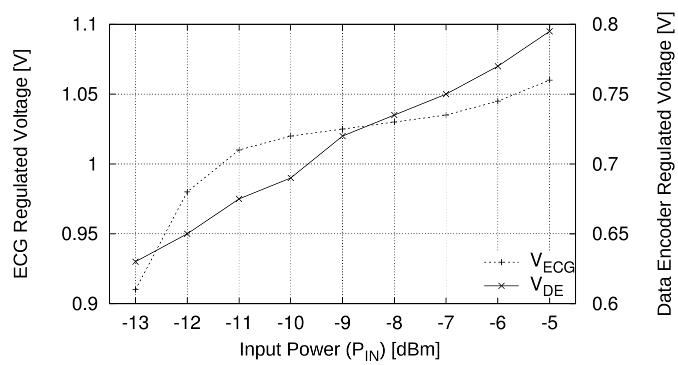


Fig. 15: Measured ECG monitoring and data encoder supply voltages as a function of input power.

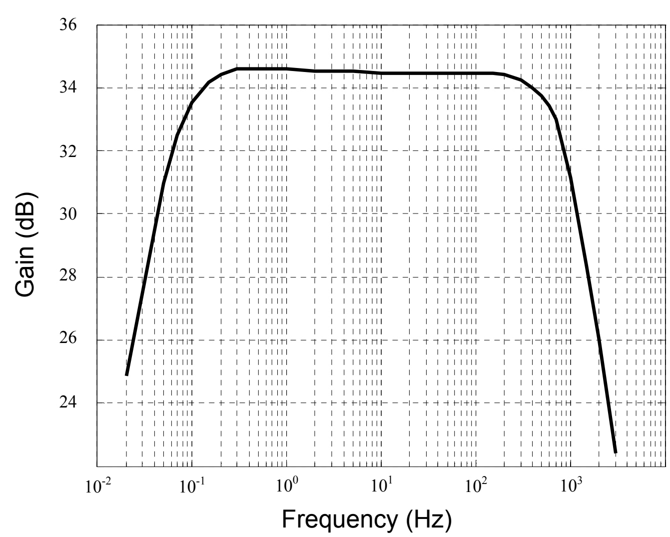


Fig. 16: Measured gain and bandwidth of the low noise amplifier.

of 40 cm from the hub to receive an RF power of -13 dBm. At 40 cm the required sensitivity of the MICS receiver is -87 dBm. Beyond 40 cm the sensor node cannot be powered as the ISM RF power received by the antenna is smaller than -13 dBm (i.e., the minimum required RF power).

Fig. 19(a) and Fig. 19(b) illustrate the measured waveforms of the asynchronous pulse encoder. In Fig. 19(a) the output of the pulse encoder is presented for a LT transition with U/D = 0. In this condition the pulse width is 80ns. For a LT transition with U/D = 1, the pulse width equals 40ns, as shown in Fig. 19(b).

The output signals of the sensor node are shown in Fig. 20. In this measurement an input voltage of 2.5mV peak to peak is applied to the input and the sensor node is remotely powered by an RF signal of -13 dBm.

For system validation, the ECG waveform is reconstructed from the RF signal available from the output of the MICS-band OOK transmitter. Fig. 21 shows the measured and reconstructed ECG waveform. In the measurement, the output of the transmitter is connected to an envelope detector, followed by an IF amplifier, as depicted in Fig. 22. The IF amplifier amplifies the 25MHz base-band signal and filters unwanted RF noise. For the applied ECG signal the ADC converts on average 45k times in one second. Since each conversion includes 2 bits, thus we can say that the sensor has a data rate of 90 kbits per second. This value, however, is not fixed and the date rate depends on the number of conversions made. A higher input frequency would require a higher data rate, but the analog front-end limits the maximum frequency to 1 kHz. Hence, a maximum data rate in the range of hundreds of kb/s is expected. Fig. 23 shows the measured power consumption of the sensor node as a function of the data rate.

Table III compares the performance of this work with that of recently published designs. Among the many parameters shown in Table III, this work demonstrates superior design characteristics, such as high sensitivity (-13 dBm), lower average sampling rate and the power consumption is 9.7 μW, which is 41 % lower than the state of the art. Moreover, the designed IC allows for high system integration with three external components.

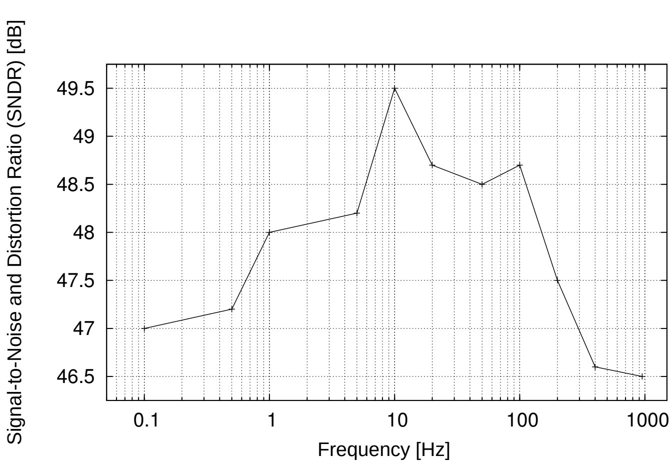


Fig. 17: Measured total SNDR of the ECG monitoring front-end.

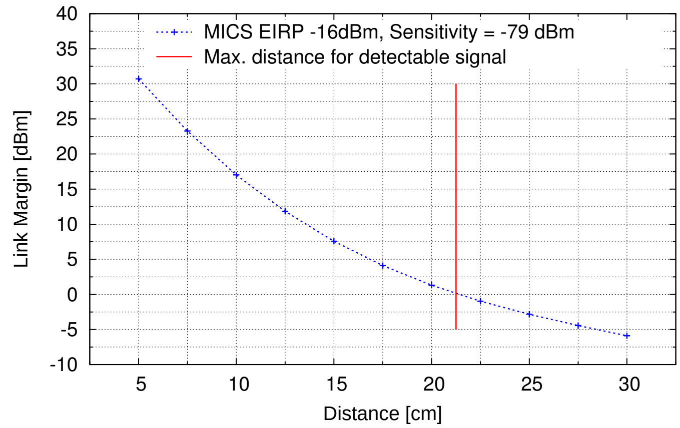
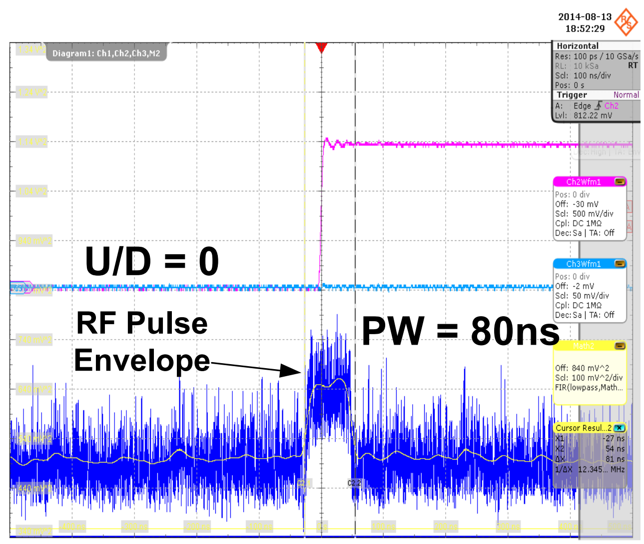
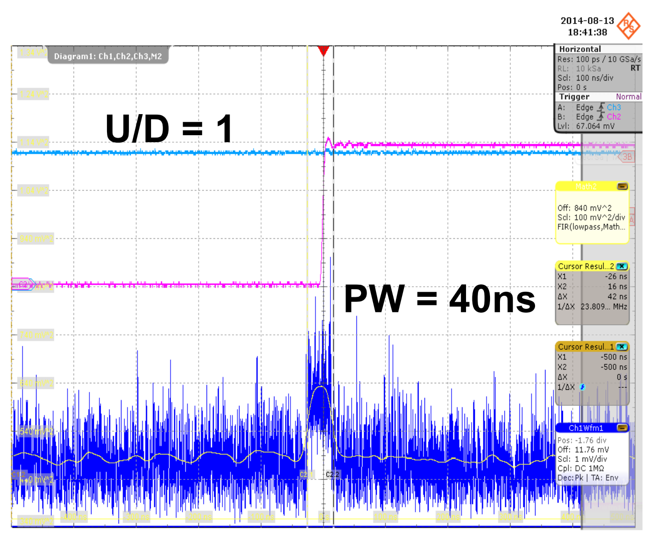


Fig. 18: Estimated link margin for data transmission in the 402MHz MICS band.



(a)



(b)

Fig. 19: Measured encoder output waveforms: (a) 80 ns for U/D = 0 and (b) 40 ns for U/D = 1.

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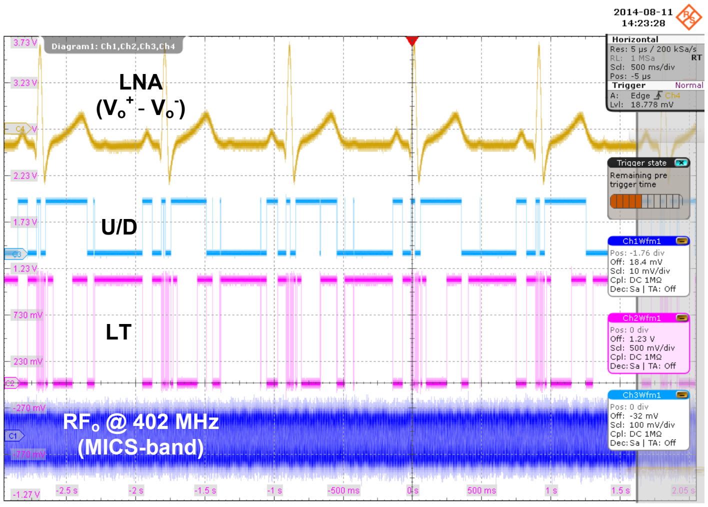

Fig. 20: Measured output signals of the sensor node.

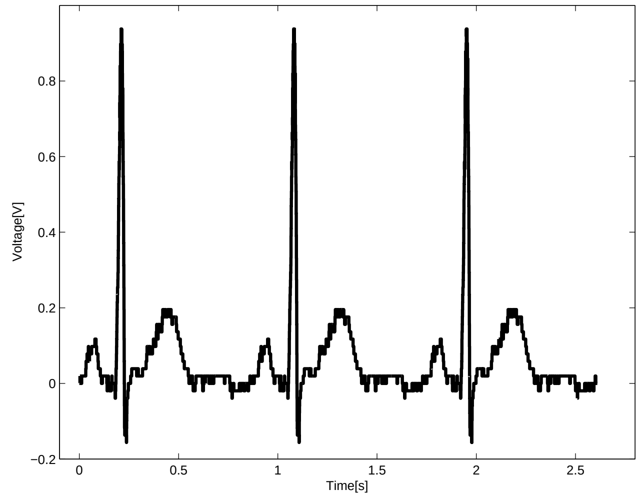

Fig. 21: ECG signal reconstructed from data transmitted by the sensor node.

TABLE III: Summary and comparison of the sensor node with previously published designs

Specifications	This Work	[1]	[2]	[3]	[4]
Application	Near-Field ECG Monitoring	Far-Field Neural Recording	Far-Field General purpose	Near-Field ECG Monitoring	Far-Field General purpose
Type of Sensor	ECG	Neural	EEG, EMG	ECG	ECG, EEG and EMG
Type of Energy Harvesting	RF	RF	RF	Battery	RF/Thermal
Sensitivity (dBm)	-13	-8	-12	n.a.	$-10^{\S}$
Supply Voltage (V)	1.25	0.8	1.8	1.2/3	1.35
Number of Analog Channel(s)	1	1	1	1	4
ADC Resolution (bits)	8	8	8	12	8
Input referred noise (V)	16.8μVrms†	14.5μVrms	1.25μVrms	1.5μVrms†	$<2\mu$Vrms
Frequency (MHz)	13.56/402	915	900	13.56	402/433
Data Rate (kb/s)	90	150-800	up to 500	424	200
External Components	1 TX Inductor	n.a.	Storage Capacitor	1 Crystal, NFC IC	2 Crystals, Storage Cap. and TX Inductor
Power Consumption (μW)	9.7	20	16.6	18.24	19
Power Consumption Distribution among Active blocks	1-Ch. FE, 8bit ADC, PE and TX	1-Ch. FE, 8bit ADC, Logic RX and TX	1-Ch. FE, 8bit ADC, Logic and TX	1-Ch. FE, 12bit ADC, MCU, SRAM and FeRAM	1-Ch. FE, 8bit ADC, DSP and 0.013% Duty Cycled TX
Modulation (TX)	OOK	OOK	ASK	ASK	BFSK
Area(mm^2)	1.9x2.0	0.96x1.6	2.0	6.9x6.9	3.3x2.5
Overall system size(cm)	9x7.5‡	1x1.5	0.91x0.73	n.r.	n.r.
Technology CMOS(μm)	0.18	0.13	0.13	0.13	0.13

† Input referred noise calculated for 6mV input voltage.
‡ Including test structure on the PCB such as connectors, trace lines and antennas without size optimization.
§ -10 dBm is used for sensor kick-start only.

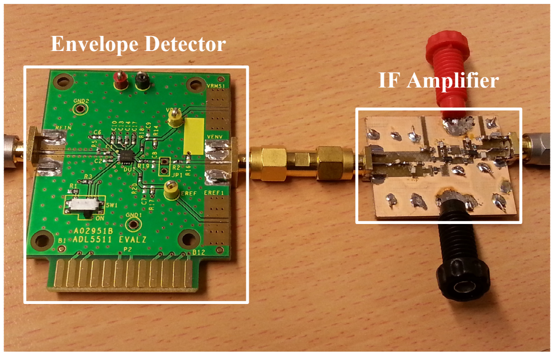

Fig. 22: Envelope detector and IF amplifier used in the ECG waveform reconstruction.

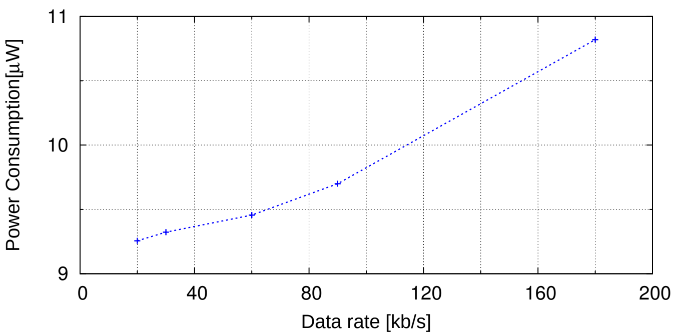

Fig. 23: Measured power consumption as a function of data rate.

IV. Conclusion

A 13.56/402 MHz autonomous wireless sensor node with ECG monitoring has been fabricated in standard 0.18 μm CMOS IC technology. Powered from a -13 dBm RF signal at 13.56 MHz, the energy harvester achieves a maximum power conversion efficiency of 19 %. Asynchronous data encoding has been demonstrated. The total power consumption of the ECG sensor node is 9.7 μW for a data rate of 90 kb/s.

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