An ECG Recording Front-End with Continuous-Time Level-Crossing Sampling

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***Abstract*— An ECG recording front-end with a continuous-time asynchronous level-crossing analog-to-digital converter (LC-ADC) is proposed. The system is a voltage and current mixed-mode system, which comprises a low noise amplifier (LNA), a programmable voltage-to-current converter (PVCC) as a programmable gain amplifier (PGA) and an LC-ADC with calibration DACs and an RC oscillator. The LNA shows an input referred noise of 3.77 μV_{rms} over 0.06 Hz - 950 Hz bandwidth. The total harmonic distortion (THD) of the LNA is 0.15% for a 10 mV_{pp} input. The ECG front-end consumes 8.49 µW from a 1 V supply and achieves an ENOB up to 8 bits. The core area of the proposed front-end is 690×710 μm^2, fabricated in a 0.18 µm CMOS technology.**

***Index Terms*— biomedical recording system, ECG recording, analog-to-digital conversion, pseudo-resistor, voltage-to-current converter, asynchronous ADC, level-crossing ADC, offset calibration, level-crossing sampling**

I. Introduction

Wearable systems with wireless biomedical data recording are nowadays drawing enormous attention from medical and consumer electronics industries. In such a system, the signal acquisition front-end plays a key role in the definition of signal fidelity, transmitted data size and power consumption. Conventional readout interfaces, utilizing uniform sampling, constantly generate samples and consume power during data transmission regardless of the sparse biomedical signals. To decrease the data size and power consumption of the transmitter from the sensor side, data compression or non-uniform sampling has been developed [1]-[5]. Level-crossing sampling is an attractive solution among these options as samples are generated only when the input signal crosses predefined threshold levels. In other words, there is no sampling if the input signal remains constant, reducing data size and power consumption [6]-[14]. Most of the previously reported works regarding level-crossing sampling are either theoretical analyses or standalone LC-ADC designs. As there are only few fully integrated systems with level-crossing sampling for biomedical applications, this inspired us to design the whole readout front-end and apply it to biomedical signal recording.

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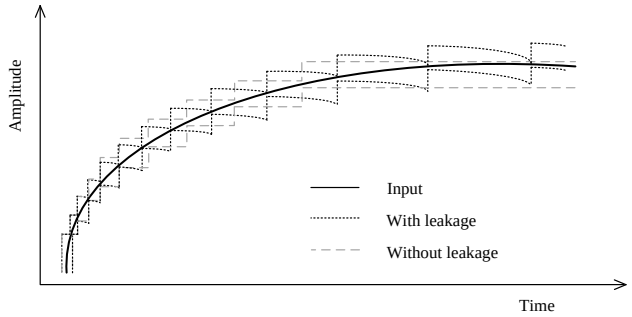


Fig. 1 Comparison window is distorted due to the leakage in the capacitive DAC.

This work is a follow-up of previous work [15], but with the entire readout system integrated on a single chip.

The recently published LC-ADCs [6]-[15] can be divided into different categories. First, based on how the level crossing is detected, there are floating-window and fixed-window structures. The floating-window structure suffers from variations of the comparator offset and the need for a large common-mode swing while the fixed-window does not. Second, considering the feedback loops, a distinction can be made between the use of capacitive and resistive DACs. The capacitive DAC does not consume static power but the leakage current becomes a fundamental issue since the LC-ADC does not periodically refresh its capacitor array. As shown in Fig. 1, the comparison window is distorted due to the leakage. So it is not practical to use the capacitive DAC in a LC-ADC for applications in which the input frequency can be as low as mHz. The LC-ADC in previous works [12][15] was implemented with a single-bit capacitive-feedback DAC and fixed-window detection, leading to considerable power savings. However, when the input signal lowers to Hz or sub-Hz, the capacitive DACs are not able to hold the input signal for a long time, resulting in dramatic SNDR degradation. In summary, the requirements for integrating an LC-ADC in a readout system for biomedical applications are the following:

1) the feedback DACs should not suffer from leakage and the performance should not degrade at very low frequencies (down to sub-Hz);

2) fixed-window detection for the comparators is necessary to save power while maintaining the same performance;

3) on-chip automatic calibration should be integrated to

reduce offset.

From the requirements mentioned above, we conclude that a resistive DAC or a current-mode DAC should be chosen because of its better performance at low frequencies, since they are not susceptible to leakage. Both options have their own advantages and disadvantages. We eventually chose the current-mode approach as offset injection and cancellation can be done at the same current summation node, as will be explained in the following sections.

In this paper, we address the issues mentioned above and describe the design of an ECG readout system. The chip includes a low-noise amplifier (LNA), a programmable voltage-to-current converter (PVCC), a 7-bit level-crossing ADC with calibration DACs and an RC oscillator. More details of the proposed LC-ADC are discussed in the following sections. The system working principle is presented in Section II. Section III describes the analog front-end, while Section IV presents the LC-ADC implementation. Measurements are reported in Section V, followed by the conclusion in Section VI.

II. System Design

To achieve a good tradeoff between power efficiency and conversion accuracy, a typical signal processing chain usually starts with an LNA, followed by a PGA and a successive approximation register (SAR) ADC [16][17]. The LNA is optimized for noise efficiency [24] and distortion while the PGA is optimized for driving the capacitive SAR-ADC, adjusting the gain. A simple way to utilize level-crossing sampling is replacing the capacitive SAR-ADC with a capacitive LC-ADC like the ones in [11]-[15]. However, as mentioned in Section I, there are leakage related issues associated with capacitive structures at low frequency applications. Also, fixed-window detection should be used as the common-mode voltage of the comparator is fixed and thus the requirements on the comparator design can be achieved. Consequently, a resistive DAC structure [7] is not applicable in this design as the common-mode voltage of the comparator is not fixed. Furthermore, the power supply limits the dynamic range in a voltage domain system, which becomes even more serious for low-voltage designs.

To overcome the issues mentioned above, we propose the voltage and current mixed system shown in Fig. 2. The system is a fully differential system to obtain a good linearity. The differential input signal is amplified by the LNA in the voltage domain and then converted into a current by the programmable voltage-to-current converter (PVCC). The PVCC adjusts the gain of the system and outputs current for the LC-ADC. The output current of the PVCC, the level-crossing DAC (LC DAC) and the calibration DAC (CAL-DAC) are summed at the same node. Then a current-to-voltage (I/V) converter converts the residue current into a voltage. The details of the I/V converter will be discussed in section IV. After the I/V conversion, the comparators (CMP) take the logic decision from the output of the I/V converter. The control logic (LC Logic and CAL Logic) keeps the whole system operating asynchronously.

As the whole system works continuously, it is impossible to suppress offset inaccuracies by using circuit techniques such as auto-zeroing. To solve this problem, an offset calibration DAC (CAL-DAC) and asynchronous calibration logic (CAL Logic) have been introduced to calibrate the offset of the whole system during the reset. The details of the calibration will be discussed in section IV. Furthermore, bias circuits with a regulator and current mirrors were also included in the system. The regulator at the left lower corner outputs the tunable common-mode voltage for the LNA and the I/V converter. The current mirror is also tunable to enable the system adjustment.

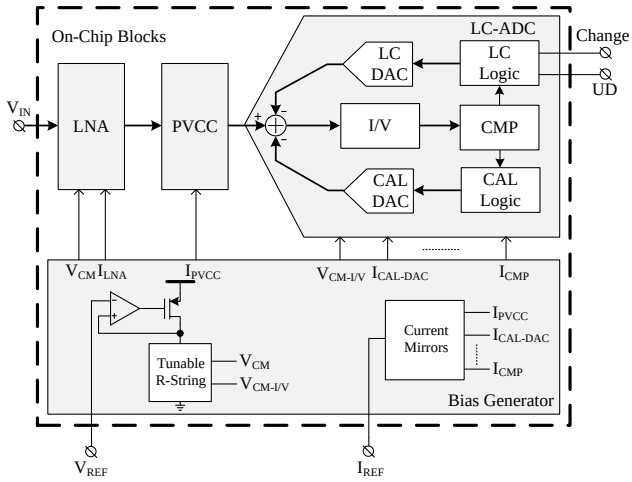


Fig. 2 Block diagram of the propsed ECG recording front-end.

The proposed system benefits from four aspects. Firstly, the current-mode DAC does not have the leakage issue. Secondly, a higher dynamic range is achievable as the signal amplification to the current domain is not limited by the supply voltage. In other words, higher current consumption brings higher dynamic range, which is not possible in the voltage domain. Thirdly, all the currents can be summed at one node and the feedback DAC (LC DAC) and the offset calibration DAC (CAL-DAC) can be easily integrated, resulting in a reduced design complexity. Fourthly, a differential current-to-voltage (I/V) conversion block keeps the comparison window fixed. The common-mode output voltage of the current-to-voltage (I/V) converter determines the common-mode voltage of the comparator and can be easily optimized.

Since the programmable voltage-to-current converter (PVCC) works in class A, a higher biasing current in the PVCC possibly indeed offers larger dynamic range (DR), more phase margin and higher settling accuracy. But the DAC dynamic range and resolution also need to be modified accordingly in order to match the PVCC. So a larger DR can only be achieved at the expense of more power consumption from both the PVCC and the DAC. In this design, given the tradeoff among power consumption, device matching, output swing and distortion, we decided to set the voltage gain of the LNA to 50, and further adjust the gain in the programmable voltage-to-current converter. Considering the power budget and full scale input range of the subsequent LC-ADC, we limited the current swing of the PVCC to 800 nAp-p. Supposing

the ECG amplitude to be 1 mV and the PVCC set at its largest gain, the signal amplitude reaches at most 50 mV and 800 nA after the LNA and the PVCC, respectively. Consequently, we set the transconductance of the PVCC from 2 nA/mV to 16 nA/mV (in four steps), which in turn limits the maximum input voltage range of the PVCC to 400 mVp-p and of the LNA to 8 mV at the lowest gain, respectively.

As higher amplitude resolution for the LC-ADC results in more samples while details are missing if the amplitude resolution is too low [12], an adaptive-resolution algorithm [10] [11] [14] could be beneficial for this work. However, additional bits are needed in the reconstruction to label the resolution for each sample. The adaptive-resolution algorithm can be included in future work if the issue above can be solved. The amplitude resolution of the LC-ADC in this work is fixed to 7 bits.

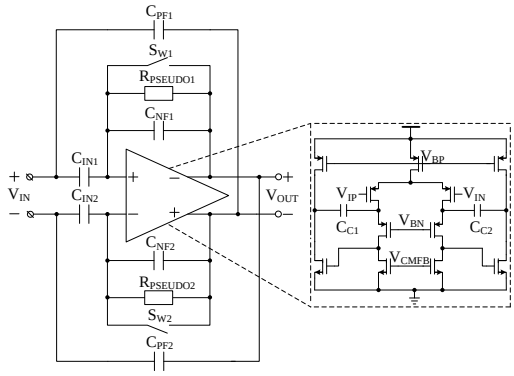


Fig. 3 Block diagram of the LNA

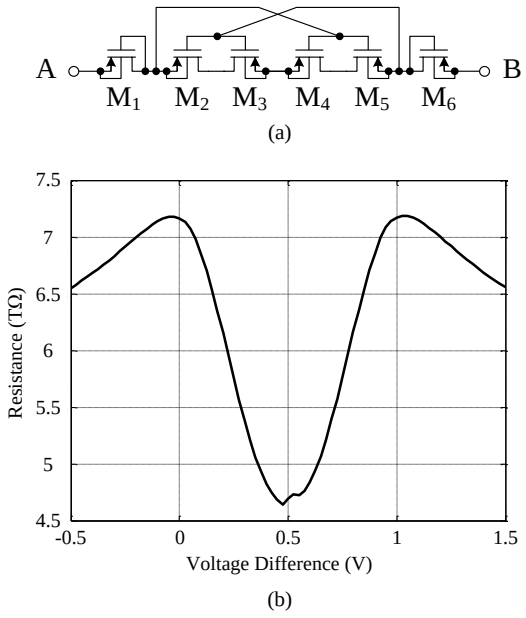


Fig. 4 (a) Circuit diagram of the pseudo-resistor. (b) Simulation results for the DC behavior of the proposed pseudo-resistor.

III. Analog Front-End

A. Low-Noise Amplifier

To reject the DC offset from the skin-electrode contact, the LNA has been configured as an AC-coupled band-pass filter, as shown in Fig. 3. The high-pass cutoff frequency, which is set by the pseudo-resistor $R_{PSEUDO1(2)}$ and the negative feedback capacitor $C_{NF1(2)}$, is given by $1/(2\pi R_{PSEUDO1(2)}C_{NF1(2)})$. The mid-band gain A_V is set by the ratio between the input capacitor $C_{IN1(2)}$ and the negative feedback capacitor $C_{NF1(2)}$ as $C_{IN1(2)}/C_{NF1(2)}$. The low-pass cutoff frequency is dominated by the LNA gain (A_V), the transconductance (gm) of the input pair and the compensation capacitor ($C_{C1(2)}$) and equals $gm/2\pi A_V C_{C1(2)}$. In addition, reset switches $S_{W1(2)}$ have been added to quickly set the input common-mode voltage at the system initialization.

Considering the trade-off among noise, device matching, area, power and input impedance, we set the input capacitor and the negative feedback capacitor to about 20 pF and 400 fF, respectively. To increase the input impedance, a positive feedback loop [18] was introduced in this work. The positive feedback capacitor ($C_{PF1(2)}$) has been given the same value as $C_{NF1(2)}$. The input impedance, after applying the positive feedback loop, can be expressed by

$$Z_{in} = \frac{V_{in}}{I_{in}-I_{pf}} = \frac{A_V}{sC_{IN1(2)}} \quad (1)$$

where V_{in} is the input voltage, I_{in} is the input current and I_{pf} is the current from the positive feedback loop. So the input impedance is boosted by a factor of A_V. In reality, any parasitic capacitance from the source degrades the boost factor [18].

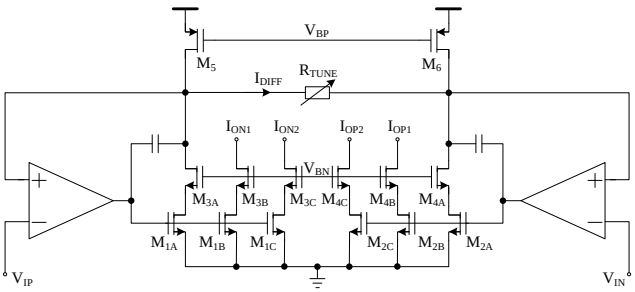
There are three major noise contributors in the LNA: the OTA, the pseudo-resistor and the positive feedback loop. The latter two noise sources can be neglected since: 1) the noise generated by the pseudo-resistor has very limited bandwidth from DC to the high-pass cutoff frequency of the LNA [25]; 2) the resistance (electrode contact resistance) seen from the LNA input is several orders of magnitude smaller than the positive feedback capacitor. The input referred noise of the LNA can be expressed by

$$\overline{V_{in,LNA}^2} = \overline{V_{n,OTA}^2} \cdot (1 + \frac{C_{NF1(2)}}{C_{IN1(2)}})^2 \quad (2)$$

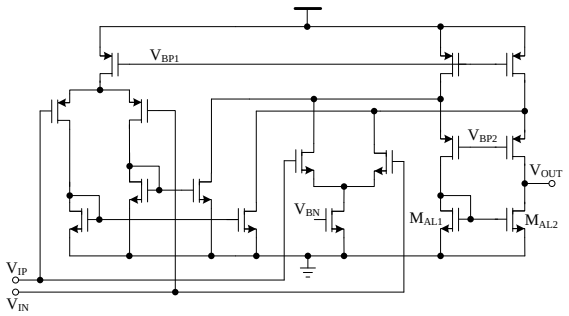
where $V_{n,OTA}^2$ is the input referred noise of the OTA. A similar analysis can also be found in [26]. So the noise of the LNA is dominated by the noise of the OTA, as expected.

A fully differential two-stage low-noise operational amplifier with cascode compensation [19] was used to implement the opamp (Fig. 3). To minimize the noise, pMOS transistors with large areas (160 µm / 6 µm) were employed for the input pair. Each input branch is biased with a current of 225 nA. We set the low-pass cutoff frequency to around 1 kHz, which is enough for the band of interest in the ECG recording application at hand.

Pseudo-resistors bias the input pair at a proper voltage level and determine the high-pass cutoff frequency. Such resistors are usually the bottleneck to improve the linearity performance in biomedical amplifiers. To set the high-pass cutoff frequency to tens of mHz, a resistance in the order of 10^{12} to 10^{13} ohm is necessary. Conventional pseudo-resistors [20] do not show a



(a)



(b)

Fig. 5 (a) Circuit diagram of the V-I convertor. (b) OTA used in the V-I convertor.

symmetrical characteristic when we sweep the voltage on both terminals. Also the resistance varies at least one order of magnitude. All these effects result in distortion in the LNA.

In this work, we propose a balanced pseudo-resistor structure as shown in Fig. 4 (a). To guarantee that the high-pass cutoff frequency is low enough, medium-voltage pMOS transistors were adopted. The simulated resistance behavior of the pseudo-resistor is presented in Fig. 4 (b). M_1 (M_6) is connected as a diode to generate a voltage drop from both terminals. The inner source-bulk connected pairs M_2 and M_3 (M_4 and M_5) are in series and their gates are controlled by the drain voltage of opposite outer transistor M_6 (M_1). From A to B, or equally from B to A, there are always three drain-coupled pMOS transistors (M_3, M_5 and M_6) and three source-coupled pMOS transistors (M_1, M_2 and M_4). Consequently, a fully balanced structure from both sides of the pseudo-resistor is obtained. For the simulation, we fixed one terminal (A) to 0.5 V and swept the voltage of the other terminal (B) from -0.5 V to 1.5 V. Fig. 4 (b) shows a desirable symmetry in resistance (from 4.5 TΩ to 7.5 TΩ).

B. Programmable Voltage-to-Current Converter

In conventional voltage-mode systems, a PGA follows the LNA to adjust the gain and drive the subsequent ADC. Since the LC-ADC in this work operates in the current domain, we propose a voltage-to-current (V/I) converter with a tunable resistor string to perform the same function. The voltage-to-current conversion requires the following characteristics: 1) the converter should work from a low-voltage supply (1V); 2) the V/I conversion ratio should be digitally controllable; 3) the current after conversion should be easily copied.

The circuit diagram of the V/I converter is shown in Fig. 5(a). The differential input voltage (V_{IP},V_{IN}) is connected to the negative inputs of the operational transconductance amplifiers (OTA). These OTAs are used to further boost the gain of the two loops, respectively. The feedback loop formed by the OTA, M_{1A}(M_{2A}) and M_{3A}(M_{4A}) forces the positive terminal to follow the differential input (V_{IP}, V_{IN}) with a loop gain of $A_V g_{m1} g_{m3} r_{o1} r_{o3}$. The differential voltage drops across the tunable resistor R_{TUNE} and generates the current I_{diff}, which can be expressed by

$$I_{diff} = \frac{(V_{ip}-V_{in})\times(\frac{A_V g_{m1} g_{m3} r_{o1} r_{o3}}{1+A_V g_{m1} g_{m3} r_{o1} r_{o3}})}{R_{TUNE}} \approx \frac{(V_{ip}-V_{in})}{R_{TUNE}} \quad (3)$$

where $g_{m1(3)}$ is the transconductance of the transistor $M_{1A(3A)}$, $r_{o1(3)}$ is the output resistance of the transistor $M_{1A(3A)}$ and AV denotes the open-loop gain of the OTA (Fig. 5 (b)). R_{TUNE} is a resistor string with switches controlled by the digital logic. The resistance of R_{TUNE} defines the transconductance of the V/I converter. The output current after conversion is obtained by copying current from the loop ($M_{1B(C)}$ copy the current from M_{1A}). Since the output stage is not in the feedback loop, its output impedance is roughly $g_{m3} r_{o1} r_{o3}$. A similar analysis applies for the other half of the differential PVCC.

As shown in Fig. 5(a), M_5 and M_6 provide the biasing current for the converter. M_{1A} and M_{2A} are acting as common-source stages and cascoded by M_{3A} and M_{4A} to increase the loop gain. The tunable resistor R_{TUNE} is tuned by two digital bits. The resistance can be set to 175 kΩ, 350 kΩ, 700 kΩ and 1400 kΩ. So the largest transconductance is 8 times larger than the smallest one. The resistance from the feedback loop (approximately $g_{m3} r_{o1} r_{o3} / A_V g_{m1} g_{m3} r_{o1} r_{o3}$) is much smaller than the one from $M_{5(6)}$ and R_{TUNE} thanks to the feedback. Note that a higher transconductance can be set at the expense of a larger current consumption and distortion. Finally, $M_{1B(C)}$ and $M_{2B(C)}$ copy the converted current for the subsequent level-crossing ADC. In this work, the resistor is connected at the drain of the transistors. Therefore, the consumed headroom is minimized while voltage and current swing are maximized. Also, the converted current is easily copied and combined with the following stage, resulting in a flexible design.

The circuit diagram of the OTA used in the PVCC is shown in Fig. 5(b). Although the gain of the LNA in the previous stage is relatively low (34dB), a rail-to-rail input stage of the OTA is still necessary to guarantee the linearity of the conversion under the low-voltage supply. So a folded cascode amplifier with both pMOS and the nMOS input pairs has been designed. To match and bias the common-source amplifier ($M_{1A(B,C)}$ and $M_{2A(B,C)}$) at the output of the OTA properly, the active load (M_{AL1} and M_{AL2} in Fig. 5(b)) is not cascoded. The OTA is driving the gate of the nMOS transistor only, and the current consumption of the OTA is also preferably low to maintain the feedback loop stable, so each OTA here consumes a current of about 120nA.

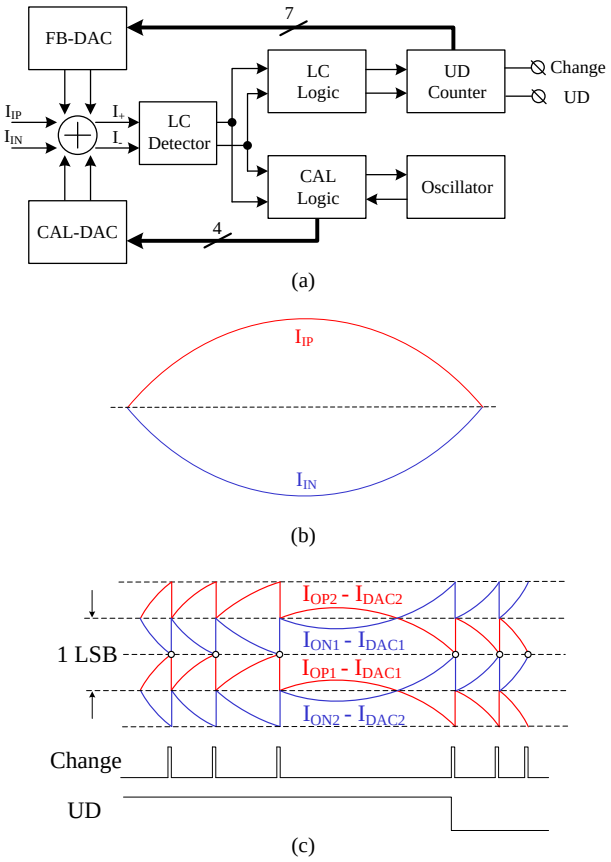


Fig. 6 (a) Block diagram of the proposed LC-ADC. (b) Example input signal. (c) Level-crossing waveforms.

IV. Level-crossing ADC

The block diagram of the proposed LC-ADC is shown in Fig. 6 (a). Only one side is shown for clarity. The details of all the sub-blocks will be introduced in this section.

After the voltage-to-current conversion, I_{IN} (I_{IP}) is fed to the LC-ADC. There are two DACs in the proposed system. The one that is in the feedback loop is called FB-DAC; the other one that is in the calibration loop is called CAL-DAC. FB-DAC performs the addition or the subtraction whenever there is a level-crossing while CAL-DAC calibrates the offset during the system reset. The FB-DAC and the CAL-DAC never operate simultaneously. All the currents are summed at the input node of the level-crossing (LC) detector. The residue current is then compared by the LC detector. During the system reset, the LC logic, the up/down (UD) counter and the FB-DAC are resetting and the CAL DAC is triggered by the CAL logic and the oscillator to minimize the offset current. The calibration bits are stored in the registers in the CAL logic once the reset has been done, and then the FB-DAC starts to work. The working principle of the multi-bit LC-ADCs can be found in [7][11]. Example waveforms illustrating the working principle of the proposed LC-ADC with the FB-DAC are shown in Fig. 6 (b) and (c). The UD counter functions as a digital integrator. The feedback loop forces the output of the FB-DAC to track the input signal (I_{IN} or I_{IP}) and to inject the offset current to the input, resulting in residue currents ($I_{ON1(2)}$ - $I_{DACN1(2)}$ and $I_{OP1(2)}$ - $I_{DACP1(2)}$). Whenever the two differential residue currents cross each other, the output of the LC detector toggles and the LC logic at the next stage starts to update the UD counter. The FB-DAC injects the offset current and the LC-ADC continues to track the input signal, being ready for the next crossing.

A. Segmented current DAC

For the tradeoff between accuracy and design complexity, the 7-bit DAC is segmented into a 3-bit thermometer-decoded MSB array and a 4-bit binary-weighted LSB array. The system diagram of the segmented current DAC is shown in Fig. 7(a). A delay is inserted in front of the LSB array to minimize glitches at the output.

Due to the low voltage supply, the current cell used in both arrays of the DAC was designed with a single-transistor current source (M_1) and a switching transistor pair (M_2, M_3) as is shown in Fig.7 (b). Since the interested signal band for ECG signals is below 500Hz, the speed and settling time are not an issue in this design. The driving circuit is composed of M_4-M_7 (M_8-M_{11}). M_5 and M_6 (M_9 and M_{10}) limit the output swing and reduce the clock feed through from the previous stage. Consequently, transistors M_2 and M_3 operate in the saturation region and a cascode configuration is formed. Therefore, the output impedance of the current cell is enhanced.

B. Level-crossing detector

The residue current from both the PVCC and the DACs are summed at the input node (I_+, I_-) of the level-crossing detector. The current is converted into a voltage and, the comparator outputs a logic high or low. The level-crossing detector is shown in Fig. 8(a). It consists of a differential

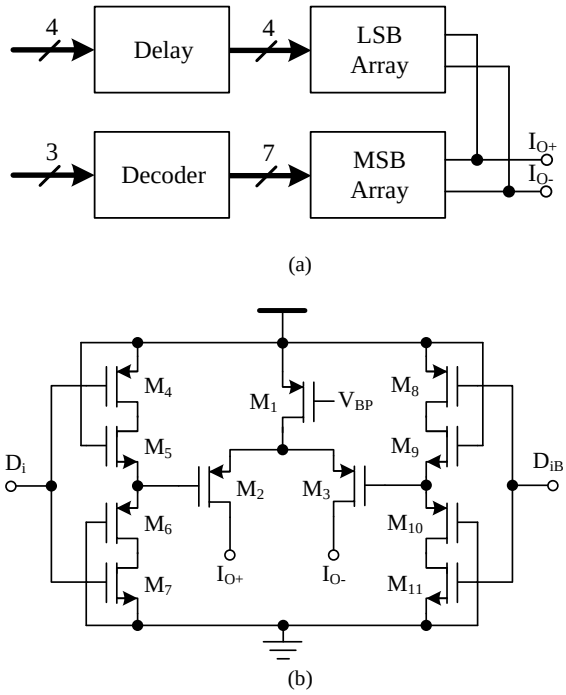


Fig. 7 (a) Block diagram of the current DAC. (b) Circuit diagram of the current cell.

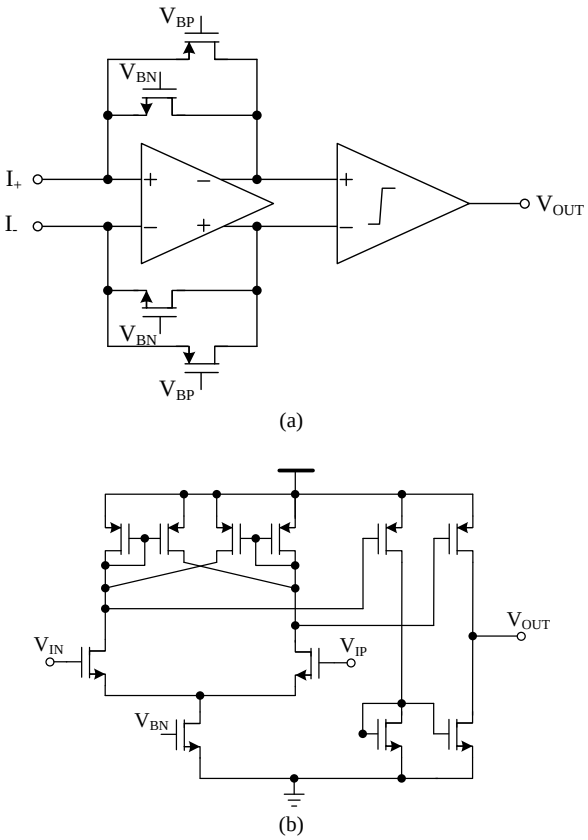


Fig. 8 (a) Level-crossing detector with an I/V convertor as the first stage and a comparator as the second stage. (b) Circuit diagram of the comparator.

current-to-voltage (I/V) converter and a voltage comparator. The I/V converter is similar to the current comparator in [21], but designed with a single-stage fully differential amplifier.

As the outputs of the PVCC and the DAC are both current mirrors, the PVCC and the DAC output CM voltage is preferably fixed at a favorable biasing point. This is critical for the continuous-time operation and tracking accuracy. A simple current comparator with open-loop operation does not suffice to quickly stabilize the CM voltage of the current summation node when the input current (I+, I-) varies. More complicated current comparators always have internal feedback (negative or positive) to either sense the small current difference or speed up the comparison. Furthermre, these current comparators always have a non-linear (e.g. log-domain) I-V conversion and output their high and low values in terms of voltage.

In this work, the I/V converter utilizes both pMOS transistors and nMOS transistors in the feedback loop to achieve symmetrical performance for current sourcing and sinking. The pMOS transistors and nMOS transistors are biased in the subthreshold region. They exhibit large resistances when the input is at the optimum common-mode voltage level and small resistances when the input is not at the optimum level. A desirable nonlinear transresistance is thus obtained. A small input current difference is converted into a relatively large voltage difference. In level-crossing ADC, this is a favorable situation as the input current difference is always within 1 LSB.

Consequently, the use of the non-linear resistances of the

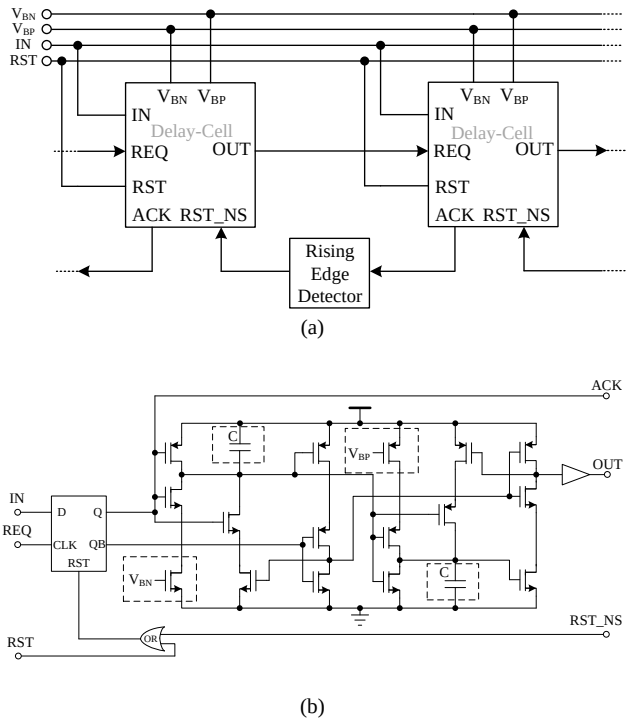


Fig. 9 (a) Delay chain used in the asynchronous logic control. (b) Circuit diagram of the delay cell.

MOSFETs (the ones biased by V_{BN} and V_{BP} in Fig. 8 (a)) in the I-V convertor offers two advantages: 1) a high-resistance path to sense and convert a small input current into a large voltage; 2) a low-resistance path (via either the nMOS or pMOS) to stabilize the CM voltage of the current summation node when the voltage there deviates from its favorable biasing condition for the PVCC and the DAC. So the I-V convertor stabilizes CM voltage and buffers the current summation node for the following voltage comparator.

The voltage comparator is depicted in Fig. 8 (b). To improve the noise robustness, hysteresis has been added to the comparator by means of the cross-coupled pMOS current mirrors.

C. Delay cell in the asynchronous logic

In the level-crossing ADC, the whole system is based on an asynchronous hand-shake protocol highly relying on delay, so a delay cell for the hand-shake operation is vital for the system operation. The asynchronous logic used is modified from the one in [7]. We only discuss the delay here.

The diagram of the delay is shown in Fig. 9(a). The circuit diagram of a single delay cell is presented in Fig. 9(b). All the current sources in the delay cell share the same biasing voltages V_{BN} and V_{BP}. IN is the signal from the asynchronous logic control, and it can be considered as an enable signal. IN equals "0" means there is no level crossing. Otherwise, the delay cell is enabled to transmit a "1" from the previous cell to the REQ of the next cell. Once the "1" is acquired from the next cell, ACK together with the rising edge detector (RED) generate a "1" to RST_NS to reset the previous cell.

The delay cell in [22] is based on a structure called thyristor

[23]. The advantages of such a delay cell include low-voltage operation, no static current consumption and that the pulse width is not related to the delay time. The delay cell in [22] has only an nMOS transistor based thyristor. In this design, we added an pMOS transistor based thyristor in cascade to further improve the robustness. The detailed working principle of each thyristor based delay element can be found in [22]. The delay time is defined by the delay capacitor C and the current source in the dashed box.

D. Offset calibration

A simplified block diagram of the offset calibration is shown in Fig. 10(a). Different from the asynchronous logic control based on a delay chain in the feedback loop, the offset calibration control here utilizes an oscillator. The calibration DAC circuit itself here is the same as the 4-bit binary-weighted DAC in the feedback loop.

An example waveform of the digital control logic for offset calibration is shown in Fig. 10(b). At the system reset, the rising edge detector (RED) generates a pulse to reset all the blocks. The logic control block then outputs an enable signal to activate the oscillator, which starts to generate pulses. The comparator output controls the up/down counter to count up (or down) to decrease the voltage difference at the input of the comparator.

There are two possible conditions during the calibration: 1) the offset is within the calibration range; or 2) the offset exceeds the calibration range. The first case results in comparator toggling while the latter one causes data overflow of the up/down counter. In both cases, the logic control can detect either the toggling pulses from the comparator or the data overflow (OVF) pulses from the up/down counter. Example waveforms of the signal at the input of the comparator (V_{IP},V_{IN}) and the finishing pulse for calibration are shown in Fig. 10(c). Dotted lines are used to indicate the repeated cycles. The comparator toggling (or data overflow) generates a finishing pulse to trigger the shift registers in the control logic to count. The length of the shift registers determines the number of repeated cycles. To make the calibration more robust, the number of repeated cycles was set to 16. The control logic disables the oscillator output after the repeated number of cycles reaches 16.

The LSB current in the CAL-DAC determines the minimum distinguishable offset. A larger CAL-DAC dynamic range gives a larger calibration dynamic range. So for a fixed resolution (4-bit in our case), there is a trade-off between the calibration range and the minimum distinguishable offset. For more calibration bits (> 4 bits), the calibration range and the minimum offset can be both improved but more area and parasitic capacitance will be added.

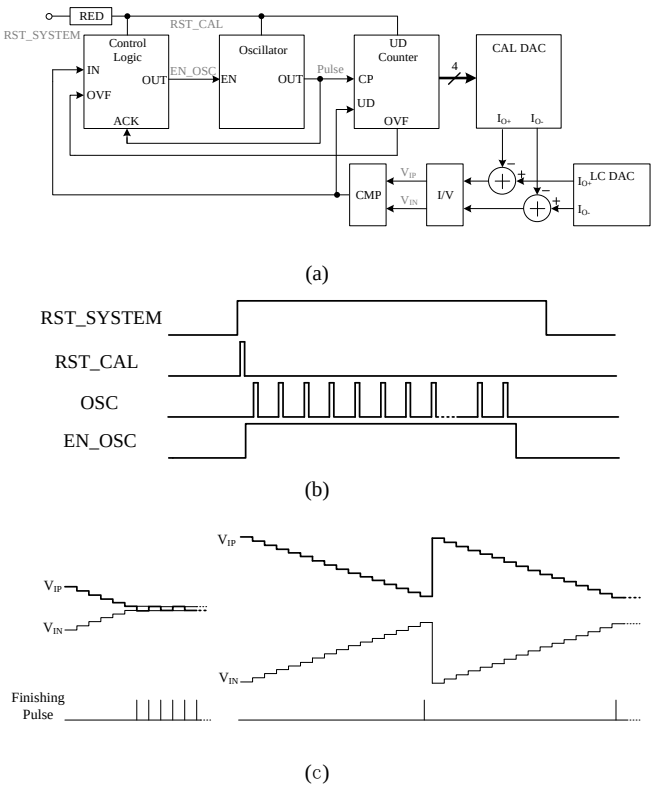


Fig. 10 (a) Simplified block diagram of the offset calibration. RED denotes the rising edge detector. (b) Example waveform of the digtal logic control. (c) Example waveform of the signal at the comparator input. The left one depicts that the offset is within the calibration range while the right one means the offset exceeds the range. Repeated cycles are ignored and depicted by the dotted line to clarify the waveform.

V. MEASUREMENTS

The proposed ECG recording front-end has been implemented in a 0.18 μm CMOS technology. The active area is approximately 690×710 μm^2. A microphotograph of the chip is shown in Fig. 11. The supply voltage was set to 1 V for all the measurements.

The measured frequency response of the LNA is shown in

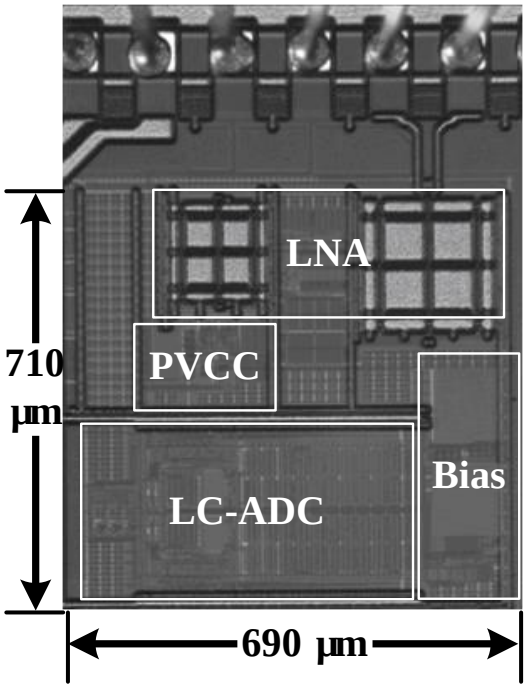


Fig. 11 Die microphotograph of the ECG readout front-end implemented in a 0.18 μm CMOS process. The core area is 690×710 μm^2.

Fig. 12. The high-pass cutoff frequency is around 60 mHz while the low-pass cutoff frequency is approximately 950 Hz. The low-pass cutoff frequency can be further adjusted by external capacitors to reject more noise, as the band of interest for ECG application is up to 500 Hz.

Fig. 13 shows the measured input-referred noise power spectrum density (PSD) of the LNA. The input-referred noise integrated from 60 mHz to 950 Hz results in 3.77 μV_{rms}. The noise efficiency factor (NEF) introduced in [24] quantifies the tradeoff among power, noise and bandwidth and is defined by:

$$NEF = V_{rms,in}\sqrt{\frac{2*I_{tot}}{\pi*V_T*4kT*BW}} \quad (4)$$

where $V_{rms,in}$ is the input-referred rms noise voltage, I_{tot} is the total current consumption of the amplifier, and BW is the amplifier bandwidth. The LNA in this work achieves an NEF of 4. In biomedical applications where signal fidelity is important, the THD performance is also critical. Although the maximum input-referred range of the system is 8 mV_{PP}, we applied input sinusoidal signal amplitudes up to 10 mV_{PP} to check the performance of the LNA. The THD at 10mV_{pp} input is 0.15%, which is good enough for the targeted system resolution. The measured THD in turn verifies the performance of the proposed fully balanced pseudo-resistor.

Due to the limited number of pads, we did not leave test pads for measuring the LC-ADC alone in this work. Furthermore, designing an off-chip current driver complicates the measurements. So the test signals for the LC-ADC are always from the output of the LNA and the PVCC. In other words, the SNDR we obtained from the LC-ADC output is the SNDR of the whole system. In line with previous works [12][15], a logic

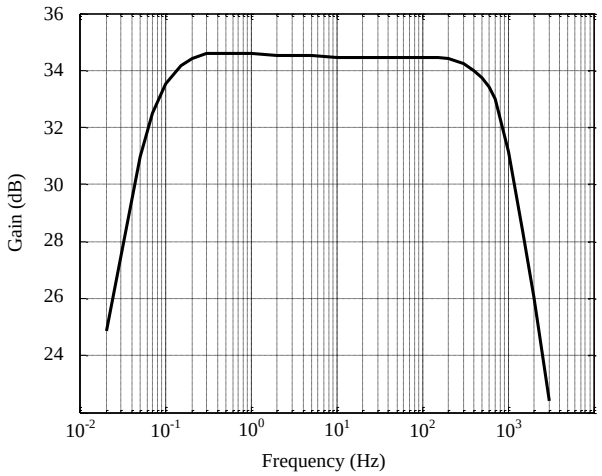


Fig. 12 Gain-bandwidth measurement of the LNA. The high-pass cutoff frequency is around 60 mHz while the low-pass frequency is approximately 950Hz.

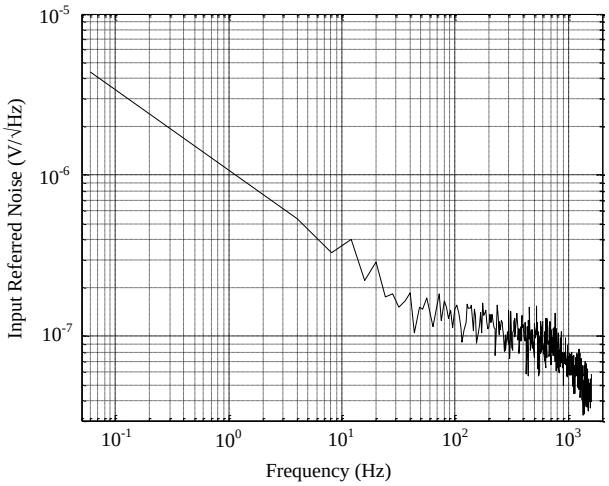


Fig. 13 Measured input-referred noise voltage PSD of the LNA. Four-time averaging was used during the measurement.

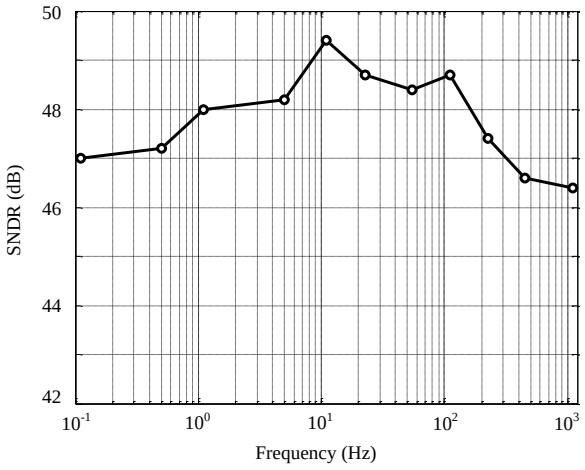


Fig. 14 SNDR as a function of the input frequency ranging from 0.11 Hz to 1.1 kHz for a 6 mV_{PP} input signal. 5th order polynomial interpolation was used to reconstruct synchronous signals to calculate the SNDR by means of a standard FFT. The timer was adjusted to work from 5 kS/s to 5 MS/s (the oversampling ratios are between 980 and 4545) for the entire input frequency range from 0.11 Hz to 1.1 kHz.

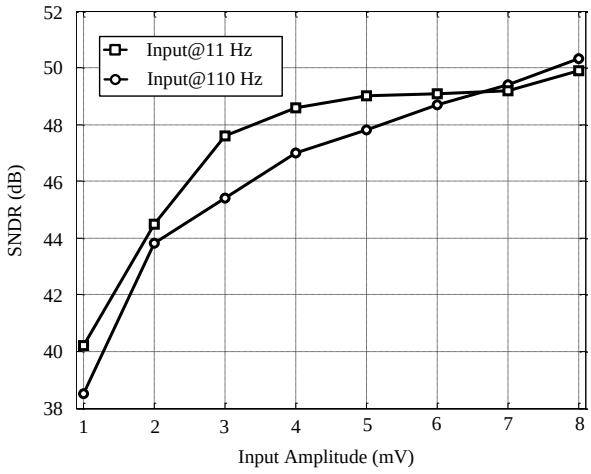


Fig. 15 SNDR for input amplitudes ranging from 1 mV to 8 mV for input frequencies of 110Hz and 11 Hz, respectively. The timer was set to 500 kHz and 50 kHz for 110 Hz and 11 Hz, respectively.

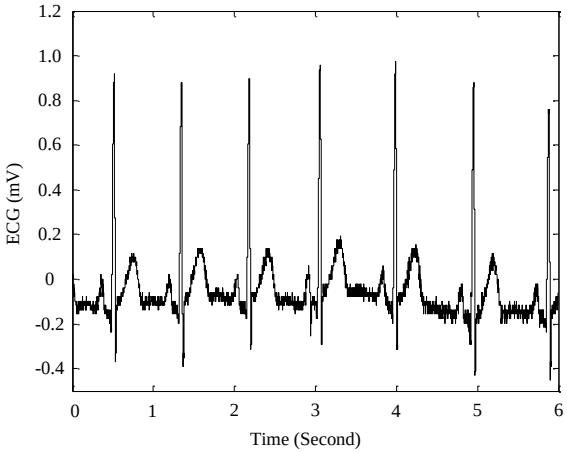


Fig. 16 Example of a recorded ECG after reconstruction from the acquired digital signal. ECG is extracted by connecting two electrodes to the backside of the subject's hands and setting the transconductance of the PVCC to 8 nA/mV (R_{TUNE} = 350 kΩ).

TABLE I
PERFORMANCE SUMMARY OF THE SYSTEM

Parameter	Value
Technology	0.18 µm
Supply Voltage	1 V
LNA Voltage Gain	34 dB
LNA Input-Referred Noise	3.77 μV_{RMS} (60 mHz-950 Hz)
LNA NEF	4
LNA THD	0.15 % @ 10 mV_{PP} input
LNA CMRR	67dB (@ 50 Hz)
PVCC Transconductance	2/4/8/16 nA/mV
ADC SNDR	46.4 - 50.2 dB
Total Power	8.49 µW@1kHz, 8 mV_{PP}
Chip Area	690 ×710 μm^2

analyzer was used in the measurements to count the time in between the asynchronous samples. Signal reconstruction and interpolation were performed in MATLAB utilizing polynomial interpolation. A 5^{th} order polynomial interpolator was used throughout all the measurements. The SNDR as a function of the input frequency ranging from 0.11 Hz to 1.1 kHz for a 6 mV_{PP} input sinusoid signal has been tested and is shown in Fig. 14. The timer was adjusted to work from 5 kS/s to 5 MS/s (the oversampling ratios are between 980 and 4545) for the entire input frequency ranging from 0.11 Hz to 1.1 kHz.

The measured SNDR as a function of the input signal dynamic range is shown in Fig. 15 for a 110 Hz and a 11 Hz sinusoidal signal. The logic analyzer was set at 500 kS/s and 50 kS/s for the 110 Hz and the 11 Hz input signals, respectively. The input signal range at the input of the LNA was from 1 mV to 8 mV.

We also applied the fabricated chip to record the ECG signal from a human volunteer to verify the function. A typical three-electrode measurement was performed. The reference electrode was at the right leg of the subject, the other two electrodes were at the back side of the subject's hands and connected to the differential input of the LNA. The transconductance of the PVCC was set to its second largest one (8 nA/mV). The acquired digital data after reconstruction is shown in Fig. 16.

The performance of the proposed system is summarized in Table I. The system achieves better performance than another LC sampling based readout system [13]. The LC sampling system is not yet comparable to standard approaches ([16] [17] [27] [28]) in terms of power. However, the system has some other advantages that conventional systems are not able to offer. The LC sampling system generates fewer samples [10] - [14] and thus holds the potential to consume less power in wireless transmission, data storage and computation. Furthermore, the current swing of the current-mode system is not limited by the supply voltage, thus offering larger dynamic range than the voltage-mode system in a low-voltage supply environment. Future work may focus on integration into a wireless system. Processing the data locally for feature extraction (QRS detection [29] [30]) could also be promising.

VI. CONCLUSION

An ECG recording system with level-crossing sampling has been presented in this paper. A voltage and current mixed-mode system is proposed. The LNA with a fully balanced pseudo-resistor guarantees a good linearity. Resolving the input signal further in the current domain allows for large dynamic range applications while operating from a low-voltage supply, avoids leakage and offers more design flexibility. The use of a current feedback DAC eases the integration of calibration blocks in the continuous-time domain. The circuit has been designed and fabricated in a 0.18 µm CMOS technology. The proposed system is also very suitable for other biomedical applications where the signals are sparse.

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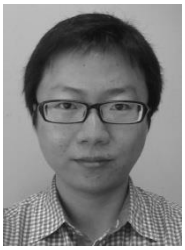

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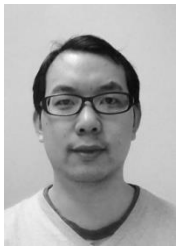

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