# A Sub-Microwatt Asynchronous Level-Crossing ADC for Biomedical Applications

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***Abstract*—A continuous-time level-crossing analog-to-digital converter (LC-ADC) for biomedical applications is presented. When compared to uniform-sampling (US) ADCs LC-ADCs generate fewer samples for various sparse biomedical signals. Lower power consumption and reduced design complexity with respect to conventional LC-ADCs are achieved due to 1) replacing the n-bit digital-to-analog converter (DAC) with a 1-bit DAC; 2) splitting the level-crossing detections; 3) fixing the comparison window. Designed and implemented in 0.18 µm CMOS technology, the proposed ADC uses a chip area of 220×203 µm$^2$. Operating from a supply voltage of 0.8 V, the ADC consumes 313 – 582 nW from 5 Hz to 5 kHz and achieves an ENOB up to 7.9 bits.**

***Index Terms*—analog-to-digital conversion, asynchronous ADC, 1-bit DAC, level-crossing ADC, level-crossing sampling, biomedical recording.**

## I. Introduction

ADCs are indispensable blocks in wearable and implantable biomedical data acquisition systems. Conventional ADCs are based on the uniform sampling mechanism, with the sampling frequency determined by the highest expected spectral frequency. Nevertheless, many bio-signals are sparse in the time domain, comprising both long periods of low frequency content and short periods of high frequency information. In this case, uniform sampling constantly generates the samples from the sensed signal at a relatively high rate regardless of the signal variation, resulting in a waste of system energy in data conversion, transmission and storage.

From a technology perspective, in deep-submicron technology, analog design suffers a lot from short-channel transistors with lower output resistance and lower intrinsic gain. At lower supply voltages, the highest achievable signal-to-noise ratio (SNR) and dynamic range (DR) are reduced due to the lower voltage swing. On the other hand, however, digital circuits directly benefit from technology scaling. So processing the signal digitally and employing time-to-digital conversion becomes more advantageous.

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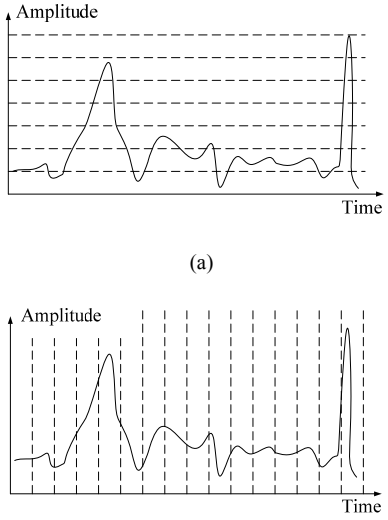



Fig. 1 (a) LC sampling (b) Uniform sampling

A new and promising ADC alternative for biomedical data acquisition is based on so called level-crossing sampling [1], [2]. The principle of a level-crossing (or delta modulation) ADC was originally introduced in 1966 [3]-[5]. Its working principle is similar to that of a flash ADC, but it adopts only two continuous-time comparators. As is shown in Fig. 1, contrary to uniform sampling (Fig. 1(b)), in level-crossing sampling (Fig. 1(a)), samples are generated only when the input signal crosses the threshold levels, while the time in between two consecutive samples is measured by a timer. The conversion results of this LC-ADC are thus composed of digital codes for the voltage magnitude and the time intervals.

Advantages of LC-ADCs include: 1) low-frequency and low-amplitude inputs are sampled less densely in time than high-frequency and high-amplitude inputs. Hence, a much lower average sampling rate is achievable for biomedical applications [2]; 2) the spectrum of the resulting output is alias-free and contains only harmonics of the input signal with no quantization noise floor, so signal-to-noise-plus-distortion ratios (SNDR) of LC-ADCs can exceed the theoretical limit of conventional systems with the same resolution in amplitude [6]-[12]; 3) similar to successive-approximation register (SAR) ADCs, the only analog block is a comparator, whereas the other blocks are digital. The power consumption of digital blocks decreases with technology scaling; 4) only a clock or time-to-digital converter (TDC) is required to count the time for

each sample. Resolution in time benefits from technology scaling; it is even possible to process the non-uniform samples by a continuous-time DSP without a clock [7]; 5) in a LC-ADC, magnitude quantization is replaced with time quantization, which can be more precise when using a low supply voltage; 6) if implemented in a clock-less fashion, LC-ADCs produce lower EMI emission [2], [7], [10], [13], [14]; 7) the digital output of a LC-ADC is continuously available for real time processing, which is different from uniform sampling in the discrete time domain. So the conversion does not need to be triggered by a clock and a faster response to sudden input variations like spikes in biomedical signals or the motion-artifacts in ExG recording [15] can be expected

Some LC-ADCs and their applications have been reported in recent years [6]-[14], [16]. They usually consist of two comparators, an n-bit DAC, an up/down counter, a timer and control logic, as is shown in Fig. 2. But they are still not mature in comparison with their uniform sampling counterparts such as successive-approximation register (SAR) ADCs. Basically, most of the power is consumed by the n-bit DAC and comparators. This is due to that: 1) one or even two n-bit DACs are realized by either resistor strings or capacitor arrays which consume quite some power; 2) in order to guarantee the required short decision time when the common-mode voltage of the comparators moves across the full-scale input range, comparators with adequate performance usually consume a lot of power as comparators adopted in LC-ADCs usually comprise cascades of continuous-time amplifiers.

In this paper we propose a novel way of detecting the level crossings at system level and new structures of the DAC at circuit level. As a consequence, the power consumption of the LC-ADC is reduced dramatically. This work is a follow-up of previous work [17], but proposes a different circuit structure in the DAC and the comparators. More details of the proposed LC-ADC are discussed in the following sections. Based on different biomedical signals, we compare the number of samples generated by LC-ADCs and uniform sampling (US) ADCs in Section II. In Section III, we analyze the possibility of lowering power consumption and propose solutions at system level. Section IV introduces the circuit implementation. Measurements are presented in Section V, followed by the conclusion in Section VI.

## II. Level-crossing sampling of biomedical signals

The block diagram of a conventional LC-ADC is shown in Fig. 2. The comparators operate in the continuous-time domain, the feedback loop forces the comparison window to stay around $V_{IN}$, the up/down counter functions as the digital integrator and the time in between two samples is recorded by the timer. The operation of the conventional LC-ADC was summarized in [6], [7].

In LC-ADCs, conversions are triggered by the signal crossings of predefined levels. In other words, active signals trigger more conversions, and a higher resolution in the amplitude domain results in a higher average sampling rate than in case of a lower resolution in the amplitude domain. In this section, we apply the basic level-crossing algorithm to various

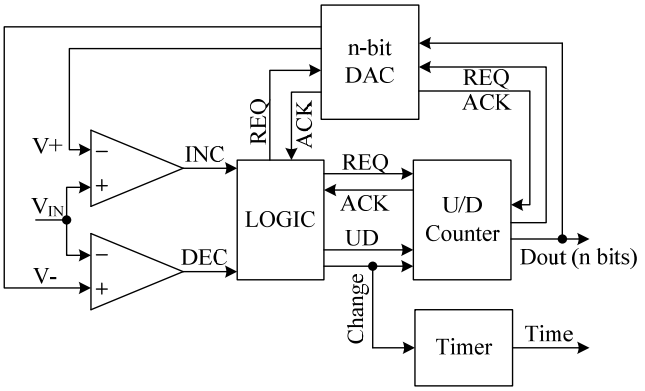



Fig. 2 Block diagram of a conventional LC-ADC

types of biomedical signals in order to analyze the average sampling rate for LC-ADCs for these signals. For resolutions in the amplitude domain varying from 3 bits to 8 bits, the resulting number of samples over a particular simulation time for both the LC system and the US system are compared. The appropriate resolution in the amplitude domain for LC-ADCs in biomedical applications is concluded at the end of this section.

Under the condition that the timer frequency is much higher than the signal frequency and the quantization levels are without any error, ideally, we expect a resolution of LC-ADCs for which it holds that [1], [8]

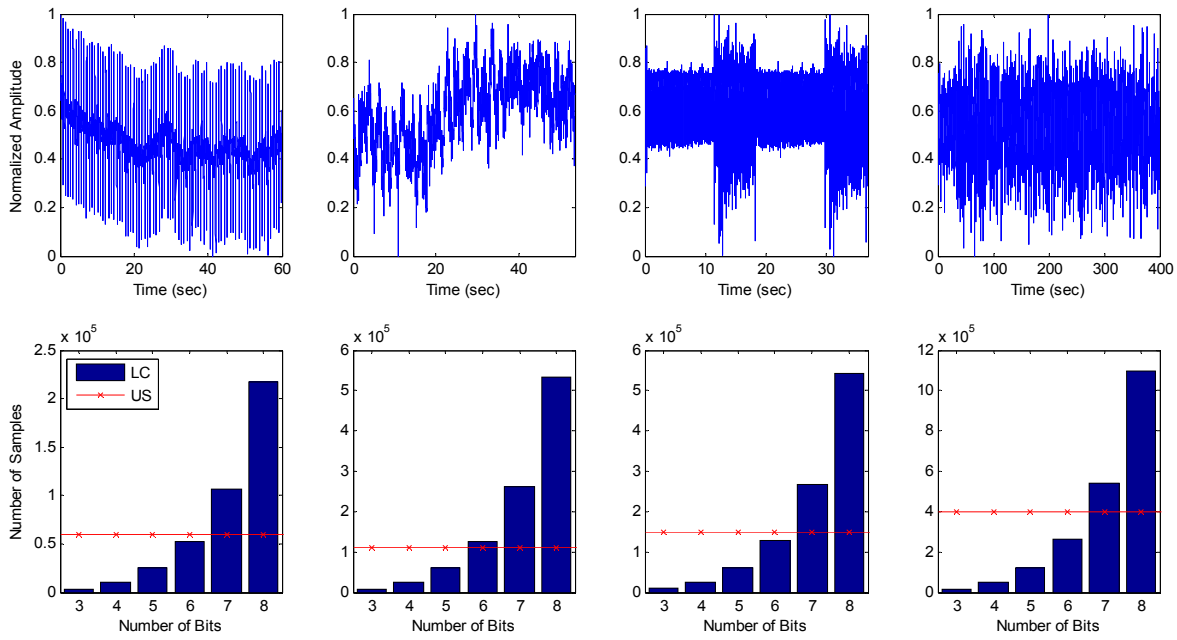
$$SNR = 20\log OSR - 11.2 \quad (1)$$

OSR is the clock oversampling ratio, i.e. the ratio of the timer frequency to the input signal frequency. As opposed to level-crossing sampling, SNR of uniform sampling is expressed as a function of the number of bits $n$ in the amplitude domain and thus

$$SNR = 6.02 \times n + 1.76 \quad (2)$$

Note that the number of quantization levels in amplitude determines the SNR in uniform sampling systems while the OSR in time defines the SNR in LC sampling systems. Detailed analysis of how the time and the amplitude resolution affect the resolution of LC-ADCs can be found in [1], [8], [11]. Indeed, it was shown in some previous works [6]-[11], [13], [14] that with lower resolution in amplitude, LC-ADCs still can exceed the related theoretical limit defined in (2). In other words, in order to obtain n-bit resolution in LC-ADCs, it is not necessary to set the number of quantization levels as $2^n$. It can be $2^{n-1}$ or even lower as long as the OSR of the timer can meet the resolution requirement.

Since LC sampling and uniform sampling are different sampling mechanisms, it is worthwhile to compare the generated number of samples for both of them with the same resolution for the same input signal. Simulations and calculations of different signals in MATLAB were conducted as follows. Typical biomedical signals, for example, ECG [20], [21], EEG [22], [23], ECoG [24] and EMG [25] were chosen for the simulations in MATLAB. The original transient signals were normalized in the range from 0 to 1 V for the sake of clarity.




(a) ECG (b) EEG (c) EMG (d) ECoG

Fig. 3 The normalized input transient signal and the corresponding number of samples for comparison: (a) ECG, (b) EEG, (c) EMG, (d) ECoG. The amplitude of the original signals were normalized for clarity, the number of bits denotes the accuracy in the amplitude domain. "US" denotes uniform sampling while "LC" represents level-crossing sampling.

As the original signals were sampled at particular frequencies (ECG, EEG, EMG, and ECoG were sampled at 1kHz, 2.048kHz, 4kHz and 1kHz, respectively) and thus were not suitable for LC sampling, linear interpolation is used to add more samples to the original signals. OSR in time was set to 1000 to reach the targeted 8-bit overall resolution in this work, so the size of the input signal after interpolation was 1000 times the original one.

In a uniform-sampling system, samples are constantly generated. By multiplying the original sampling frequency $f_s$ and sampling duration we obtain the number of samples. For LC-ADCs, we set the amplitude resolution from 3 to 8 bits to do the comparison with US-ADCs.

The normalized original transient input signals and the number of samples for comparison are depicted in Fig. 3. “US” represents uniform sampling, “LC” means level-crossing sampling. As can be seen from Fig. 3, US and LC sampling reveal two different trends for the generated number of samples when the resolution varies from 3 to 8 bits. As expected, US remains constant for all input signals and all resolutions while LC sampling shows a exponentially rising trend. For the various ExG signals the results are slightly different. Basically, the sparser the signal is, the more the LC-ADC can benefit from that. Furthermore, the number of samples goes up exponentially when the resolution in LC sampling increases. For 8-bit resolution applications, if the amplitude resolution of LC-ADCs is 8 bits, more samples than for US-ADCs are expected according to the bars in the bottom four graphs. Generally, fewer samples are acquired for LC sampling than for uniform sampling for amplitude resolutions lower than 6 bit.

From the discussion above, for the discussed 4 biomedical signals, a resolution of 5-bit or 6-bit in the amplitude domain indeed enables LC-ADCs to generate fewer samples than US-ADCs while maintain higher resolution in time. In this work, we set the comparison window to be 1/64 of full-scale input range, corresponding to 6-bit resolution in the amplitude domain. Introducing an adaptive resolution algorithm or further reducing the amplitude resolution of the LC-ADCs results in even fewer samples, but more details of the signal are lost as well. Further discussions on the relationship between the threshold levels and the obtainable data compression can be found in [10], [11], [13], [26].

## III. Discussion on Conventional Architecture

The power consumption of the previously proposed LC-ADCs [6], [7], [11] is usually ranging from a few to tens of microwastts. In order to investigate the possibility of reducing the power consumption, an analysis from a system level perspective is necessary. Since the power consumption in LC-ADCs is event related, we start with the fluctuation characteristics of the input signal.

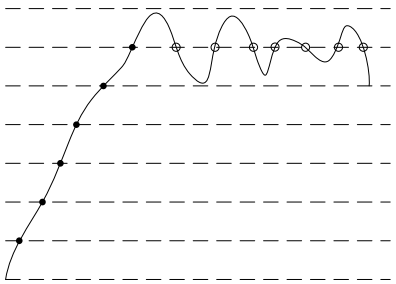


Fig. 4 Different level crossings: consecutive level crossings(CLC; solid dots) and repeated level crossings (RLC; hollow circles)

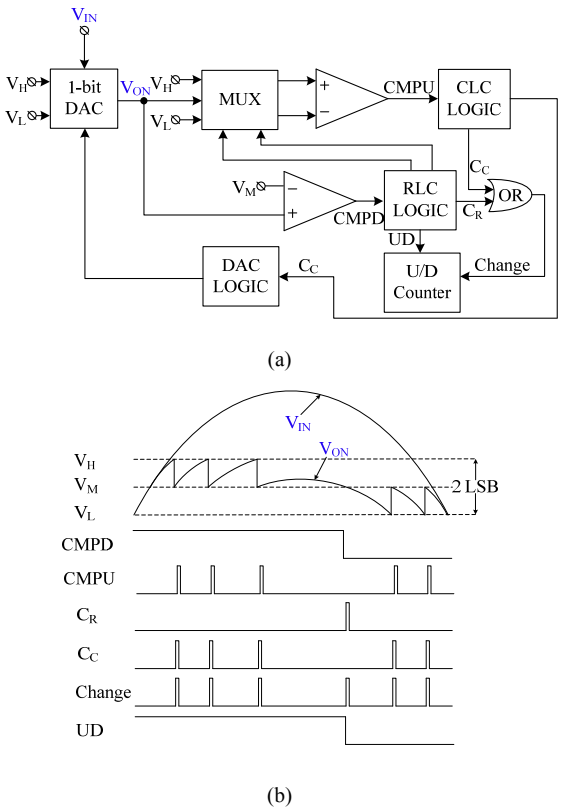



Fig. 5 (a) Block diagram of the proposed structure (b) Example waveforms

First of all, from the input signal side, we assume that any unwanted level crossings due to noise are suppressed by introducing hysteresis in the DACs or the comparators [7], [11] and [16]. Let's assume that the input signal is varying as in Fig. 4. We hereby define two types of level-crossing points: one is called consecutive level crossing (CLC) and represented by solid dots; the signal crosses the upper (or lower) levels consecutively. The other type is named repeated level crossing (RLC) and represented by hollow circles; the signal moves up and down around one level within 2 LSB. Apparently, it is not power efficient to update the whole system if the conversion is triggered by repeated level crossings, as the signal variation is indeed only within 2 LSB.

Secondly, the comparison window between the upper and lower levels in previous works was set by two identical comparators, one of which is always idle in the case of consecutive level crossings. As a result, half of the power consumed by these two comparators is somehow wasted. It is possible to lower the power consumption of the idle comparator or even shut it down, but additional circuits are needed [17].

Thirdly, the up/down counter outputs digital codes, which are then converted by the n-bit DAC to analog voltages to track the input voltage. Nevertheless, the n-bit DAC conveys the delta information of only 1 LSB for each sample. According to the operation of an LC-ADC, a 1 bit DAC should be enough.

Fourthly, the output voltages of the DAC track the input voltage over the full-scale range, which means the operating common-mode voltage of the comparators changes a lot. In order to accommodate this large common-mode voltage range, the comparators need to consume quite some power but input common-mode voltage related offsets still generate different time offsets and hence distortion. Related discussions on how to fix the common-mode voltage can also be found in [11], [13], [17] and [18].

## IV. System and Circuit Implementation

The system structure of the proposed LC-ADC is shown in Fig. 5 (a). An example waveform is depicted in Fig. 5 (b). The comparison window is fixed by introducing a 1 bit DAC with offset injection to the input. The 1 bit DAC tracks the input signal $V_{IN}$, performs subtraction or addition on the tracked input when there is a level crossing, and outputs $V_{ON}$.

The comparison windows of 1 LSB in previous designs are widened to 2 LSB ($V_H$-$V_L$=2 LSB) in this work. $V_M$, $V_H$ and $V_L$ are voltage references. $V_M$ is equal to ($V_H$+$V_L$)/2. The MUX is controlled by the logic output from the lower comparator, which only compares the output of the DAC ($V_{ON}$) with $V_M$. In other words, the lower comparator is only for detecting the varying direction of the signal. The MUX switches between ($V_H$, $V_{ON}$) and ($V_L$, $V_{ON}$), one of which is then compared by the upper comparator. Therefore, the comparison window is now set by $V_M$ and $V_H$ (or $V_L$). Depending on the signal-crossing direction detected by the lower comparator, $V_{ON}$ and $V_H$ (or $V_{ON}$ and $V_L$) are then fed to the input of the upper comparator.

Consequently, adding an analog multiplexer and one more level ($V_M$) allows the two comparators to operate individually while still functioning as a comparison window of 1 LSB. Therefore, level-crossing detection is split, with the upper comparator for consecutive level crossing and the lower comparator for repeated level crossing. For signals with different proportions of RLC to CLC, different power consumptions of the two comparators can be set in order to save power, which will be discussed in the following sub-section.

Furthermore, RLC logic controls the MUX, outputs the up/down signal ("UD" in Fig. 5 (b)) to the up/down counter and the related level-crossing pulse ("$C_R$" in Fig. 5 (b)) due to repeated level crossings. CLC logic controls the DAC logic and outputs a pulse ("$C_C$" in Fig. 5 (b)), which is triggered by consecutive level crossings. "$C_R$" and "$C_C$" are then fed to the input of the logic OR gate to compose "Change" in Fig. 5 (b). Note that repeated level crossings only refresh the up/down counter while consecutive level crossings update the whole system.

### *A. 1 bit DAC*

The main requirement of the DAC for the proposed system is injecting an offset voltage while tracking the continuous-time input. The proposed 1-bit DAC for doing so is shown in Fig. 6(a). The waveforms in Fig. 6(b) depict how the switches operate. Different from the previously published two-branch structure [17], there are three identical branches in the capacitor array. The middle one is for tracking the input while the other two are for positive or negative offset injection (OI). Two capacitors in each branch are connected in series in order to achieve a continuous-time AC-coupled input. nMOS transistors are utilized as switches. Due to the nature of the offset-injection mechanism, any mismatch in capacitors result in offset accumulation, namely, more "$C_C$" in "up" (UD equals "1") than in "down" (UD equals "0") or vice versa. Therefore, a pseudo resistor [19] comprising 4 transistors is introduced to cancel

any unwanted accumulation during offset injection, and also to fix the DC common mode voltage at the output node when the input signal does not vary. In this case, the voltage swing at the output of the DAC is in the order of several mV or tens of mVs at most, so the ultra-high resistance and ultra-low current of the pseudo resistor is suitable to finely tune and compensate for any possible accumulation when there is mismatch in the capacitor array.

The middle branch is connected to the left (or right) branch for normal operation when $V_{ON}$ stays within the comparison window; the right (or left) branch is connected to $V_H$ or $V_L$ (depending on the signal ranging in between $V_L$ and $V_M$ or $V_M$ and $V_H$). Therefore, one of the two OI branches is always charged with the needed predefined voltage. Suppose that $V_{ON}$ crosses $V_H$. The CLC logic thus outputs a "$C_C$" pulse, which is then converted by the DAC logic to control signals $\Phi_1$, $\Phi_2$ and $\Phi_{1L}$ (or $\Phi_{2L}$), injecting negative offset into the capacitor array by charge sharing. Note that $\Phi_{1H}$ and $\Phi_{2H}$ stay low during this phase. As is shown in Fig. 6(b) for the first "$C_C$" pulse, $S_{ML}$ and $S_{RL}$ are switched off first to disconnect the left OI branch from the tracking branch and make the right OI branch ready for charge sharing. After that $S_{MR}$ and $S_{LL}$ are closed to connect the predefined charged right OI branch to the tracking branch and discharge the left OI branch. $V_{ON}$ is thus reset by sharing charge between the tracking branch and the newly connected branch. Due to this, $V_{ON}$ is decreased by 1 LSB. The charging process is similar to the discharging process, but with one of the two OI branches connecting to $V_H$. In the two-branch structure [17], it takes some time for the voltage of the OI branch to settle with enough accuracy before it can be reconnected. Improved from the previous two-branch structure, the settling time requirement of the three-branch is relaxed considerably.

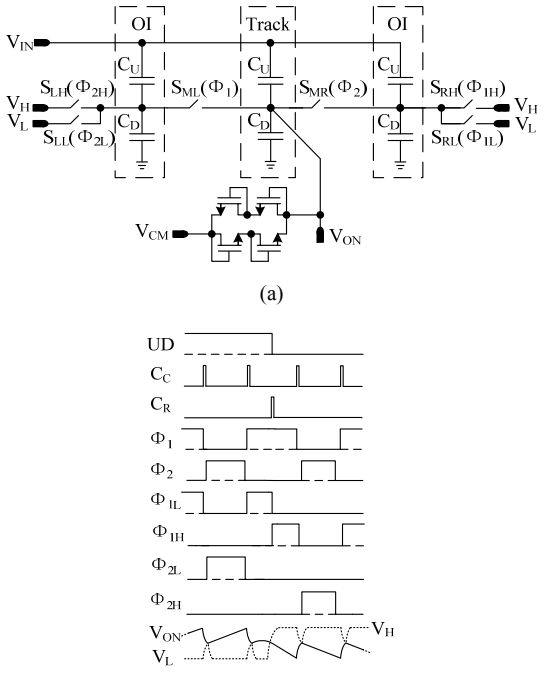



Fig. 6 (a) Proposed 1 bit DAC (b) Example waveforms

$\Phi_1$ and $\Phi_2$ are non-overlapping to avoid directly connecting the tracking branch to the voltage reference $V_H$ or $V_L$. $C_D$ is the unit capacitor while $C_U$ is 14 times larger, so that 14/15 of the input variation falls on the upper plate of $C_D$. Since the settling time of the capacitor array is not related to the resetting time anymore, we have gotten rid of the trade-off between the settling time and the capacitance. Moreover, power consumption of the capacitor array is not a major concern here as the offset voltage injected at each crossing corresponds to 1 LSB. According to the analysis above, we should make the switches as small as possible, while the capacitors are preferably made as large as possible. However, due to the trade-off between accuracy and area, we finally set the lower capacitor to 200fF (for a single branch), which is good enough for our targeted resolution.

The advantages of the proposed 1-bit DAC include: 1) the input voltage range is not limited, as the tracked input voltage is shifted up or down within the comparison window as soon as it reaches the fixed comparator level. In other words, the input signal swing can be higher than in conventional structures and can even exceed the supply voltage rails; 2) there is no information loss during offset injection, unlike the scheme proposed in [18]; 3) the power consumption of the capacitor array is much lower than that of the conventional structure, as a delta voltage step of only 1 LSB per conversion is required.

### *B. Window comparators*

The continuous-time comparator used is shown in Fig. 7. The input stage comprises a PMOS input pair loaded by nMOS diodes. The current from the input stage is amplified by a second and a third stage. All the transistors are operating in subthreshold. The MUX is realized by four switches. Small size transistors were chosen to lower the charge injection.

Considering the two inputs of the upper comparator for the proposed LC-ADC, $V_{IN+}$ is always lower than $V_{IN-}$ when the signal stays in between the comparison window. Therefore, the third stage does not consume static power as the pMOS is shut down by the output of the second stage when there is no level crossing. Only when the $V_{IN+}$ is approaching $V_{IN-}$ the third stage starts to draw current from the power supply.

Although the upper and lower comparators share the same structure, their power consumption is not necessarily equal. Generally, consecutive level crossings happen more often than repeated level crossings. For example, there are only two RLCs in one cycle of any sinusoid signal but a lot more CLCs. Similar results can be found for ExG signals. Therefore, we set the lower comparator in power saving mode while the upper one is set in normal operating mode. In this design, the current consumptions are roughly 135 nA and 270 nA for the lower and the upper comparator, respectively.

Offset may cause inaccuracy in the comparison levels. As the comparators in LC-ADCs work continuously, it is impossible to introduce auto-zeroing. In previous works, offset was compensated by either applying a compensating DC level at the input [7], or DACs to tune the offset [11], [13]. In this work, off-chip voltage references with potentiometers were adopted as reference levels, so the comparator offset could be compensated by tuning the reference levels.

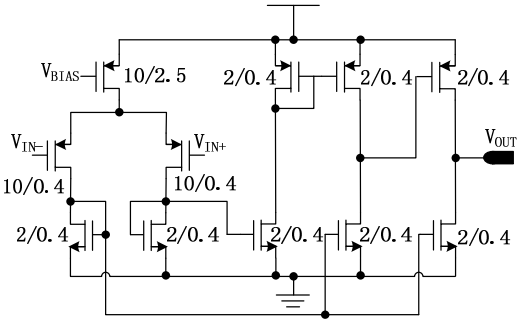



Fig. 7 Three-stage comparator

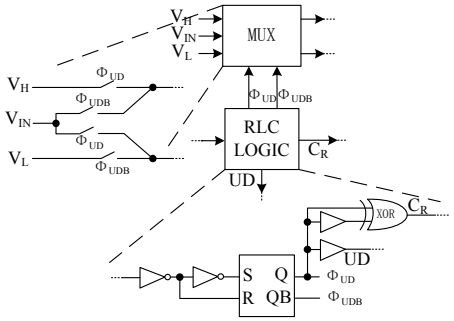



Fig. 8 Detailed circuits of RLC logic and MUX

### C. Digital block

LC-ADCs do not require a clock to trigger the operation of all the blocks, and are instead driven by input voltage variations. The CLC logic block is modified from the one in [7]. Fig. 8 shows the RLC logic block and MUX. Inverters and an RS latch have been added at the output of the comparator to enhance the speed and output swing of its binary output signals. All the switches in the MUX are nMOS transistors, which are controlled by the outputs of the RS latch. Depending on the comparison result from the lower comparator, either $V_{IN}$ and $V_L$ or $V_{IN}$ and $V_H$ pass through the switches. Whenever the input signal crosses the middle level $V_M$, UD changes and the XOR outputs a $C_R$ pulse.

## V. Measurement Results

The proposed LC-ADC has been implemented in AMS 0.18 µm CMOS technology. The active area is approximately 220×203 µm$^2$. The micrograph of the chip is depicted in Fig. 9. The capacitor array dominates the area. The digital supply and analog supply are both 0.8 V. The whole LC-ADC includes all the blocks shown in Fig. 5. The U/D counter was also integrated on chip. A logic analyser was used in the measurements for counting the time. Since level-crossing sampling is non-uniform sampling, in order to use the standard FFT for signal spectrum analysis, signal reconstruction and interpolation were performed in MATLAB utilizing polynomial interpolation. The order of the polynomial interpolation in the reconstruction has only a slight effect on the SNDR, so we varied the reconstruction order from 3$^{rd}$ to 6$^{th}$ for each measurement to find the best SNDR. Different algorithms result in reconstruction accuracy variation. Their effects on accuracy have been investigated and reported in [1], [8], [9]. The measurement results on the prototype and related discussion are presented below.

### A. Accuracy

The dynamic performance of the ADC for an 800 mV$_{PP}$ input signal, its input frequency swept from 5 Hz to 5.1 kHz is shown in Fig. 10. Since the input voltage range is not limited by the voltage reference or even the supply voltage, we can achieve a larger LSB from a higher input swing for a given accuracy. But there is a trade-off between power consumption and performance. In the measurements, 16 mV was chosen for 1 LSB. The same value applies for all measurements conducted unless mentioned otherwise. As the targeted overall resolution in this work is 8-bit, higher oversampling ratios of the timer results in much larger data size and does not improve the performance that much. Therefore, the logic analyser was adjusted to work from 10 kS/s to 5 MS/s for the entire input frequency range from 5 Hz to 5.1 kHz (the oversampling ratios are between 980 and 2440).

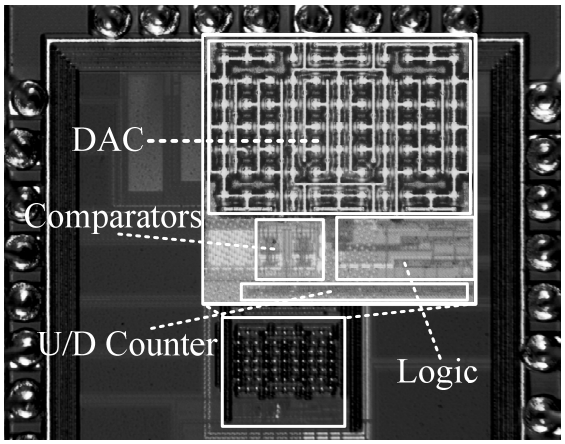



Fig. 9 Chip micrograph

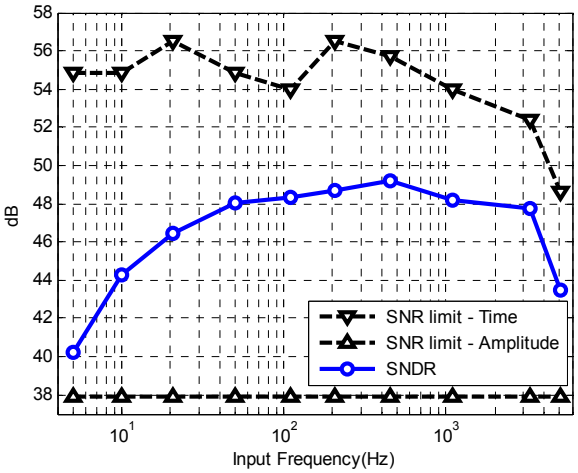



Fig. 10 SNDR as a function of the input frequency ranging from 5 Hz to 5.1 kHz for a 0.8 $V_{PP}$ input signal. 3$^{rd}$ to 6$^{th}$ order polynomial interpolations were used to reconstruct synchronous signals to calculate the SNDR by means of a standard FFT. The timer was adjusted to work from 10 kS/s to 5 MS/s (the oversampling ratios are between 980 and 2440) for the entire input frequency range from 5 Hz to 5.1 kHz while the resolution in the amplitude domain is 6-bit. The theoretical SNR limit due to the finite OSR of the timer and finite amplitude accuracy were also plotted as references.

Note that the varying tendency of the SNDR in this work is different from that of an alias-free LC-ADC [7], [13], [14], in which SNDR rises with input frequency, because there is smaller in-band harmonic distortion as the input frequency increases. As can be seen from Fig. 10, the SNDR decreases due to the leakage when the input frequency goes down to 5 Hz while it degrades at higher input frequencies because of higher harmonic distortion and slope overload. The theoretical SNR limits due to the finite OSR of the timer and finite amplitude accuracy have also been plotted in Fig. 10 as references.

Fig. 11 shows the measured spectrum of the ADC output when the input frequency reaches 5.1 kHz. The logic analyser was set at 5 MS/s and a reconstruction sampling frequency of 102.4 kS/s and 1024 points were used to derive the spectrum. The SNDR degradation is mainly due to offset accumulation and slope overload. The offset accumulation could, in principle, be canceled in the digital domain by high-pass filtering, or be compensated by monitoring the mean value of the output bit stream and adding more "1" or "0" to the digital output, or be solved in a closed loop in the analog domain [27].

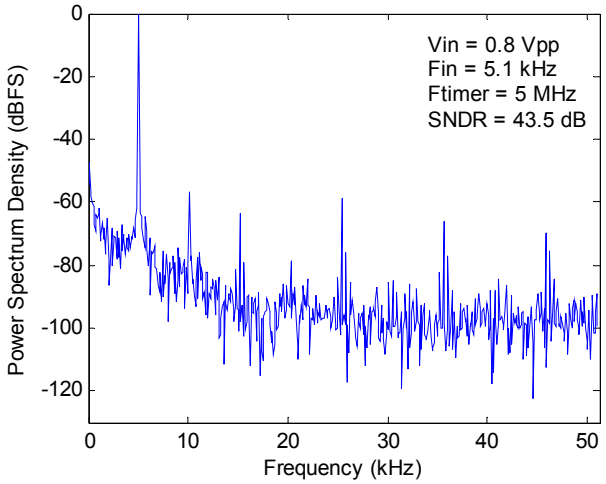



Fig. 11 FFT of the measured ADC output for a 5.1 kHz sinusoidal input, using 1024 points reconstructed at 102.4 kS/s. A 3rd order polynomial interpolator was used to reconstruct the signal.

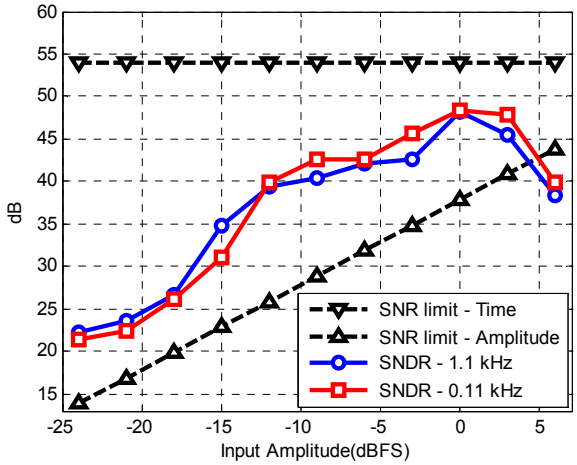



Fig. 12 SNDR for input amplitude ranging from 50 mV to 1.6 V for input frequencies of 1.1 kHz and 0.11 kHz, respectively. The timer was set to 2 MHz and 200 kHz for 1.1 kHz and 0.11 kHz, respectively.

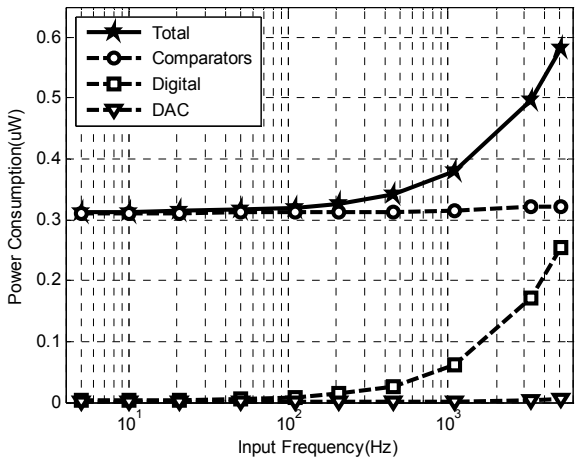



Fig. 13 Power consumption as a function of input frequency ranging from 5 Hz to 5.1 kHz, for a 0.8 $V_{PP}$ input signal.

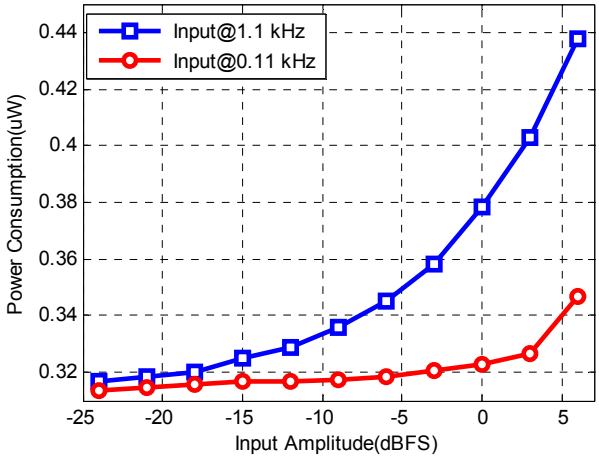



Fig. 14 Power consumption as a function of input amplitude ranging from 50 mV to 1.6 V for input frequencies of 1.1 kHz and 0.11 kHz, respectively.

Since the input operating range of the offset injection based structure is not limited by the power supply, it is interesting to explore the performance of the LC-ADC for input signals that exceed the power supply voltage. A plot of the measured SNDR as a function of the input signal dynamic range is shown in Fig. 12 for a 1.1 kHz and a 0.11 kHz sinusoidal signal. The logic analyser was set at 2 MS/s and 200 kS/s for the 1.1 kHz and the 0.11 kHz input signals, respectively. 0dBFS indicates that the input voltage swing equals the power supply voltage (800 mV). As this design was optimized for an input voltage of 800 $mV_{PP}$, the peak SNDR of the LC-ADC is achieved at 0 dBFS for both cases. When the input amplitude increases up to 1.6 V, slope overload affects the performance and the SNDR drops. Furthermore, as expected, the SNDR decreases with the input amplitude because fewer levels are crossed for an input signal with lower amplitude. Apparently, the capacitor array suffered more from the slower varying signals, which explains the reason why the SNDR of the LC-ADC for 0.11 kHz is slightly lower than for 1.1 kHz. Also, the SNR limits due to the time accuracy and the amplitude accuracy are included as references. In summary, the overall SNDR is higher than the SNR limit in amplitude because of the timer OSR, and the ADC still functions properly when the input exceeds the power supply.

TABLE I
PERFORMANCE SUMMARY

| Parameter | [7] | [11] | [13] | [18] | This Work |
|---|---|---|---|---|---|
| Technology | 90 nm CMOS | 0.18 µm CMOS | 130 nm CMOS | 0.5 µm CMOS | 0.18 µm CMOS |
| Supply Voltage | 1 V | 0.7 V | 0.8 V | 3.3 V | 0.8 V |
| Amplitude Resolution | 8 bits | 4 - 8 bits | 4 - 8 bits | 7 bits | 6 bits |
| Timer Resolution | w/o timer | 1 µs | w/o timer | - | 0.2 to 100 µs |
| Adaptive Resolution | No | Yes | Yes | No | No |
| Automatic Calibration | No | No | Yes | No | No |
| Reconstruction | Test DAC | $6^{th}$ order interpolation in MATLAB | Test DAC | - | $3^{rd}$ to $6^{th}$ order interpolation in MATLAB |
| SNDR | 47 - 62 dB | Peak 43.2 dB | 47 - 54 dB | Peak 34 dB | 40 – 49 dB |
| Input Bandwidth | 200 Hz – 4 kHz | 1 Hz - 1.1 kHz | 20 Hz – 20 kHz | - | 5 Hz – 3.3 kHz |
| Full-Scale Input | 0.5 $V_{PP}$ | 1.4 $V_{PP}$ | 0.72 $V_{PP}$ | 2.68 $V_{PP}$ | 1.6 $V_{PP}$ |
| Power Consumption | 40 µW[a] | 25 µW[b] | 2.6 – 7.4 µW | 10.73 µW[c] | 313 to 582 nW |
| FOM | 4.9-27.3 pJ/conv. | 106 pJ/conv. | 210-880 fJ/conv. | - | 219-565 fJ/conv. |
| Active Area | 0.06 $mm^2$ | 0.96 $mm^2$ | 0.36 $mm^2$ | - | 0.045 $mm^2$ |

a. Static power consumption from the two comparators
b. Without off-chip logic
c. Calculated from the 4-channel static power consumption

### *B. Power consumption*

Fig. 13 and Fig. 14 show the power consumption that has been measured as a function of the input frequency and amplitude, respectively. The measurements were taken under the same condition as held for Fig. 10 and Fig. 12, respectively. The ADC consumes 313 nW and 582 nW for 5 Hz and 5.1 kHz input signals with 800m$V_{PP}$, respectively. The total power consumption of the ADC increases with the input frequency. The comparators' power consumption dominates the static power consumption while the digital circuits and the DAC contribute to most of the dynamic power (see Fig. 13). Similar varying trends can be found in Fig. 14 when the input amplitude changes from 50 mV to 1.6 V.

In order to compare with other previously reported LC-ADCs, the well-known equation for the figure of merit (FOM)

$$FOM = \frac{Power}{2 \cdot BW_{eff} \cdot 2^{ENOB}} \quad (3)$$

is used. The performance of the LC-ADC is summarized and compared in Table I. Compared to other LC-ADCs [7], [11], [13], [18], the proposed LC-ADC achieves comparable performance in FOM to the one reported in [13]. Since on-chip automatic calibration [13] makes the circuit much more autonomous albeit at the expense of consuming additional power and area, for a future implementation, the introduction of a self-calibration loop and reduction of its associated power and area may be considered.

## VI. CONCLUSION

A level-crossing ADC for biomedical applications has been presented in this paper. Innovations at both system level and circuit level pave the way to a low-power operation for the LC-ADC. Distinguishing RLC from CLC allows for independent operation of both comparators, avoids unnecessary updates of all the blocks in the LC-ADC and offers more design flexibility for the comparators. The use of a 1-bit DAC with three branches relaxes the settling time requirement. The circuit has been designed and fabricated in AMS 0.18 µm CMOS IC technology. Lower power consumption and less design complexity have been achieved due to the proposed topology. The event-driven nature makes the proposed ADC very suitable for biomedical applications.

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## REFERENCES

[1] N. Sayiner, H. V. Sorensen, and T.R.Viswanathan, "A level-crossing sampling scheme for A/D conversion," *IEEE Trans. Circuits Syst. II*, vol. 43, no.4, pp. 335–339, Apr. 1996.

[2] Y. Tsividis, "Event-driven data acquisition and digital signal processing-a Tutorial," *IEEE Trans. Circuits Syst. II*, vol. 57, no. 8, pp.577-581, Aug. 2010.

[3] H. Inose, T. Aoki, and K. Watanabe, "Asynchronous delta-modulation system," *Electron. Lett.*, vol. 2, no. 3, pp. 95–96, Mar. 1966.

[4] J.W. Mark and T. D. Todd, "A nonuniform sampling approach to data compression," *IEEE Trans. Cmmun.*, vol. com-29, pp. 24-32, Jan. 1981

[5] J.Foster and T.K.Wang, "Speech coding using time code modulation," *Proc. IEEE SoutheastConf.*, 1991, vol. 2, pp. 861-863

[6] E. Allier, J. Foulier, F. Sicard, A. Dessani, E. Ander and M. Renaudin, "A new class of asynchronous A/D converters based on time quantization", *IEEE Int. Symp. on Asynchronous Circuits and Systems*, Vancouver, Canada, May 2003, pp.196-205.

[7] B. Schell and Y. Tsividis, "A continuous-time ADC/DSP/DAC system with no clock and with activity-dependent power dissipation," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp.2472-2481, Nov. 2008.

[8] K. Kozmin, J. Johansson and J. Delsing, "Level-crossing ADC performance evaluation towards ultrasound application," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 8, pp.1708-1719, Aug. 2009.

[9] T. Wang, D. wang, P. J. Hurst, B. C. Levy and S. H. Lewis, "A level-crossing analog-to-digital converter withtriangular dither," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 9, pp.2089-2099, Sep. 2009.

[10] M. Kurchuk and Y. Tsividis, "Signal-dependent variable-resolution clockless A/D conversion with application to continuous-time digital signal processing," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 5, pp.982-991, May 2010.

[11] M. Trakimas and S. R. Sonkusale, "An adaptive resolution asynchronous ADC architecture for data compression in energy constrained sensing applications," *IEEE Trans. Circuits and Syst. I*, vol. 58, no. 5, pp.921-934, May 2011.

[12] R. Agarwal and S. R. Sonkusale, "Input-feature correlated asynchronous analog to information converter for ECG monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 5, pp.459-467, Oct. 2011.

[13] C. Weltin-Wu and Y. Tsividis, "An event-driven, alias-free ADC with signal-dependent resolution," in *Proc. IEEE Symp. VLSI Technology and Circuits*, Hawaii, U.S.A., 2012, pp. 28-29.

[14] Y. Li, K. Shepard, and Y. Tsividis, "A continuous-time programmable digital FIR filter," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp.2512–2520, Nov. 2006.

[15] S. Hong, S. Lee, T. Roh and H.J. Yoo " A 46 µW motion artifact reduction bio-signal sensor with ICA based adaptive DC level control for sleep monitoring system" in *Proc. IEEE CICC, San Jose*, CA, U.S.A., 2012, pp. 1-4.

[16] F. Akopyan, R. Manohar, A. B. Apsel, "A level-crossing flash asynchronous analog-to-digital converter" in *Proc. IEEE Int. Symp. Asynchronous Circuits and Systems*, Berkeley, CA, Mar. 2006, pp. 11-22.

[17] Y.Li and W.A.Serdijn, "A continuous-time level-crossing ADC with 1-bit DAC and 3-input comparator" in *Proc. IEEE Int. Symp. Circuits and Systems*, Seoul, South Korea, 2012, pp. 1311-1314.

[18] W. Tang, C. Huang, D. Kim, B. Martini, and E. Culurciello, "4-channel asynchronous bio-potential recording system," in *Proc. IEEE Int. Symp. Circuits and Systems*, Paris, France, 2010, pp. 953 –956.

[19] T. Delbrück and C. A. Mead, "Analog VLSI adaptive, logarithmic widedynamic-range photoreceptor," in *Proc. IEEE Int. Symp. Circuits and Systems*, London, UK, vol. 4, 1994, pp. 339–342.

[20] [Online]. Available: http://www.physionet.org/physiobank/database/ptbdb/

[21] Bousseljot R, Kreiseler D, Schnabel, A. Nutzung "Der EKG-signaldatenbank CARDIODAT der PTB über das internet." *Biomedizinische Technik*, Band 40, Ergänzungsband 1 (1995) S 317

[22] [Online]. Available: http://www.brainsignals.de/

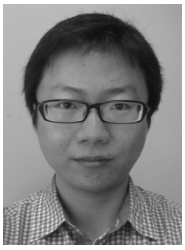
[23] G. Schalk, J. Kubanek, et.al, "Decoding two-dimensional movement trajectories using electrocortico-graphic signals in humans, *J. Neural Eng.*, vol. 4, pp. 264-275, June 2007.

[24] U. Hoffmann, J. M. Vesin, T. Ebrahimi, and K. Diserens, "An efficient P300-based brain-computer interface for disabled subjects," *J. Neuroscience Methods*, vol. 167, no. 1, pp. 115–125, Jan. 2008.

[25] [Online]. Available: http://physionet.org/physiobank/database/emgdb/

[26] J. N. Y. Aziz, K. Abdelhalim, R. Shulyzki, et. al, " 256-channel neural recording and delta compression microsystem with 3D electrodes," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp.995-1005, Mar. 2009.

[27] Yu M. Chi and G. Cauwenberghs, " Micropower integrated bioamplifier and auto-ranging ADC for wireless and implantable medical instrumentation" in *Proc. IEEE ESSCIRC, Seville*, Spain, 2010, pp. 334-337.



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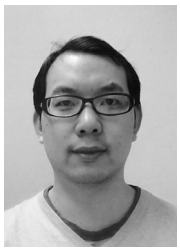

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