An Ultra Low-power Class-AB *Sinh* Integrator

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ABSTRACT

A new ultra low-power Class-AB *Sinh* integrator is proposed here. The translinear companding integrator is based on hyperbolic-sine transconductors and uses only one grounded capacitor to implement a Class-AB integrator, which saves considerable chip area. Furthermore, the proposed circuit presents excellent performance with respect to power efficiency. To validate the circuit principle, the integrator has been simulated in standard $0.35\mu m$ CMOS technology and designed to operate from a 1.5-V ($\pm$ 0.75V) supply voltage, with a current consumption of only 14nA. The THD is kept below 1%, with a modulation index as high as 20 and yields a 75-dB dynamic range at the 1-dB compression point.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles - *Advanced technologies, Input/output circuits.*

General Terms

Documentation, Performance, Design, Theory, Verification.

Keywords

Sinh integrator, class-AB integrator, log-domain filters, low-power circuit design, analog electronics.

1. INTRODUCTION

Class AB circuit design is an efficient approach to matching the requirements of good linearity, low noise contribution and low power consumption. In a Class-AB topology the quiescent bias levels in the active devices are set at relatively low levels, usually much lower than the expected signal swings. Consequently, for small signals the circuit operates in Class-A and for large signal swings operates with the efficiency of a Class-B design. This results in a higher Dynamic Range (DR) compared to conventional Class-A operation together with an improvement in power efficiency.

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In log-domain filters operating in class A, the currents are limited by $I_{in}, I_{out} > -I_o$. This means that the restriction in current-mode circuits is only single-sided. Hence, the combination of the companding circuit technique and Class-AB operation enables us to obtain more power-efficient analog signal processing where the DR can be extended without increasing the maximum SNR or the quiescent power consumption.

The hyperbolic-sine (*Sinh*) function is at the base of most of the Class-AB translinear filters [1]. Instead of a single transistor in common-emitter configuration as for class A integrators, the class-AB sinh filter is characterized by hyperbolic-sine transconductors, as described in the following sections.

The outline of the paper is as follows. Section 2 describes the general block diagram of a companding *sinh* integrator. Subsequently, Section 3 deals with the description of the proposed integrator as well as a CMOS implementation. Some results provided by simulations are also presented in this section. Finally, Section 4 presents the conclusions.

2. COMPANDING SINH INTEGRATOR

The proposed design is based on the general block diagram of a companding integrator, defined by Seevinck [2].

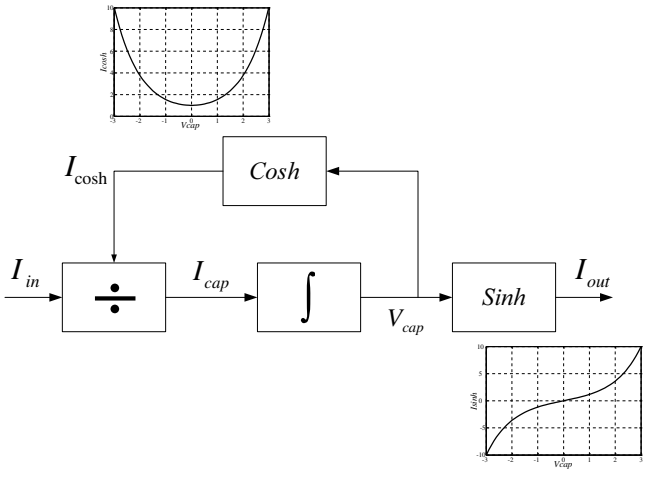


Figure 1: Block diagram of the companding sinh integrator

The block diagram of a companding *sinh* integrator is given in Fig.1. It consists of a divider, a linear time in-

tegrator, a hyperbolic-sine expander block that generates the output current I_{out} from the internal capacitance voltage V_{cap}, $I_{out} = \sinh(V_{cap})$, and a hyperbolic-cosine block that generates the derivative of the output signal I_{out} with respect to V_{cap}, $I_{cosh} = \frac{d\sinh(V_{cap})}{dV_{cap}} = \cosh(V_{cap})$ [3].

From the bock diagram given in Fig.1, one can see that the capacitance current can be defined as

$$I_{cap} = \frac{I_{in}}{I_{cosh}}. \tag{1}$$

The V-I transfer function of the sinh output structure, is described by

$$I_{out} = 2I_o \sinh(\frac{V_{cap}}{V_T}) = I_o e^{\frac{V_{cap}}{V_T}} - I_o e^{-\frac{V_{cap}}{V_T}}. \tag{2}$$

Despite the nonlinear relations of the output current to the capacitance voltage and the capacitance current to the input current, the integrator can be considered to be an implementation of a first-order linear differential equation $I_{in} = dI_{out}/dt$ by applying the chain rule

$$I_{in} = I_{cap} \cdot I_{cosh} = C \cdot \frac{dV_{cap}}{dt} \cdot \frac{d\sinh(V_{cap})}{dV_{cap}} \Rightarrow I_{in} = C \cdot \frac{dI_{out}}{dt}. \tag{3}$$

3. CLASS-AB SINH INTEGRATOR DESIGN

To implement the companding integrator presented in Fig.1, we propose a new ultra low-power Class-AB *sinh* integrator. The schematic of the completed integrator is given in Fig.2.

Instead of a single transistor in common-emitter configuration in class A integrators, the class-AB sinh filter is characterized by hyperbolic-sine transconductors.

One can analyze the new *sinh* integrator in terms of Translinear Loops (TL). As seen from Fig. 2, the integrator consists mainly of 3 *sinh* transconductors, defined from the translinear loops $Q_{1A} - Q_{2A} - Q_{2B} - Q_{1B}$, $Q_{3A} - Q_{4A} - Q_{4B} - Q_{3B}$ and $Q_{5A} - Q_{6A} - Q_{6B} - Q_{5B}$, which implement the current splitter, the divider-Cosh block and the Sinh output stage, respectively.

At the output, the relation between I_{out}, I_{out+} and I_{out-}, defined from the Sinh output stage $Q_{5A} - Q_{6A} - Q_{6B} - Q_{5B}$, is described by

$$I_{out} = I_{out+} - I_{out-} \tag{4}$$

$$I_{out+} \cdot I_{out-} = I_{dc}^2. \tag{5}$$

The current splitter comprising transistors Q_{1A} through Q_{1B}, which is a geometric-mean current splitter, implements

$$I_{in} = I_{in+} - I_{in-} \tag{6}$$

$$I_{in+} \cdot I_{in-} = I_{out+} \cdot I_{out-} = I_{dc}^2. \tag{7}$$

In addition, the third *sinh* transconductor $Q_{3A} - Q_{4A} - Q_{4B} - Q_{3B}$ realizes the divider-Cosh block, thus defining the correct non-linear current through the capacitor to obtain a global linearization, i.e., an externally linear transfer function. The currents I_{CA}, I_{CB} and I_{cap} are given by

$$I_{cap} = I_{CA} - I_{CB} \tag{8}$$

$$I_{CA} \cdot I_{CB} = \frac{I_{dc}I_o}{I_{cosh}} \cdot \frac{I_{dc}I_o}{I_{cosh}} \tag{9}$$

assuming $I_{cosh} = I_{out+} + I_{out-}$. Hence, considering also the static translinear loop $Q_{1A} - Q_{2A} - Q_{3A} - Q_{4A} - Q_{5A} - Q_{6A}$, we have

$$I_{out+} \cdot \frac{I_{dc}I_o}{I_{cosh}} \cdot I_{dc} = I_{in-} \cdot I_{CA} \cdot I_{out+}. \tag{10}$$

Thus, substituting Eq.7 into Eq.10, we end up with

$$I_{CA} = \frac{I_{in+}I_o}{I_{cosh}} \tag{11}$$

and having Eq.11, Eq.9 and Eq.7, the current I_{CB} can be written as

$$I_{CB} = \frac{I_{in-}I_o}{I_{cosh}}. \tag{12}$$

Subtracting Eq.12 from Eq.11 results in

$$I_{CA} - I_{CB} = \frac{I_{in+}I_o}{I_{cosh}} - \frac{I_{in-}I_o}{I_{cosh}} \Rightarrow I_{cap} = \frac{I_{in}I_o}{I_{cosh}}. \tag{13}$$

From Eq.13, we can verify that the proposed integrator indeed implements a companding *sinh* integrator as shown in Fig.1. Next, from the dynamic translinear loops, consisting of $C - Q_{5A} - Q_{6A}$ and $C - Q_{5B} - Q_{6B}$, we obtain

$$I_{cap}I_{out+} = CV_T\dot{I}_{out+} \tag{14}$$

and

$$I_{cap}I_{out-} = -CV_T\dot{I}_{out-} \tag{15}$$

where the dot represents differentiation with respect to time. Finally, substituting Eq.14 and Eq.15 in Eq.13, we can obtain the input-output relation

$$I_{in} = \frac{CV_T}{I_o}\dot{I}_{out} \tag{16}$$

which is a linear differential equation, describing an inherent lossless companding integrator with time constant $\tau = \frac{CV_T}{I_o}$. In order to obtain a lossy integrator we can easily introduce a negative feedback path from the output to the input of the integrator, resulting in

$$I_{in} = I_{out} + \frac{CV_T}{I_o}\dot{I}_{out} \tag{17}$$

describing a first-order low-pass filter with cutoff frequency ω_C according to

$$\omega_C = \frac{I_o}{CV_T}. \tag{18}$$

Simulating first the proposed integrator using quasi-ideal exponential devices, i.e. bipolar transistors with very large current gain ($\beta = 10^6$), one can see in Fig.3 the magnitude of the frequency response of the *sinh* lossy integrator, with the cutoff frequency varying from 318 Hz to 636 kHz, showing the large frequency tuning range typical to translinear filters.

The externally linear internally nonlinear (ELIN) behavior of the integrator can be seen from the output current and the capacitance current, respectively, in Fig.4 for an input signal swing much larger than the bias current I_o.

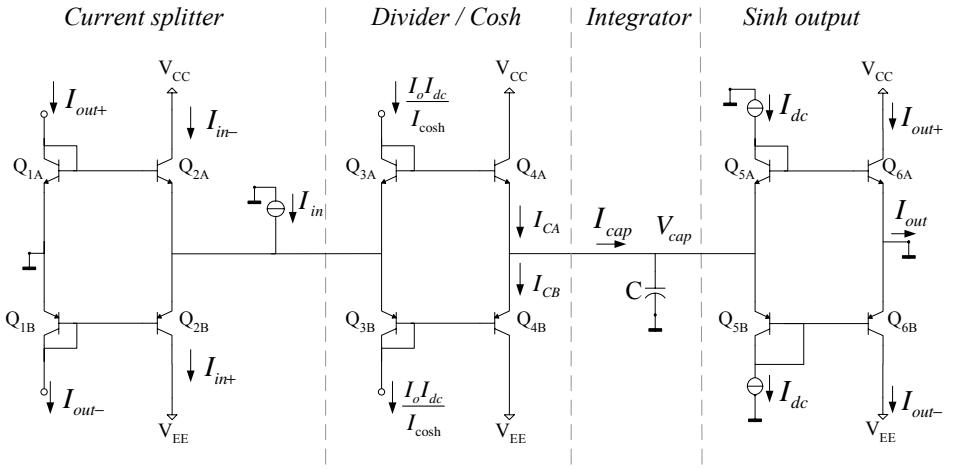


Figure 2: Circuit diagram of the proposed class-AB sinh integrator

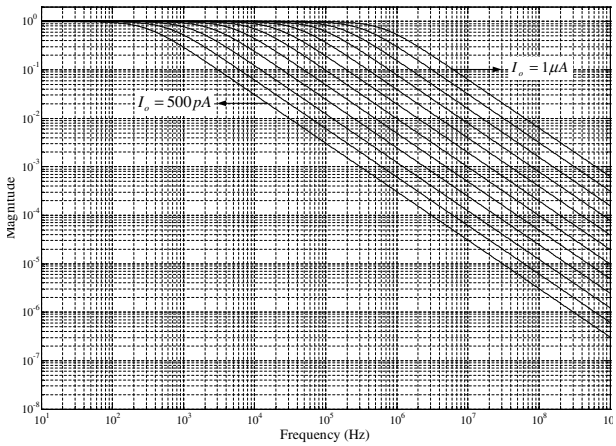


Figure 3: Frequency response changing Io from 500pA to 1uA using quasi-ideal exponential devices

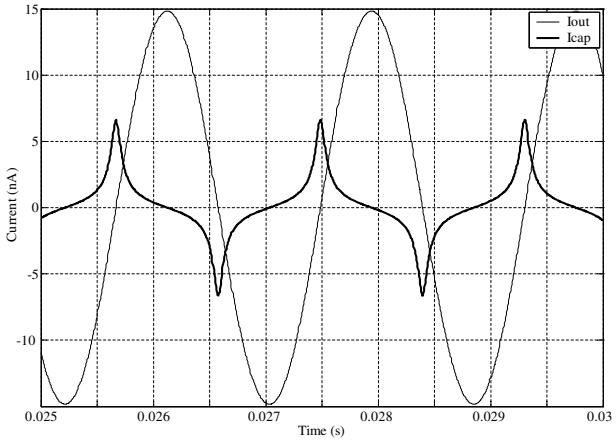


Figure 4: Output current and capacitance current for large input signal swing using quasi-ideal exponential devices

3.1 CMOS Integrator Implementation

To validate the circuit principle, we have implemented and simulated the proposed integrator using models of AMS's 0.35 μm CMOS IC technology. The circuit has been designed to operate from a 1.5-V ($\pm$ 0.75V) supply voltage. The schematic of the completed integrator is given in Fig.5. The bipolar transistors have been replaced by equivalent CMOS transistors operating in weak inversion. The transistors have an aspect ratio of $100\mu/1\mu$, in order to extend the weak inversion operation up to $2\mu A$. In addition, to realize the expression $\frac{I_o I_{dc}}{I_{cosh}}$, we added in the loops transistors M_7 and M_8. The current I_{cosh} can be obtained easily by adding the positive and the negative output currents.

In class-AB operation, a static non-linear current splitter is used at the input to divide the bipolar input current I_{in} into two currents I_{in+} and I_{in-}, which are both strictly positive. The current splitter presented here is a geometric-mean splitter, comprising transistors $M_{1A} - M_{2A} - M_{2B} - M_{1B}$, where the corresponding equations are given by

$$I_{in+}, I_{in-} = \frac{\pm I_{in} + \sqrt{I_{in}^2 + 4I_o^2}}{2}. \tag{19}$$

The output splitter currents are shown in Fig.6, for a sinusoidal input signal with an amplitude of 10nA and a bias current I_o of 1nA.

As shown in Fig. 1, and in Eq.4 and Eq.13, the companding integrator can be characterized by a hyperbolic-sine transconductor at the output and a combined *cosh*-divider block at the input, which relates the currents I_{out} and $I_{cosh} = \frac{I_{in} \cdot I_o}{I_{cap}}$ to the capacitance voltage V_{cap}, respectively. The simulated transfer functions of those blocks are shown in Fig. 7. The simulated output current with respect to the capacitance voltage is shown in Fig. 7a whereas the ratio between the input and capacitance currents versus V_{cap} is illustrated in Fig. 7b.

The hyperbolic-sinusoidal transconductance of the output stage results in an inherently nonlinear dynamic relation between I_{cap} and I_{out}, which can be described by [4]

$$I_{cap} = CV_T \frac{\dot{I}_{out}}{\sqrt{I_{out}^2 + 4I_o^2}}. \tag{20}$$

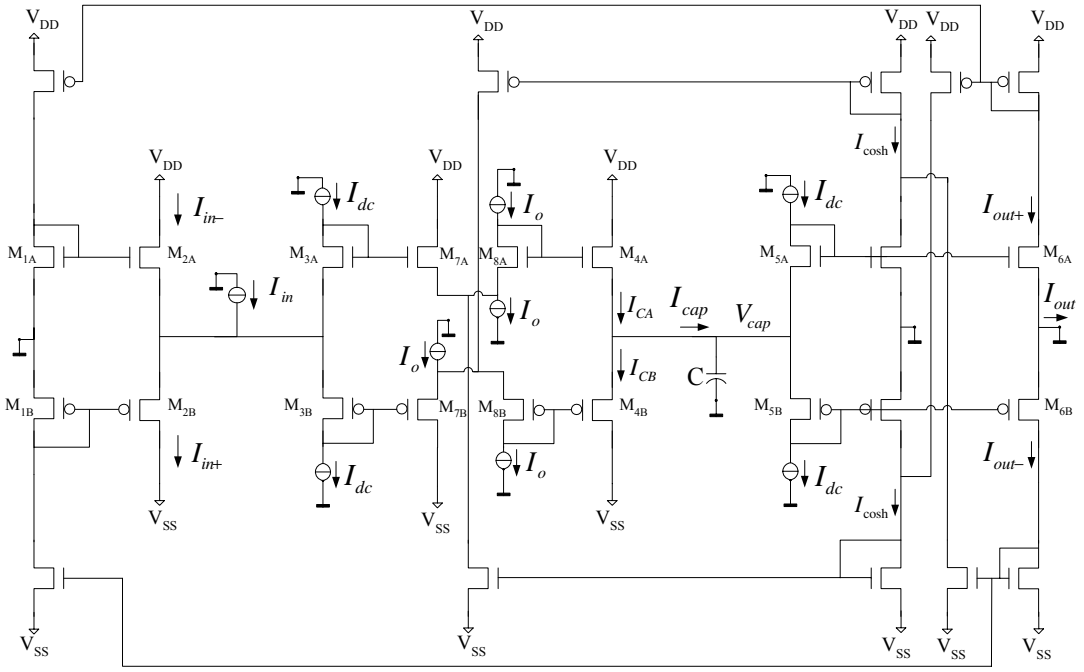


Figure 5: Schematic of the CMOS class-AB sinh integrator

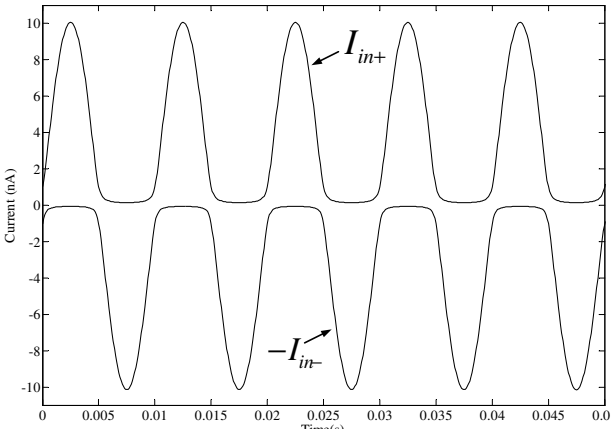
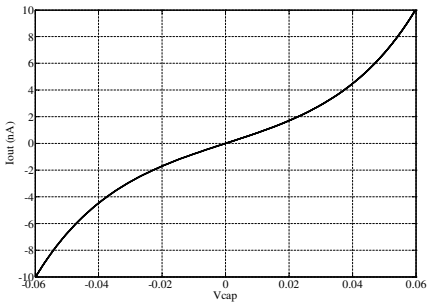
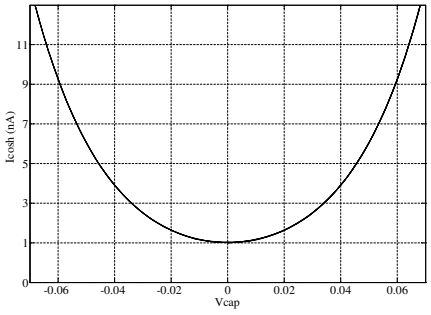


Figure 6: Simulated current splitter output currents



(a)



(b)

Figure 7: Simulated currents with respect to the capacitance voltage V_{cap} (a) output current I_{out} and (b) I_{cosh}

As shown in Fig.8, I_{cap} is nearly sinusoidal for low values of m, where m represents the modulation index ($m = I_{in}/I_o$). This linear behavior can be explained through the denominator of Eq.20, which does not vary that much for low output currents. Thus, the I_{cap} is more or less proportional to the derivative of I_{out}. The capacitance current becomes more nonlinear when m increases, i.e. for large output swings, as seen in Fig.8.

However, despite the nonlinear nature of the capacitance currents in *sinh* integrators, an exactly linear transfer function can be realized, as one can see in Fig.9, where the output is still defined by a sine function for m varying from 1 to 20.

In addition, one can see the linear tunability of the filter, described in Eq.17, from the simulated frequency response, given in Fig.10. With reference to Eq.18, the cutoff fre-

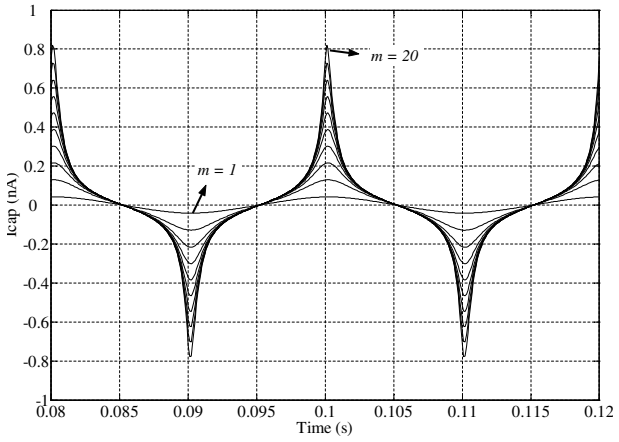


Figure 8: Simulated capacitance current I_{cap} with I_o equals 1nA and input amplitude changing from 1nA to 20nA

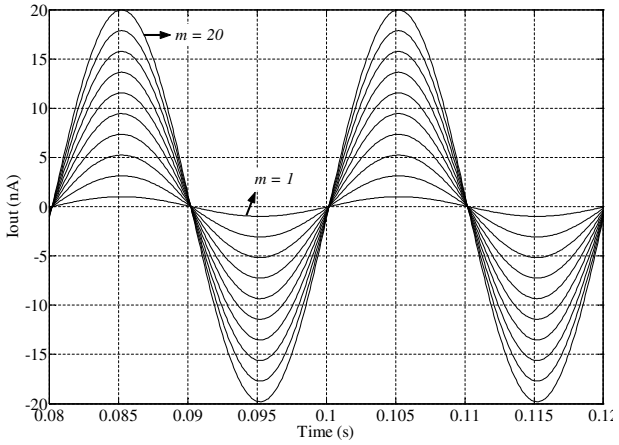


Figure 9: Simulated output current I_{out} with I_o equals 1nA and input amplitude changing from 1nA to 20nA

quency is directly proportional to bias current I_o, changing from 318 Hz to 1.2 MHz with I_o equal to 500 pA and 2 μA, respectively, and C equal to 10 pF. Thus, it can be deduced that the cutoff frequency of the filter can be linearly controlled over a wide frequency range.

The Dynamic Range (DR), defined as the ratio between the maximum signal amplitude for a given distortion (in this case, 1-dB compression point) and the noise floor, is shown in Fig.11. The output RMS current noise for I_o = 1nA is 4.2pA, resulting in a DR at the 1-dB compression point of approximately 75 dB. The total current dissipation is 11nA ($11 \cdot I_o$) for a lossless configuration and 14nA ($14 \cdot I_o$) for the lossy integrator (first-order low-pass filter).

Fig.12 shows the total harmonic distortion (THD) at the output as a function of the modulation index m and input signal frequency. At a frequency much lower than the cutoff frequency (f_c), i.e. $f_c/10$, the THD is kept below 1%, with a modulation index as high as 20. As expected, the THD increases for an input signal frequency close to f_c. In this case, f_c equals 636 Hz and results in a THD at the cutoff frequency of 0.3% for $m = 1$ and 3.2% for $m = 20$.

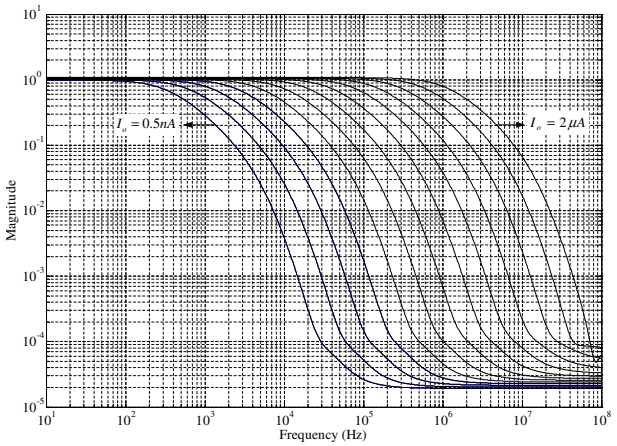


Figure 10: Frequency response changing Io from 500pA to 2uA

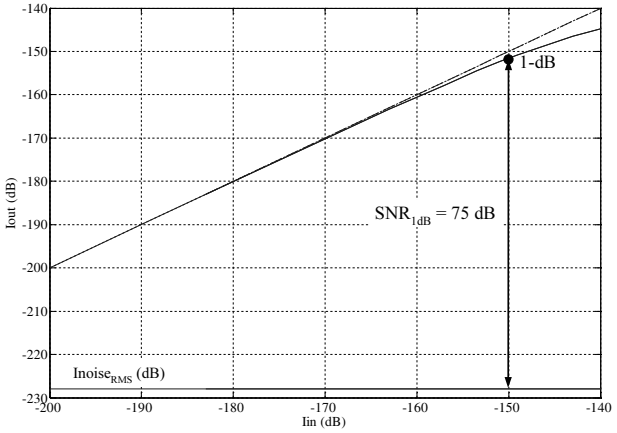


Figure 11: Signal-to-noise ratio at 1dB compression point for I_o = 1nA

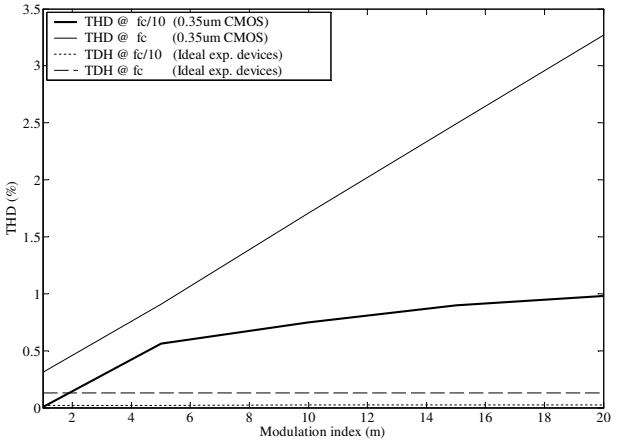


Figure 12: Total Harmonic Distortion versus m for frequencies @fc and @$fc/10$

Table.1 makes a comparison with other log-domain Class-AB designs. The first advantage of this design is that it

Table 1: Performance comparison of the proposed class-AB integrator with other implementations

	Serdijn et al. [3]	Punzenberger et al. [5]	El-Gamal et al. [6]	Python et al. [7]	Redondo et al. [8]	This work
Technology	Bipolar	BiCMOS	Bipolar	CMOS	CMOS	CMOS
Capacitance	$1 \cdot C$	$2 \cdot C$	$2 \cdot C$	$2 \cdot C$	$2 \cdot C$	$1 \cdot C$
Bias current (without splitter)	$13 \cdot I_o$	$11 \cdot I_o$	$12 \cdot I_o$	$12 \cdot I_o$	$13 \cdot I_o$	$9 \cdot I_o$
Supply voltage	3.3V	1.2V	1.2V	1.5V	1V	1.5V
P_{diss} per pole & ω_c (quiescent)	$42 \cdot CV_T$	$13 \cdot CV_T$	$14 \cdot CV_T$	$18 \cdot CV_T$	$13 \cdot CV_T$	$13 \cdot CV_T$

uses only one capacitor to implement a Class-AB integrator, which saves considerable chip area. This is particularly important for low-frequency designs where we inevitably need to use large capacitance values. Furthermore, the proposed circuit presents an excellent performance with respect to power efficiency. The power efficiency of a continuous-time filter is a figure of merit used in comparing various filter topologies and can be estimated by means of the power dissipation per pole P_{diss} & cut-off frequency f_c, defined as $\frac{P_{diss}}{f_c}$ [9].

The performance of the filter is summarized in Table 2.

Table 2: Performance of the proposed integrator for two different cutoff frequencies

Technology	0.35μm CMOS	
Bias current	$I_o = 1$nA	$I_o = 2\mu$A
Capacitance	10pF	10pF
Supply voltage	1.5V	1.5V
Center frequency (f_c)	636Hz	1.27MHz
Total bias I_o (Lossless integrator)	11nA	22μA
Total bias I_o (Lossy integrator)	14nA	28μA
Power dissipation	22.5 nW	45 μW
Dynamic Range (1-dB)	75 dB	75 dB
Noise current (rms)	4.2pA	6.9nA
Supply voltage range	1V - 3V	1.5V - 3V
Power diss. per pole & f_c	35.37pJ	35.37pJ

4. CONCLUSIONS

A new ultra low-power Class-AB *Sinh* integrator based on hyperbolic-sine transconductors is presented. The proposed integrator uses only one grounded capacitor and shows excellent power efficiency, compared with existing log-domain Class-AB implementations.

The lossy integrator is simulated using CMOS transistors in weak-inversion, operating from a 1.5-V ($\pm$ 0.75V) supply voltage. The total current consumption of the first-order low-pass filter is 14nA and the DR at the 1-dB compression point is 75 dB. The filter can handle signals much larger than the bias current, while keeping THD below 1%.

5. REFERENCES

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