Receiver RF Front-End with 5GHz-Band LC Voltage-Controlled Oscillator and Subharmonically-Locked Ring Oscillator for 17GHz Wireless Applications

Aleksandar Tasić[1], Stephen S.Y. Yue[2], Dennis K.L. Ma[3],
Wouter A. Serdijn[1], John R. Long[1] and David L. Harame[4]

[1] Electronics Research Laboratory, Delft University of Technology, The Netherlands
Phone: +31 (0)15 278 9423; Fax: +31 (0)15 278 5922; E-mail: a.tasic@tudelft.nl
[2] ATI Technologies, Inc., Canada, [3] Synopsys, Inc., Canada,
[4] IBM Microelectronics, Burlington, VT, USA

***Abstract* – A 17GHz RF receiver front-end consisting of a low-noise amplifier, dual balanced mixers, an LC voltage-controlled oscillator, and a frequency tripler implemented using a ring oscillator is presented in this paper. The measured LC-VCO phase noise is –112dBc/Hz at 1MHz offset from a 5.7GHz carrier. For a 1.3-3V range in VCO tuning voltage, the locking range of the tripler is 5.5GHz (16.1GHz-21.6GHz). The receiver front-end conversion gain is 13.2dB with a noise figure of 7.1dB (SSB 50Ω) and a 3rd-order input intercept point of –6.2dBm. The 1.84mm^2 testchip draws 36mA from a 2.2V supply.**

***Index terms* – receiver RF front-end, quadrature downconverter, low-noise amplifier, mixer, tripler, oscillator.**

I. Introduction

New standards are being defined to increase overall capacity and support data rates above 100Mbit/s for emerging wireless networking applications. Portions of the 10-66GHz spectrum may be allocated for line-of-sight access: 802.16 [1] supports a data rate of 134Mb/s above 10GHz, whereas HiperLINK [2] proposes a data rate of 155Mb/s close to 17GHz band.

This paper describes an exploratory 17GHz downconverter (LNA and dual quadrature mixers) and two oscillators: a 5.4-6GHz LC voltage-controlled oscillator (VCO) and an injection-locked oscillator for wireless applications. In addition to providing a high-purity 17GHz carrier after locking, the 5.4-6GHz VCO output can also support the 802.11a [3], HiperLAN2 [4], and 802.16a standards.

The design of the oscillators and quadrature downconverter circuits used in the experimental implementation of a 17GHz receiver front-end is described in the following section (Section II) of this paper. Measurement results for the testchip, fabricated in a production SiGe-BiCMOS technology [5], are detailed in Section III.

II. 17GHz Receiver RF Front-End

A block diagram of the receiver test circuit is shown in Fig. 1.

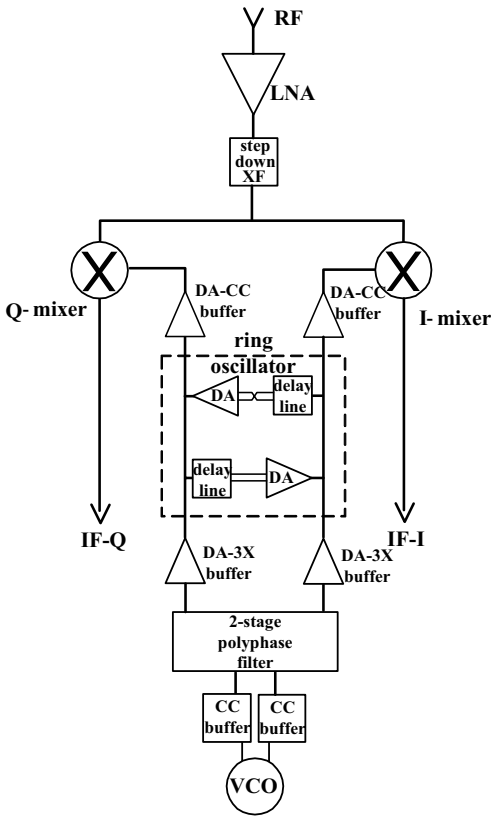

Fig. 1: 17GHz receiver RF front-end block diagram.

The receiver IC has three main blocks: a 5GHz-band oscillator, a 17GHz-band injection-locked oscillator, and a 17GHz quadrature downconverter (LNA and mixers).

The LC voltage-controlled oscillator, two common-collector buffers (CC in Fig. 1) and a two-stage polyphase filter generate a quadrature 5.4-6GHz local oscillator (LO). The quadrature LO signals used to drive the 17GHz downconverting mixers are generated by a delay-line ring oscillator locked to the 3rd harmonic of the 5.4-6GHz quadrature LO. The harmonics are generated by amplitude limiting of differential amplifiers DA-3X in Fig. 1. The 2-stage delay-line ring oscillator uses differential amplifier gain stages (DA in Fig. 1) and asymmetric on-chip LC delay lines [6]. The phase of the ring oscillator outputs can be adjusted by a few degrees on either side of the nominal (very close to quadrature because of on-chip matching of stages). A differential amplifier and two common-collector buffers (DA-CC in Fig. 1) provide the interface between the mixer and ring oscillator circuits. Buffering between the LO outputs and mixers also equalizes the amplitudes, so that image rejection higher than 50dB can be realized. The low-noise amplifier (LNA), interstage step-down transformer (XF) and dual double-balanced mixers complete the RF path of the test chip.

A. 5GHz- and 17GHz-Band Quadrature Oscillators

The bipolar LC-VCO (see Fig. 2) generates the 5.4-6GHz-band LO signals. It consists of a resonating LC tank (inductor L and nMOS varactor C_V), feedback capacitors C_A and C_B, and a cross-coupled transconductor (Q_{O1}-Q_{O2}). The noise contribution of the bias tail-current source (TCS) without any degeneration to the phase noise of this oscillator is larger than all other noise contributions together (i.e., more than 70% of the total) [7]. In particular, the TCS noise around twice the oscillation frequency ($2f_0$) is the largest contributor to the phase noise after being frequency converted by the transconductor to within the bandwidth of the resonator.

Resonant-inductive degeneration (RID) of the tail-current source is used to minimize the phase noise contributed by the TCS. By forming a resonance between degeneration inductor (L_{RID}) and the base-emitter capacitance of the TCS at $2f_0$, the contributions of all noise sources from the bias source to the oscillator phase noise are reduced by a factor $(f_T/2f_0)^2$ [7]. The high impedance in the emitter at resonance reduces the transconductance and gain for thermal noise from base-resistance to the output, and impedes the flow of collector-current shot noise, making these noise contributions negligible.

A symmetric 7-turn 2.6nH degeneration inductor integrated in 1.25um thick metal allows a 4-fold improvement in phase noise for the oscillator. The 1.2nH inductor for the LC-tank is designed in 4um thick aluminum top metal. The 2-turn symmetric inductor is differentially-shielded from the silicon substrate in order to maximize its Q-factor. It has an outer dimension of 190um, metal width and spacing of 10um and 5um, respectively. Two nMOS varactors with 40 gates are used to tune the oscillator.

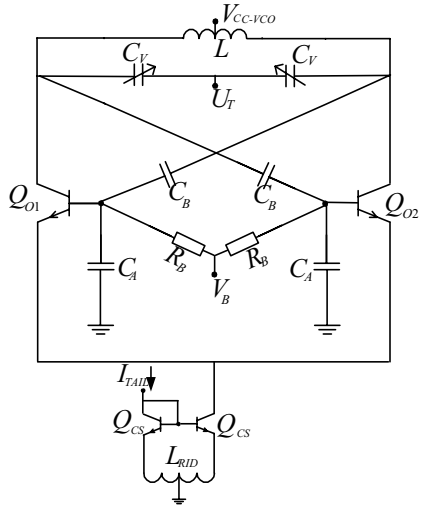

Fig. 2: LC voltage-controlled oscillator with RID TCS.

Quadrature signals that drive the tripler (DA-3X in Fig. 1) are generated by a two-stage polyphase filter with cutoff frequencies positioned in the upper half of the 5GHz band (at 5.6GHz and 5.9GHz).

The phase noise performance of the 5.4-6GHz LC VCO design is sufficient to satisfy the 802.11a, HiperLAN2, and 802.16a wireless standards (operating from 5.47-5.85GHz band), allowing a multistandard transceiver implementation.

Limiting amplifiers triple the frequency injected from the polyphase filter into each delay-line oscillator stage [6]. The ring oscillator is designed to free-run below the third harmonic of the injection amplifier outputs. The limiting amplifiers, ring oscillator gain stages, and 17GHz LO buffers are biased at 3mA, 2mA, and 3.6mA, respectively. The bias points are selected to optimize the injection-locking range and LO output amplitude [6].

Quadrature phase and amplitude accuracy of the LO signals in the 17GHz band is provided by the fully-balanced topology of the injection-locked oscillator and on-chip matching of components. Fine tuning of the output phase is realized by adjusting the bias current in each stage of the ring oscillator. The phase noise of the output is set by the 5.4-6GHz VCO after injection locking.

B. 17GHz-Band Quadrature Downconverter

The 17-GHz RF path consists of the cascode LNA, two doubly balanced mixers, and an interstage coupling transformer.

The LNA (see Fig. 3) is designed for simultaneous noise and power match to a 50Ω source. Noise matching is achieved by selecting 0.2x19.2um^2 transistors biased by a total current of 7.1mA.

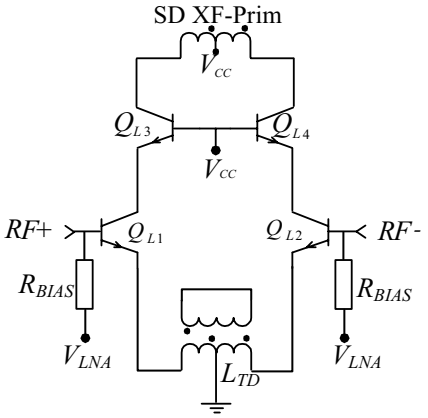

Fig. 3: LNA schematic diagram.

The LNA is degenerated by a 3-turn multi-layer (overlay) inductor (L_{TD}=0.75nH). The small inductance is realized by a short-circuiting shield winding placed beneath the top metal coil. The small inductance value facilitates an impedance match for maximum gain and power transfer at the input of the LNA without compromising the transistor transit frequencies (f_T). The interstage 1:3 step-down transformer provides a load of ~240Ω to the LNA from the mixer. The linearity of the LNA is affected by the choice of the load impedance, degeneration inductance, and bias current.

Each downconverting mixer is connected as shown in Fig. 4. The 2 mixers are driven by the secondary terminals of the step-down transformer (SD XF in Figs. 3 and 4).

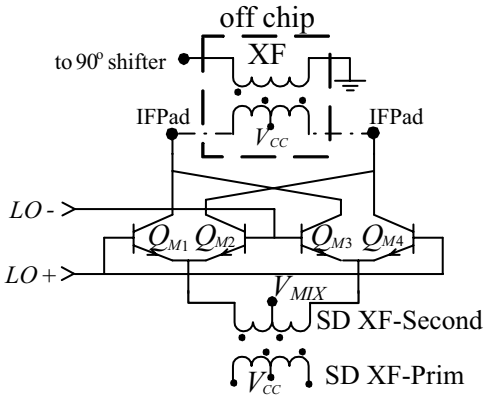

Fig. 4: Double-balanced mixer circuit.

The doubly-balanced mixer is a Gilbert-type bipolar switching quad with an on-chip current source bias via the secondary windings of the interstage (i.e., LNA-mixer) transformer. Off-chip baluns provide a differential to single-ended conversion required for testing and characterization. The mixers consume 2.1mA each.

III. Experimental Results

The receiver testchip photograph is shown in Fig. 5. It occupies an area of 2.3x0.8mm^2 (1.84mm^2), excluding bondpads. A custom test fixture (see Fig. 6) with bias and supply lines filtering was designed for testing. The testchip was mounted through a hole in the test board in order to minimize the wirebond interconnections between chip and test fixture. Differential quadrature IF signals are converted to single-ended form via external balun transformers, and a 50Ω quadrature hybrid combines the IF outputs at 100MHz. Mixer circuits see 200Ω loads.

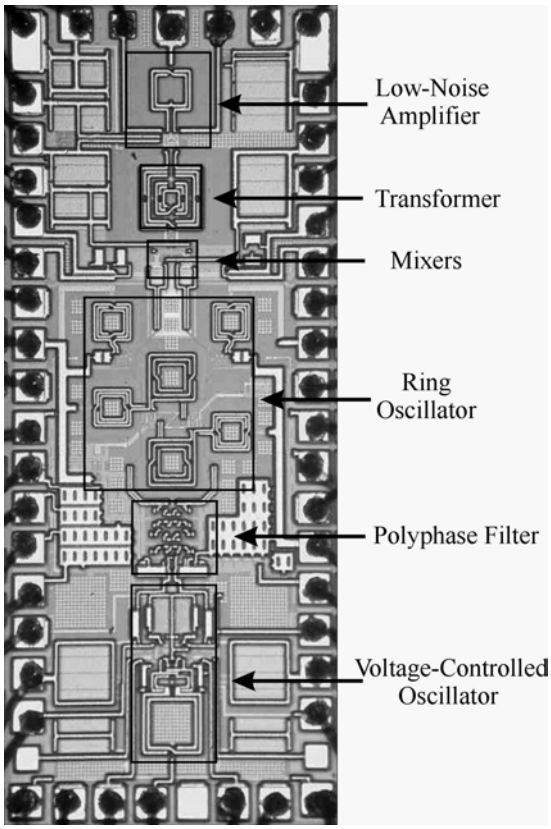

Fig. 5: 17GHz receiver RF front-end photomicrograph.

The measured results for the complete RF front-end after de-embedding from the test fixture are summarized in Table I.

Conversion gain of the receiver is limited by the mixer load impedance to 13.2dB, but could be easily increased by increasing the mixers loads above 200Ω with little effect on

IF bandwidth. The measured single sideband noise figure (50Ω) is 7.1dB, and input-referred 3rd-order intercept point is –6.2dBm at a total bias current of 11.3mA for the LNA and mixers. The image-rejection is 30dB without, and 75dB with trimming of the I/Q LO phases [6]. The input return loss and port-to-port isolation are better than –15dB and 40dB, respectively.

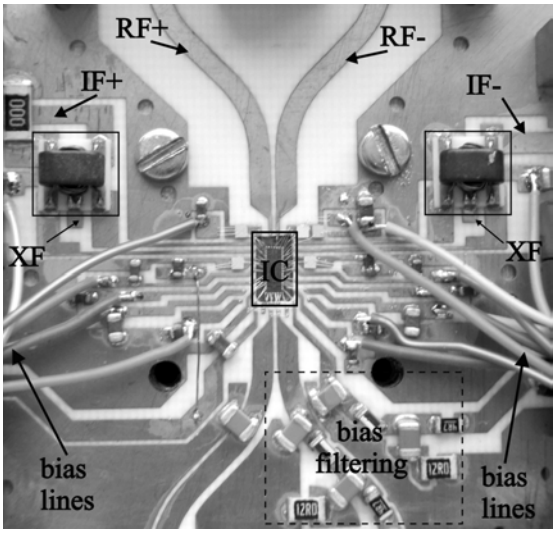

Fig. 6: The IC in the test fixture.

The VCO performance was characterized separately from a stand-alone test circuit [7], where it was shown that RID improves the phase-noise by 6dB. The tuning range is 600MHz (5.45-6.05GHz) for a tuning voltage between 1.3V and 2.2V. At 1MHz offset from 5.7GHz, the oscillator phase noise is –112dBc/Hz at a current consumption of 4.8mA, satisfying the phase noise requirements of all commercial WLAN standards in this frequency band.

TABLE I. RECEIVER PERFORMANCE PARAMETERS

Conversion Power Gain [dB]	13.2
Noise Figure [dB]	7.1
Input 3rd-Order Intercept Point [dBm]	-6.2
Phase Noise at 1MHz from 5.7GHz [dBc/Hz]	-112
Power Consumption: LNA and Mixers [mW]	25
Power Consumption: Tripler Ring Oscillator and Buffers [mW]	38
Power Consumption: VCO and Buffers [mW]	17
Total Power Consumption [mW]	80

The phase noise of the delay-line ring oscillator when injection locked is 9.5dB higher than that of the LC-VCO because of frequency multiplication. The free-running frequency of the ring oscillator is 16.1GHz. For a 2.2V VCO tuning voltage (U_T in Fig. 2, limited by the power supply), the tripler injection-locks up to 18GHz. The LC-VCO, ring oscillator, and their associated buffers draw a total of 25.2mA of current from a 2.2V supply. If the tuning voltage range is increased to 3V, the locking range can be extended up to 21.6GHz at only 2mA VCO bias current, for a total locking range of 5.5GHz.

V. CONCLUSIONS

The design of an exploratory 17GHz receiver front-end is described in this paper. Fabricated in a production 120GHz-f_T SiGe-BiCMOS technology, it demonstrates high performance achieved by drawing 36mA from a 2.2V supply: locking range of 5.5GHz, noise figure of 7.1dB, and 3rd-order input intercept point of –6.2dBm.

ACKNOWLEDGEMENTS

The authors thank Wil Straver of TU Delft for technical support, and IBM Microelectronics for fabrication access.

REFERENCES

[1] The IEEE 802.16 Working Group on Broadband Wireless Access Standards, http://www.ieee802.org/16/.

[2] ETSI HIPERLAN/2 Standard, http://portal.etsi.org/bran/kta/Hiperlan/hiperlan2.asp.

[3] *Wireless LAN MAC and Physical Layer (PHY) Specification – High-Speed PHY in the 5GHz Band*, ANS/IEEE Standard 802.11a, 1999.

[4] "Broadband Radio Access Network; HiperLAN type 2; PHY Layer", ETSI, Sophia, Antipolis Cedex, France, TS 101 475, ver. 1.3.1., 2001.

[5] A. Joseph et al., "A 0.18um 120/100GHz (f_T/f_{MAX}) HBT and ASIC-compatible CMOS using Copper interconnect", *Proceedings BCTM*, pp. 143-146, October 2001.

[6] S. Y. Yue, D. Ma and J. R. Long, "A 17.1-17.3GHz Image-Reject Downconverter with Phase-Tunable LO using 3x Subharmonic Injection Locking", *Journal of Solid-State Circuits*, vol. 39, no. 12. pp. 2321-2332, December 2004.

[7] A. Tasic, W. A. Serdijn, J. R. Long, and D. L. Harame, "Resonant-Inductive Degeneration for a Fourfold Phase-Noise Improvement of a 5.7GHz-Band Voltage-Controlled Oscillator", *Proceedings BCTM*, pp. 236-239, October 2005.