A Multi-Standard Adaptive Image-Reject Downconverter

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Abstract **– A multi-standard adaptive image-reject downconverter (oscillator and dual mixers) that satisfies the basic requirements of 2nd and 3rd generation wireless standards (i.e., DCS1800, W-CDMA, 802.11b, Bluetooth and DECT) is presented. The adaptivity between the standards is achieved by trading RF performance for current consumption, ranging from 9.9mA for the relaxed mode (2.4GHz DECT) to 20.2mA for the highest performance mode (1.8GHz DCS1800) of operation. The adaptive oscillator achieves -123dBc/Hz and -103dBc/Hz phase noise at 1MHz offset in a 2.1GHz band for bias current levels of 6mA and 0.5mA, respectively. In the highest performance mode, the image-reject downconverter (quadrature mixers) has an *IIP3* of +5.5dBm, single-side band *NF* of 13.9dB (50Ω) and conversion gain of 1.4dB, while drawing 10mA from a 3V supply.**

Index terms **– image-reject downconverter, voltage-controlled oscillator, mixer, multi-standard circuits, adaptive circuits.**

I. Introduction

Transceivers for multi-mode and multi-standard telephony are most often implemented by replicating the radio frequency (RF) front-end for each operating band or standard [1]. This allows applications such as GSM and WCDMA to operate concurrently (i.e., one can receive or make a call with either system at any time). Although high level of integration is possible on silicon, the increase in RF hardware required to implement this type of multi-standard radio increases the total current consumption, thereby reducing talk time. In such situations, the ability to share circuit functions between different standards in an adaptive multi-standard RF front-end offers the advantages of reduced power consumption, and smaller chip area, and most importantly, has the potential for lower cost. Realization of the adaptivity function requires scaling of parameters such as current consumption to the demands of the signal-processing task at hand.

The results of an exploratory multi-standard adaptive (MSA) image-reject (IR) downconverter circuit for a multi-standard adaptive RF front-end are described in this paper. This MSA downconverter design (oscillator and mixers) allows for adaptation between different standards by trading RF performance for current consumption in an adaptive way.

The following section discusses the system requirements for multi-standard adaptive receivers. The design of the adaptive quadrature downconverter circuits used in the experimental implementation is described in Section III. The measurement results are presented in Section IV, demonstrating that a 2:1 saving in power consumption is possible when adaptivity is employed.

II. System Requirements for Multi-Standard Adaptive RF Front-Ends

Concurrent operation of different wireless standards using a common RF receiver poses demands on performance (e.g., band selection, image-rejection and noise/power match prior to low-noise amplification) that are difficult to meet using a single RF path [2]. Therefore, multi-standard receivers often use duplicate circuit blocks, or even multiple RF front-ends (i.e., one for each standard).

The multi-standard receiver, shown in Fig. 1, is a compromise between these two approaches. Impedance matching, packaging and prefiltering requirements are relaxed and simplified by using multiple low-noise amplifiers (LNAs). An RF switch selects the standard of interest. A single adaptive quadrature downconverter can then be used to interface the RF and baseband sections of the receiver.

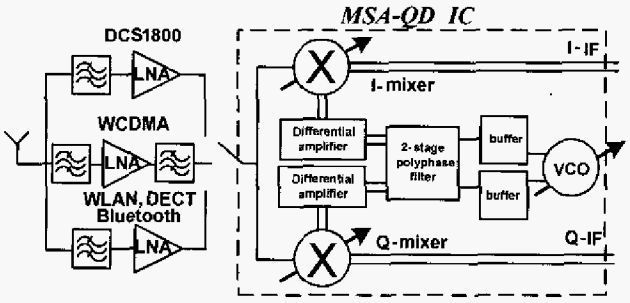

Figure 1. A multi-standard adaptive RF front-end.

If the voltage-controlled oscillator and mixer performance are adequate to cover the range of signals anticipated for each application (standard), the quadrature downconverter (QD) enables a multi-standard receiver realization with a single circuit block (MSA-QD IC in Fig. 1).

Analog and digital baseband signal processing functions could be used to monitor quality of service (e.g., error rate of the detected bit sequences) and adjust the receiver

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parameters (e.g., *tune* a single bias current or multiple currents) in real-time to meet the requirements of a given standard.

For this work, the multi-standard adaptive QD is intended to operate as a part of a zero intermediate frequency (IF) receiver for all standards except DCS1800, where low-IF operation is assumed. The test circuit consists of an adaptive voltage-controlled oscillator (VCO), oscillator buffers, a two-stage poly-phase filter to generate quadrature local oscillator signals, mixer buffer amplifiers and two adaptive double-balanced mixers, as illustrated in Fig. 1.

With respect to noise figure (*NF*) and linearity (input-referred 3rd-order intercept point, or *IIP*3) requirements of the standards, the receiver operating modes are classified as demanding (**D**, for DCS1800 and 2.1GHz W-CDMA standards), moderate (**M**, for IEEE 802.11b WLAN at 2.4GHz), and relaxed (**R**, for Bluetooth and DECT standards at 2.4GHz), as shown in Table I [3]. Table II summarizes the phase noise (*PN*) requirements for different modes of operation: phase-noise demanding mode is defined by the DCS1800 specification, moderate by W-CDMA and 802.11b/Bluetooth, and relaxed by DECT.

TABLE I. *NF* AND *IIP*3 SPECS PER MODE PRIOR TO LNA.

specs/mode	demanding	moderate	relaxed
NF [dB]	6	10	18
*IIP*3 [dBm]	-9	-12	-16

TABLE II. PHASE-NOISE REQUIREMENTS PER MODE.

spec/mode	demanding	moderate	relaxed
PN@1MHz	-123dBc/Hz	-110dBc/Hz	-100dBc/Hz

These standards illustrate the feasibility of the adaptivity design concept for multi-standard receivers. The procedure of designing for adaptivity presented here could be applied to other standards, if desired.

Characterization of adaptive and multi-standard designs requires figures of merit that refer to multiple operating conditions and/or specifications. We call these adaptivity figures of merit (AFOM). For oscillators, the phase-noise tuning range (*PNTR*) [4] is used to specify the difference between the maximum and minimum achievable phase noise. Two useful AFOM for mixers and amplifiers are the ranges of noise figure and intercept point realized when a particular parameter, e.g., bias current, is adjusted [5].

Based on the desired specifications for each mode (see Tables I and II), the phase-noise tuning range (*PNTR*=123-100-20log(2.4GHz/1.8GHz)=21dB), the noise-figure tuning range (*NFTR*), and the 3rd-order input-intercept point tuning range (*IIP3TR*) for the complete receiver are listed in Table III (performance difference between the demanding and relaxed modes of operation).

TABLE III. RECEIVER PERFORMANCE TUNING RANGES.

NFTR	*IIP3TR*	*PNTR*
12dB	7dB	21dB

III. DESIGN OF MULTI-STANDARD ADAPTIVE CIRCUITS

The design procedure for an adaptive multi-standard circuit is different from that for a single standard. Selection of specifications for quadrature downconverter and design of a quadrature local-oscillator signal generator and quadrature mixers are presented in this section.

A. Multi-Standard Adaptive Quadrature Signal Generator

The quasi-tapped VCO [4], shown in Fig. 2, is used to implement the multi-standard adaptive oscillator.

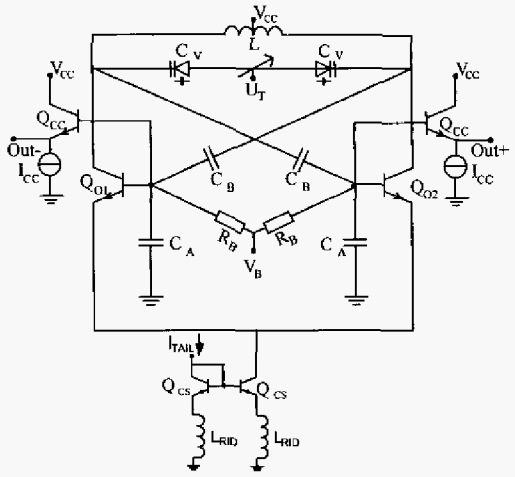

Figure 2. Quasi-tapped (QT) VCO with output buffers.

It consists of a resonating LC tank (L is its inductance and C_V its p-n junction varactor capacitance), two capacitive voltage dividers (C_A and C_B are the quasi-tapping capacitances), and a cross-coupled transconductance amplifier (Q_{O1}-Q_{O2}). A resonant degenerated tail current source is implemented with the low-Q on-chip inductor L_{RID}. It is chosen to resonate with the base-emitter capacitor of transistor Q_{CS} at twice the oscillation frequency ($2f_0$), which reduces the contribution of noise from the bias circuit to the phase noise of the oscillator [4].

The minimum and the maximum loop gain and tail current can be estimated as described in [4]. A *PNTR* of 21.4dB is realized for loop gain between 1.5 and 19 [4], which is sufficient to accommodate the multiple standards selected for this demonstration circuit. For maximum loop gain (19) and lowest phase noise (D-mode), a voltage swing across the inputs (bases) of the transconductor devices of 1.2V is estimated. Once the maximum loop gain is known, the oscillator bias point is determined. The base-bias (V_B) of

2.1V is a compromise between a large output voltage swing and saturation of transconductor devices Q_{O1} and Q_{O2} [4]. For this VCO design, power consumption between the demanding and relaxed operating modes can be reduced by about a factor of 10.

The 3nH tank inductor L is chosen as a compromise between low power consumption and high quality factor in the 2.1GHz band. The inductor is fabricated using 4um thick aluminum top metal in a 50GHz SiGe technology. This differentially-shielded symmetric 3-turn inductor uses a ladder metal filling, has an outer diameter of 320um, metal width of 20um, and metal spacing of 5um. The varactor consists of 2 base-collector diodes with 32 fingers, each 4um wide and 20um long. Metal-insulator-metal capacitances C_A=150fF (C_{II}=90fF) and C_B=600fF are chosen for a quasi-tapping ratio of 1.4. L_{RID} is set to 3.4nH using the resonant-tuning design method.

Quadrature oscillator signals that drive the mixers are derived from a two-stage polyphase filter (see Fig. 1). The first and second stage *R-C* filter sections provide rejection at 1.75 and 2.15GHz, respectively. This allows for higher image-rejection in the 1.8GHz band where low-IF operation is presumed. Image-rejection requirements are relaxed around 2.4GHz, as zero-IF operation is assumed in this band. Common-collector buffers interface the polyphase filter and the oscillator. They consist of 0.5x1.7um^2 transistors and consume 1mA each. The attenuation of the oscillation signal through the passive polyphase filter necessitates a second buffer stage between the filter outputs and the mixer quads. This buffer provides 160mV$_{pk}$ signal swing across 150Ω load resistors while consuming 1.1mA of bias current.

B. Multi-Standard Adaptive Quadrature Downconverter

In order to determine the specifications for the adaptive downconverter, an LNA with NF_{LNA}=2dB, $IIP3_{LNA}$=1dBm and 13dB gain is assumed. For the (quadrature) baseband circuitry, NF_{BB}=14dB and $IIP3_{BB}$=9dBm [6] are chosen.

From Table I and these assumptions for the LNA and baseband circuitry, the noise and linearity required for the quadrature downconverter in the different modes of operation are summarized in Table IV.

TABLE IV. REQUIRED PERFORMANCE FOR THE MSA-QD.

specs/mode	demanding	moderate	relaxed
NF_{QD} [dB]	12.7	19.75	28.8
$IIP3_{QD}$ [dBm]	6.74	3.35	-0.87

When the quadrature downconverter *NF* and *IIP*3 are adapted between 12.7dB/6.74dBm and 28.8dB/-0.87dBm the circuit satisfies the requirements listed in Table I (e.g., the D-mode performance is met with 0dB conversion gain).

The 2nd-order intermodulation performance of the quadrature mixers determines this type of distortion for the complete receiver. Typically, a receiver input-referred 2nd-order intercept point (*IIP*2) better than 45dBm would suffice for the standards under consideration (i.e., quadrature downconverter *IIP*2 should be 58dBm for 13dB LNA gain).

Fig. 3 shows the schematic of the double-balanced mixer [7] that is used to implement the quadrature downconverter.

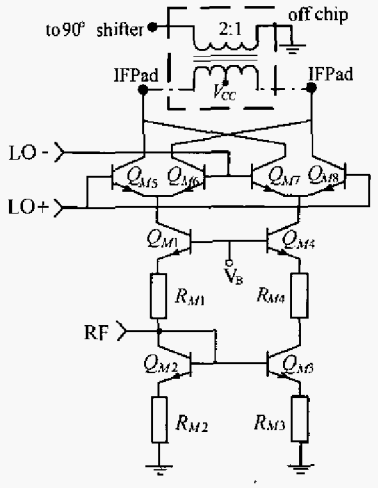

Figure 3. A mixer with an output transformer balun.

The mixer consists of a class-AB input stage ($Q_{M1\text{-}M4}$) for improved linearity, cascoded with switching quad $Q_{M5\text{-}M8}$. The single-ended input is converted into a differential current via common-base stage Q_{M1} and current mirror Q_{M2}, Q_{M3}. Distortion is further suppressed and the RF input impedance match improved by resistors R_{M1}-R_{M4}. Transistor Q_{M4} improves isolation in the input stage and attenuates local oscillator leakage to the RF input.

The transistors and resistors are sized to optimize conversion gain, noise figure, and linearity. For the mixer input stage, transistors $Q_{M1\text{-}M4}$ have a length/width ratio of 40um/0.5um and resistors $R_{M1\text{-}M4}$ are 21Ω. For the switching quad, transistors $Q_{M5\text{-}M8}$ have a length/width ratio of 8um/0.5um. The mixer performance parameters can be adaptively adjusted by changing the mixer bias current, which is set by the voltage applied to the bases of Q_{M1} and Q_{M4}. Simulations show that the downconverter satisfies the D-mode requirements, and that a factor of two reduction in power consumption is realized between its moderate and demanding modes of operation.

IV. EXPERIMENTAL RESULTS

The 0.65x1.0mm^2 testchip (excluding bondpads), shown in Fig. 4, was wirebonded into a 32-pin quad package for testing. A custom printed-circuit board (see Fig. 5) with

bias and supply line filtering was designed for testing. The differential quadrature IF signals are converted to single-ended form via external transformers with a 2:1 turns ratio. A 50Ω-quadrature hybrid combines the mixer outputs at a 70MHz IF, giving an effective mixer load of 200Ω.

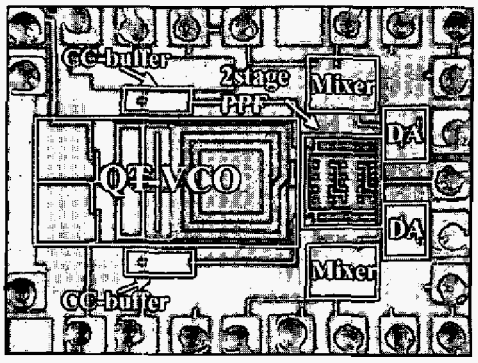

Figure 4. Adaptive downconverter photomicrograph.

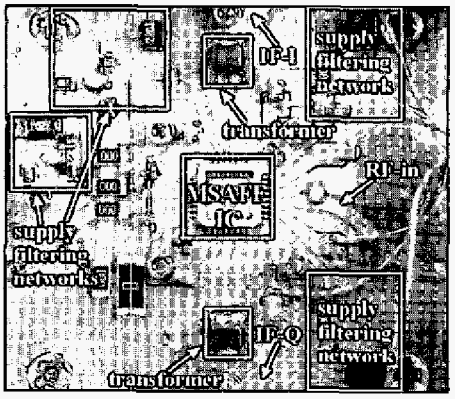

Figure 5. The packaged IC in the test fixture.

The VCO performance was characterized separately from a stand-alone test circuit [4]. Operating from a 3V supply, the adaptive VCO achieves a tuning range of 600MHz, ranging from 1.8GHz to 2.4GHz. By adapting the bias tail current between 0.5mA and 6mA, a phase-noise tuning range of 20dB is achieved, which satisfies the requirements of the five different standards considered [4].

The performance of the complete image-reject downconverter in the D-mode is summarized in Table V.

TABLE V. D-MODE MEASURED PERFORMANCE FOR IR DOWNCONVERTER.

NF[dB]	*IIP*3[dBm]	*gain*	*IRR*	*LO-RF*
13.9	5.5	1.4dB	20dB	-45dB

*IIP*3 can be traded off for an improvement in *NF*. A larger oscillator voltage swing reduces the mixer noise figure but can degrade linearity. The *IIP*2, important for zero-IF operation, is +51dBm. A further improvement of 5dB can be expected after baseband filtering, or by increasing the amplitude of the applied quadrature VCO signals [8]. The conversion gain is limited by mixer load impedance used (2x200Ω mixer load in the test setup would give a power conversion gain of 4.4dB). The measured image-rejection ratio (*IRR*) of 20dB is satisfactory for all standards except DCS-1800, which employs a low-IF architecture. However, the *IRR* can be further improved by quadrature combining the baseband signal on-chip because of improved matching. The downconverter 2 mixers consume 10mA in the D-mode. Control of circuits' bias currents could be realized by additional baseband circuitry.

The implemented downconverter has the potential to meet the specifications of a complete multi-standard receiver. By trading power consumption for performance in an adaptive way, this multi-standard adaptive quadrature downconverter offers more than a factor of 2 reduction in power consumption when switched between demanding and relaxed modes of operation, while still maintaining sufficient functionality. The total current consumption of the testchip (VCO, 2 mixers and buffers) varies from 20.2mA for the demanding DCS1800 standard to 9.9mA for the relaxed DECT standard.

V. CONCLUSIONS

In multi-standard applications, sharing functional blocks between different standards using adaptive multi-standard circuits offers lower power consumption, smaller chip area and may reduce overall cost. The exploratory $2^{nd}/3^{rd}$ adaptive multi-standard image-reject downconverter test design satisfies the requirements of DCS1800, WCDMA, WLAN, Bluetooth, and DECT standards at current consumption levels of 20.2mA, 16.2mA, 15.4mA, 10.4mA and 9.9mA, respectively.

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