Multi-Standard/Multi-Band Adaptive Voltage-Controlled Oscillator

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Abstract – **An adaptive, multi-standard voltage-controlled oscillator satisfying phase-noise requirements of both 2nd and 3rd generation wireless standards is described in this paper (i.e., 1.8GHz DCS1800, 2.2GHz WCDMA, and 2.4GHz WLAN, Bluetooth and DECT standards). A factor of 12 reduction in power consumption with a phase-noise tuning range of 20dB is realized by adapting the VCO bias to the desired application. The VCO achieves –123dBc/Hz, -110dBc/Hz and –103dBc/Hz phase noise at 1MHz offset from a 2.2GHz carrier at supply currents of 6mA, 1.2mA and 0.5mA, respectively.**

Index terms — **voltage-controlled oscillators, loop gain, phase noise, phase-noise tuning, multi-standard/multi-band circuits, adaptive circuits.**

I. Introduction

The demands for new telecom services requiring higher capacity and data rates have motivated the development of broadband, third-generation wireless systems. The coexistence of second and third generation cellular systems requires multi-mode, multi-band, and multi-standard mobile terminals. To prolong talk-time, it is desirable to share transceiver building blocks in these handsets without degrading performance when compared to single-standard transceivers.

It is possible to share components when different standards are not operating simultaneously. In these situations, considerable power can be saved by using circuits that are able to trade-off power consumption for performance on the fly. However, multi-standard front-ends typically use duplicate circuits blocks, or even entire radio front-ends for each standard. Although this approach is simple to implement, it is neither optimal in cost nor in power consumption [1]. For example, designing a voltage-controlled oscillator to satisfy the most stringent specifications consumes more power than necessary when operating under more relaxed conditions [2].

An adaptive, second/third-generation (2G/3G) voltage-controlled oscillator (VCO) that satisfies the phase-noise requirements of DCS1800, WCDMA, WLAN, Bluetooth and DECT standards is described in this paper. Operating from a 3V supply, a tuning range of 1.8-2.4GHz is realized. The VCO phase noise at 1MHz offset from a 2.2GHz carrier is -123dBc/Hz, -110dBc/Hz and -103dBc/Hz for power consumption levels of 18mW, 3.6mW and 1.5mW, respectively. By adapting VCO power consumption to the desired operating scenario, the phase noise of the oscillator can be tuned over a 20dB range with a factor of 12 reduction in power consumption.

II. Design for Adaptivity

The quasi-tapped bipolar VCO [3] shown in Fig. 1 is used to implement the adaptive oscillator. It consists of a resonant LC tank and a cross-coupled transconductor (Q_1, Q_2), where L is the tank inductance, C_V is the tuning varactor capacitance, and C_A and C_B are the quasi-tapping capacitances. Feedback via tapped capacitors (C_A, C_B) maximizes the voltage swing across the LC tank, while active devices Q_1 and Q_2 remain far from heavy saturation. Moreover, freedom to set base bias V_B lower than the supply voltage V_{CC} also allows a large tank voltage, approaching the voltage swing of a CMOS implementation. L_{RID} is degenerating inductor for tail-current source (TCS). Degeneration of the current source is necessary to minimize the phase noise contributed by the bias circuit. The oscillating signal is delivered to the 50Ω measurement equipment using an on-chip open-collector buffer and external transformer balun, *TR*. Gain of the buffer is set by emitter-degeneration resistors, R_E.

The oscillator phase noise performance depends mainly on the components in the ac signal path (e.g., transconductance cell and resonator), when noise contributed by the bias circuit is negligible [4]. However, since the voltage swing across the LC tank depends on the bias current, it is possible to adapt the phase noise of the oscillator to different specifications or standards by changing current I_{TAIL} (see Fig. 1).

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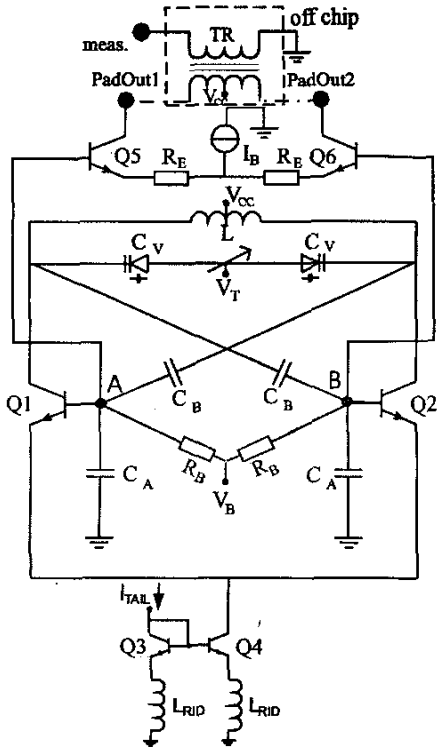

Figure 1. Quasi-tapped LC-oscillator with open-collector buffer.

We call this phenomenon *phase-noise tuning* [5], and the figure-of-merit describing the oscillator's adaptivity to phase noise is the *phase-noise tuning range* (*PNTR*). It is defined as the difference between maximum and minimum achievable phase noise.

A. Bias Noise Suppression

Resonant-inductive degeneration [4] is used to minimize the noise contribution of the oscillator's tail current source. This is done because the contribution of noise on the bias current around even multiples of the oscillation frequency to the overall phase noise of the oscillator is often larger than all other contributions combined [6]. The design procedure used here relies on forming a resonance between the degenerating inductor and the base-emitter capacitance C_Π of tail-current source at twice the oscillating frequency, $2f_0$. Noise power at the output of the current source at frequency $2f_0$ is reduced by $(f_T/2f_0)^2$ when $R_{IN}g_{m,CS}=(f_T/2f_0)^2$, where f_T is the transistor transit frequency, $g_{m,CS}$ the transconductance and $R_{IN}=2\pi f_T L_{RID}$ the impedance seen at the base of the tail-current source transistor. For a $0.5\text{x}10\text{um}^2$ current source transistor and inductance L_{RID} of 3.4nH, simulations predict tail-current noise suppression by a factor of 40, resulting in a 7dB phase-noise improvement.

B. Phase-Noise Tuning

Applying a design procedure developed for single-standard oscillators to multi-standard, multi-mode oscillators would lead to large penalties in power consumption, if the most stringent condition of the most demanding operation mode is satisfied. Selection of the design parameters for an adaptive oscillator is different from that for a single standard. The design of an adaptive, multi-standard VCO (i.e., DCS1800/WCDMA/WLAN–Bluetooth-DECT) will now be outlined.

Given the phase-noise requirements of the corresponding standards (except DECT), the required phase-noise tuning range is *PNTR*=123-110-20log(2.4GHz/1.8GHz)=11dB [7]. The specifications translated to 1MHz offset are: -123dBc/Hz for DCS1800, and -110dBc/Hz for WCDMA, WLAN and Bluetooth. When DECT is included, the *PNTR* increases to 123-100-20log(2.4/1.8)=21dB, as the phase noise requirement for DECT is -100dBc/Hz at 1MHz offset. This *PNTR*, however, is difficult to meet at low supply voltages. Therefore, a design for a minimum *PNTR*=11dB is performed.

Phase noise is related to the VCO loop gain (k) by [3]

$$\mathcal{L}(k) \propto \frac{1+n\cdot(k/2+r_B g_{ms-up})}{k^2 n^2} \qquad (1)$$

The phase-noise tuning range $PNTR(k_1,k_2)$ for a factor k_2/k_1 change in power consumption can be defined as [5]

$$PNTR(k_1,k_2)=\frac{\mathcal{L}(k_1)}{\mathcal{L}(k_2)}=\frac{k_2^2}{k_1^2}\frac{1+n(k_1/2+c)}{1+n(k_2/2+c)} \qquad (2)$$

where $c=r_B g_{ms-up}$, with r_B and g_{ms-up} being the base resistance and start-up (k=1) transconductance of the transistors Q_1 and Q_2 in Fig. 1. $\mathcal{L}$ is the phase noise of the oscillator and $n=1+C_A/C_B$ defines the VCO quasi-tapping ratio.

After eliminating the effect of noise from the biasing tail-current source (i.e., L_{RID}=3.4nH), the required *PNTR* is realized between the loop gain needed for start-up (e.g., k_{MIN}=2), and k_{MAX}=19. k_{MAX} is estimated using Eq. (2). For this loop gain value the lowest phase noise is expected.

Once the loop gain is known, the bias point for the oscillator can be determined. Choosing the base bias potential V_B is a compromise between a large output voltage swing and saturation of the transconductor devices Q_1 and Q_2 in Fig. 1. The voltage swing between the bases of the transconductor (i.e., between nodes A and B in Fig. 1) is related to the loop gain as

$$v_{AB}=\frac{2}{\pi}\frac{I_{TAIL}}{G_{TK}}=\frac{8}{\pi}kV_T \qquad (3)$$

where G_{TK} is the LC-tank conductance and V_T is the transistor thermal voltage, (approximately equal to 26mV at room temperature). For maximum loop gain and lowest

phase noise, a voltage swing of $v_{AB,MAX}$=1.2V is required. To avoid saturation of the transistors in the active part of the oscillator, v_{AB} should not be larger than $2(V_{CC}-V_B+V_{BE}-V_{CE,SAT})/(n+1)$. This worst-case condition is derived assuming the largest base and the lowest collector potential, and, therefore, insures proper operation of the transistors in the active part *at all times*. V_{CC}=3V is the supply voltage, V_{BE} is the base-emitter voltage, and $V_{CE,SAT}$ is the collector-emitter saturation voltage. For this design, a tapped capacitor ratio n=1.4 is chosen. For *PNTR*=11dB, base potential of V_B=2.1V maximizes the output voltage swing, assuming $V_{CE,SAT}$=0.3V and V_{BE}=0.85V. At this bias, a maximal phase-noise tuning range of 19dB can also be achieved for a loop gain between k_{MIN}=1 and k_{MAX}=19.

C. VCO Circuit Parameters

Tank inductor L=3nH is chosen as a compromise between low power consumption and high quality factor (at 2GHz). The inductor is fabricated using 4um thick aluminum top metal in a 50GHz SiGe technology. The 3-turn inductor has an outer diameter d_{OUT}=320um, metal width w=20um and metal spacing s=5um. Using a ladder metal filling scheme [12], the differentially driven symmetric inductor on a 15Ωcm silicon substrate has a quality factor Q_L=25 at 2.1GHz.

The quality-factor of the varactor can also limit the overall tank Q-factor in an integrated oscillator. The quality factor of the collector-base varactor is estimated at Q_C=40 from simulation. The varactor consists of 2 base-collector diodes with 32 fingers, each 4um wide and 20um long.

For a quasi-tapping ratio of n=1.4, the corresponding metal-insulator-metal capacitances C_A+C_{II}=150fF and C_B=600fF are chosen. For effective suppression of the tail-current source noise, L_{RID} is set to 3.4nH using the resonant-tuning design method outlined in the previous section. The degeneration inductor is realized in 0.85um thick second metal layer, as Q for this inductor is not of concern. The inductor outer diameter is d_{OUT}=140um, metal width w=6um, metal spacing is s=1um and it has seven turns. Finally, the open-collector output buffer is designed with R_E=750Ω linearization resistor and bias current I_B=1.1mA.

III. Measurement Results

The chip photomicrograph is shown in Fig. 2. It occupies an area of 700x970um^2, including bondpads. Wire-bonded in a 20 lead RF package, it is tested in a metal fixture with filtering on all bias and supply lines, as shown in Fig. 3. On the test board, three-stage low-pass LC filters remove low-frequency noise originating from the power supply and bias interconnections. Heavy filtering of the supply and bias lines is needed to remove spurs from the VCO output caused by pick-up from the supply and tuning lines. This unwanted interference modulates the VCO in both phase and frequency making accurate phase noise measurements impossible without the employed filtering on bias lines.

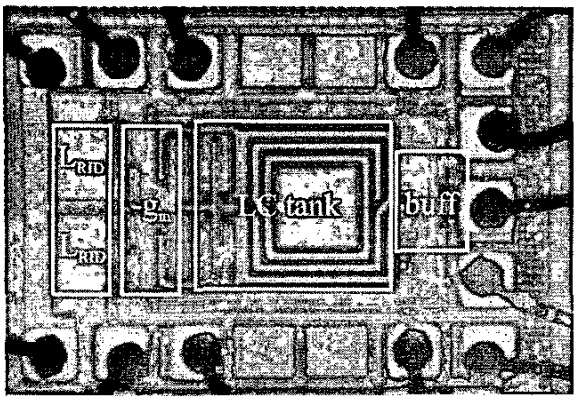

Figure 2. Multi-standard VCO photomicrograph.

For a 3V supply, the frequency tuning range of 600MHz (i.e., output from 1.8GHz to 2.4GHz) is measured, as shown in Fig. 4. This frequency range covers all the bands of interest.

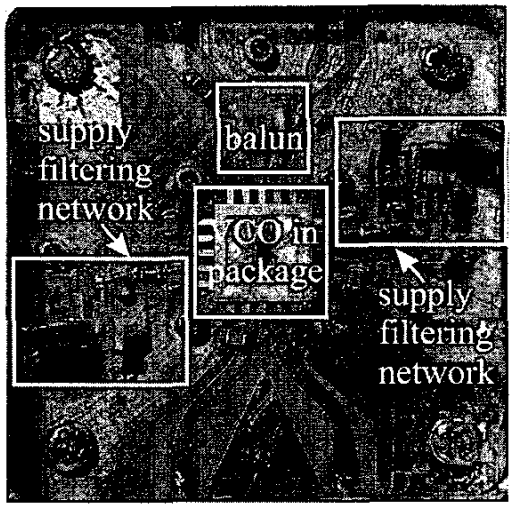

Figure 3. Packaged VCO IC on PCB in test fixture.

Plots of the measured phase noise at 1MHz offset from the 2.2GHz oscillating frequency are shown in Fig. 5. Due to the degeneration resistor R_E=750Ω in the output buffer, an output signal in order of –20dBm is measured in a 50Ω system. This results in a noise floor for the phase noise measurement of -130dBc/Hz, as seen in Fig. 5.

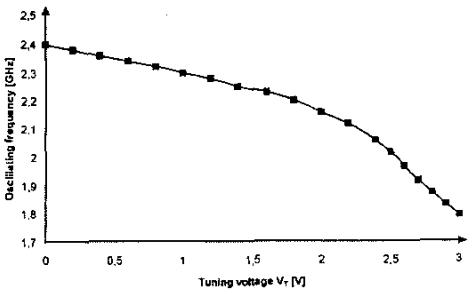

Figure 4. f_0-tuning curve for a 3V tuning voltage.

The operating conditions accompanying the measurements shown in Fig. 5 are listed in Table I. As can be seen from this Table, by adapting the bias tail current between 0.5mA/0.9mA and 6mA, a phase-noise tuning range of 20dB/15dB is achieved. This satisfies the requirements of five different wireless standards, as desired.

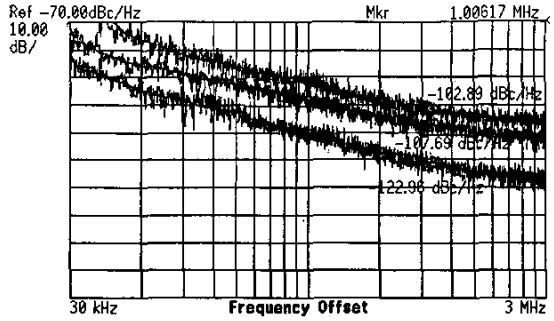

Figure 5. Phase noise at 1MHz offset from the f_0=2.2 GHz.

Note that following the measured phase-noise slope in the range 100KHz-1MHz, a phase noise better than -133dBc/Hz at a 3MHz offset is expected, fulfilling the most stringent DCS1800 requirement at this offset as well.

TABLE I. OSCILLATOR PERFORMANCE AT 2.2GHZ

PhaseNoise@1MHz	*Loop gain*	I_{TAIL}
-123dBc/Hz	20	6mA
-108dBc/Hz	3	0.9mA
-103dBc/Hz	1.7	0.5mA

The power-consumption figure of merit $FOM1=\mathcal{L}(\Delta f_{OFFSET}/f_0)^2 V_{CC} I_{TAIL}$=178 and the tuning-range figure of merit $FOM2=FOM1(f_0/\Delta f_{TUNE})^2$=167 of the oscillator under consideration are compared with other designs from the recent literature in Table II. The adaptive VCO shows a good compromise between phase-noise and frequency-tuning performance. Referring to Leeson's phase-noise formula, Eq. (4),

$$\mathcal{L} = F\frac{KT}{2P_{SIGNAL}}\frac{1}{Q_{TANK}^2}\left(\frac{f_0}{\Delta f_{OFFSET}}\right)^2 \quad (4)$$

FOM2 appears to also be a useful VCO figure-of-merit. It accounts for the frequency dependency of the phase noise as well as the power consumption and the tuning range of the oscillator, the latter related to the LC tank Q.

TABLE II. POWER-CONSUMPTION AND TUNING-RANGE FOM

Reference	*Description*	*FOM1*	*FOM2*
[9]	SiGe	178	148
[10]	SiGe	174	148
[11]	CMOS	172	152
[12]	CMOS	183	150
This work	SiGe	178	167

IV. CONCLUSIONS

By sharing functional blocks among different standards, adaptive multi-band/multi-standard front-ends offer reduced complexity, power consumption, chip area and overall cost.

A 2G/3G adaptive VCO - operating in DCS1800, WCDMA and WLAN-Bluetooth-DECT modes - has been designed which satisfies the phase-noise requirements of these standards at 18mW, 3.6mW and 1.5mW power consumption, respectively.

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