Low-power Adaptive Bipolar Low Noise Amplifier

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Abstract- **In this paper, a low-power adaptive low noise amplifier (LNA) is presented. The LNA is based on a bipolar cascode topology, uses inductive source degeneration and emitter area scaling to achieve noise and input-impedance matching simultaneously. The input impedance and the noise factor were simulated as function of the bias collector current and the results show that both are approximately constant over a range of half a decade of bias current, gracefully degrade when the bias current decreases, thereby saving power.**

1. Introduction

Since cell sizes in 4th generation (beyond 2003) telecom systems that operate at 5, 17 and 40 GHz will be much smaller than in, e.g., GSM, UMTS and GPRS (2nd and 3rd generation), the RF output stage in the transceiver will be no longer responsible for the major part of the transceiver power consumption and thus the power consumption of other transceiver parts become more important. For the front-end, these typically are: the low-noise amplifiers, the mixers, the oscillator system, the active filters, the various gain controls, etc…

Current analog front-end circuits are often designed to perform only one specific task while all key parameters, such as transfer, dynamic range, bandwidth, selectivity, etc. are set by the hardware design and not by the communication system in an adaptive way.

In this paper, we present a design methodology for low noise amplifier circuits (LNA's) that trade dynamic range (determined by its noise figure at one end of this dynamic range and by the linearity and related intermodulation figures at the other end) for power consumption.

As the LNA determines both the noise figure and the input voltage standing wave ratio (VSWR) of the receiver, it is generally required to optimize both in an orthogonal way, i.e., independent of each other. This can be done by applying feedback in the LNA topology.

The LNA design methodology presented in this paper uses inductive source degeneration and emitter area scaling to achieve simultaneously noise and input-impedance matched circuits for a given bipolar IC technology.

Moreover, the LNA performance gracefully degrades for decreasing supply current, thereby enabling the transceiver resource manager to save energy in situations where this degradation can be tolerated.

The outline of the paper is as follows. In Section 2, the BJT noise model is recapitulated, as well its noise factor. Subsequently, Section 3 describes the methodology of the optimization for bias and device geometry. Finally, some simulated results, both for the input impedance parameters and for the noise figure of a LNA at 950 MHz, are presented in Section 4.

2. Bipolar Transistor Noise Model

Bipolar transistors produce a combination of shot noise, thermal noise and flicker noise. The variance for each noise process will be specified in terms of the mean square value associated to a frequency band Δf, which is related to the power spectral density.

Since the device essentially consists of two pn-junctions, diffusion currents through these functions cause shot noise. The mean square value of a shot noise source is given by

$$\overline{i_{nj}^{\,2}}\left(\Delta f\right) = 2qI_j\Delta f \qquad (1)$$

Δf being the noise bandwidth in hertz, q the electron charge (about 1,6 x10^{-19} C) and I_j the value of the junction current in amperes, respectively.

Flicker noise (also called 1/f noise), originating from a variety of imperfections in the lattice, is another source of noise, which can be modeled as a current source between base and emitter. However, for modern transistors, this noise contribution is mostly negligible.

The resistance of the bulk material connected to the intrinsic base-emitter and base-collector junctions produces thermal noise. The (small-signal) bulk resistance of the base, denoted by r_b, is generally much larger than the collector and emitter bulk resistances and thus can be considered to be dominant. Its respective mean square value can be written as:

$$\overline{u_{nb}^{\,2}}(\Delta f) = 4kTr_b\Delta f \qquad (2)$$

where k is Boltzmann's constant (about 1.38x10^{-23} J/K) and T is the absolute temperature in kelvin. The noise contribution of the emitter resistance can be modeled simply by adding its numerical value to the base resistance r_b.

Compared to the noise that is generated in an MOS LNA, a bipolar LNA achieves a lower noise contribution at a lower current consumption [2].

The basic bipolar transistor equivalent circuit can be described with its dominant noise sources and ohmic input circuit. The 1/f noise of the base current and the shot noise of the collector leakage current are for the sake of brevity neglected in the sequel. All noise sources are assumed to be white and uncorrelated.

A chain matrix transformation $\begin{pmatrix} u_{in} \\ i_{in} \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} u_{out} \\ i_{out} \end{pmatrix}$ for the collector shot noise source is applied, yielding the situation of Fig.1. The relevant chain matrix parameters of the intrinsic bipolar transistor are given by [3]:

$$B_{tr} = \frac{-1}{gm - j\omega C_{bc}} \approx -\frac{1}{gm} = -r_e \qquad (3)$$

$$D_{tr} = -\left[\frac{\frac{1}{r_{be}} + j\omega(C_{be} + C_{bc})}{gm - j\omega C_{bc}}\right] \approx -\left[\frac{1}{\beta} + j\frac{f}{f_T}\right] \qquad (4)$$

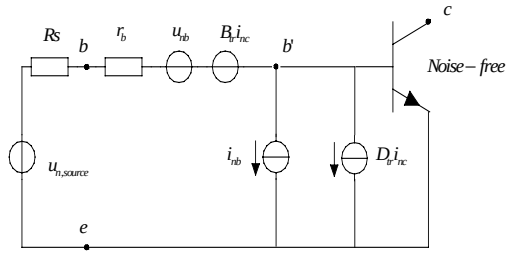

Fig.1 – Transformation of the noise sources to the input using the chain matrix

Where i_{nb} is the noise base current and i_{nc} is the noise collector current.

This expressions for the parameters B_{tr} and D_{tr} take into account the transconductance factor *gm*, the capacitance between base and collector C_{bc}, the capacitance between base and emitter C_{be}, the base emitter resistance r_{be}, the cut-off frequency f_T, the operation frequency *f*, the current gain β and also the angular frequency ω which is equal to $2\pi f$.

The source impedance *Rs* is considered to be purely ohmic with its own noise source $u_{n\ source}$. The noise factor *F* is defined as the ratio of the total available noise to the noise of the source impedance at room temperature.

$$F = \frac{\overline{u^2_{n.source}} + \overline{u^2_{n.network}}}{\overline{u^2_{n.source}}} \qquad (5)$$

We can describe the noise voltage $u_{n\ network}$ in terms of the chain parameters of the transistor. Assume that $\beta >> 1$ and $\omega r_e C_{bc} << 1$, then the noise factor becomes:

$$F = 1 + \frac{1}{Rs}\left[r_b + \frac{r_e}{2} + \frac{(r_b + Rs)^2}{2r_e\beta} + \frac{(r_b + Rs)^2}{2r_e}\left[\frac{f}{f_T}\right]^2\right] \qquad (6)$$

3. Optimization for bias and device geometry

To develop the desired noise optimization technique, we must express the noise figure in a way that takes power consumption into account explicitly. Given a specified bound on the power consumption, the method should then yield the optimum device that minimizes noise.

The input stage of the LNA based on a common-emitter stage as shown in Fig.2. This is commonly used in many RF building blocks [4].

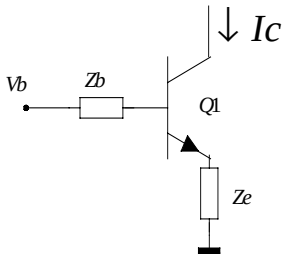

Fig. 2 - Common emitter stage

Note that *Zb* includes the source resistance (*Rs*), base resistance (r_b), the shunt impedance of bias circuit and the impedance of the impedance-matching (*Zo*) network. *Ze* includes the parasitic emitter resistance and the impedance of the degeneration elements.

To improve the linearity, the transconductance stage is usually degenerated by an impedance *Ze*, which can be implemented using resistors, capacitors or inductors. It is easily seen that transconductance stages with reactive (inductive or capacitive) degeneration yield a lower noise figure (NF) than those with resistive degeneration since the degeneration reactance (apart from its loss resistance) does not introduce additional noise.

It appears that the inductively degenerated [5,6] transconductance stage is more linear than the resistively degenerated stage, which in turn is more linear than the capacitive degenerated transconductance stage with the same transconductance and bias current

In order to offset the total loss of the matching circuits and improve linearity, inductors are also employed in the matching circuit of the LNA.

3.1 Noise Figure optimization

Given the noise figure expression in Equation (6) for a bipolar transistor and assuming $r_e = V_T/Ic$ and the cut-off frequency given by well-known expression $f_T = gm/2\pi(r_e(c_{jE}+c_{jC})+\tau_o)$, then the noise factor can be optimized with respect to the bias condition. Assuming that τ_o, c_{jE}, c_{jC} and r_b are current-independent and noting that r_e is current-dependent we can differentiate and nullify the noise factor expression to determine the optimum value for collector current.

Taking $dF/dIc = 0$ yields**:**

$$Ic,opt = \frac{V_T}{(r_b + Rs)} \cdot \sqrt{\frac{1 + (r_b + Rs)^2 . f^2 . 4\pi^2 . (c_{jE} + c_{jC})^2}{\frac{1}{\beta} + f^2 . 4\pi^2 . \tau_O^2}} \quad (7)$$

We can see that the optimization current *Ic,opt* for minimum noise increases weakly with frequency. Using this optimum collector current in the expression of the noise figure yields a minimum noise figure, which equals:

$$F_{Icopt} = 1 + \frac{1}{Rs}\left[\begin{array}{l} r_b + (r_b + Rs)^2 . f^2 . 4\pi^2 . (c_{jE} + c_{jC}) \tau_O \\ + \frac{(r_b + Rs)}{Rs} \cdot \sqrt{\left[\frac{1}{\beta} + 4\pi^2 . f^2 . \tau_O^2\right]\left[1 + 4\pi^2 . f^2 . (c_{jE} + c_{jC})^2 . (r_b + Rs)^2\right]} \end{array} \right] \quad (8)$$

3.2 Input impedance optimization

The aim of the input impedance optimization is to obtain simultaneously noise and input impedance matched circuits.

To achieve both noise matching and impedance matching a passive network is designed. However, the passive network can also degrade the noise figure. The loss of the input matching circuit degrades the noise figure performance of the LNA and its gain performance.

In order to minimize the losses in the passive network around the transistor, the size of the transistor is first designed so that the transistor becomes noise matched to the characteristic impedance of the system, typically 50 Ω, at the desired frequency. See the horizontal arrow in Figure 3.

The emitter length is then adjusted so that the optimum source resistance *Rsopt* equals *Zo* (50 Ω) at the minimum noise current density and at the frequency *f*. This corresponds to the vertical arrow in Fig. 3.

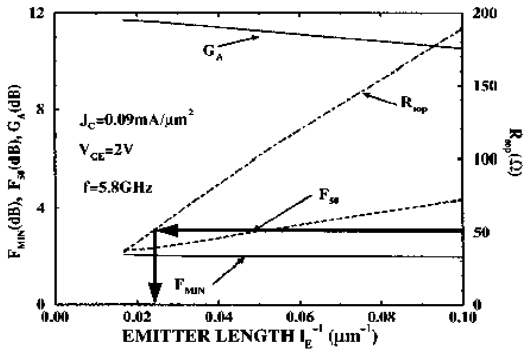

Fig.3 – Noise parameters as function of the emitter length [2]

The real part of the optimum noise impedance is now matched to 50 Ω without having degraded the minimum noise figure.

The general expression for noise factor can also be described in terms of the minimum noise figure and the source admittance, as given by classical noise theory:

$$F = F\min + \frac{Rn}{Gs}[(Gs - Gopt)^2 + (Bs - Bopt)^2] \quad (9)$$

where

$$F\ \min\ = 1 + 2.Rn[Gopt\ + Gc\ ] \quad (10)$$

Rn being the noise resistance, *Gs* the noise conductance, *Gsopt* the optimum noise conductance, *Bs* the noise susceptance and *Bsopt* the optimum noise susceptance, respectively.

The noise resistance determines the radius of constant noise figure circles in the Smith chart [7]. *Rn* is essential for predicting the variation of the noise figures. With decreased *Rn*, the constant noise contours have greater separation and larger diameter for a given *Fmin*, providing greater tolerance to circuit variations.

As described in [7], *Gsopt* is different from the input conductance, whereas *Bsopt* is equal to the complex conjugate of the input susceptance of the device. This is a fundamental characteristic of both bipolar and field-effect transistor and underlines the requirement for separate treatment of matching the real part of the input impedance and the real part of the optimum noise impedance.

Thus, contours of constant noise factor are circles centered around (*Gopt*, *Bopt*) in the admittance plane. They are also circles when plotted on a Smith chart because the mapping between the two planes is a bilinear transformation, which preserves circles.

In [2], expressions for the optimal noise resistance (*Rsop*), the noise resistance (*Rn*), the optimum noise admittance (*Ysop*), and the minimum noise figure (*Fmin*) are derived. It is also described in [2] that, in order to achieve optimal low-noise and input impedance matching at the desired frequency, the emitter length (*Le*) of the bipolar transistor in the LNA can be optimized, since the expressions for *Rn* and *Rsopt* scale as Le^{-1}, whereas the expression for *Ysopt* scales as *Le*.

When we develop the expressions for the optimal conductance and the optimal susceptance for the minimum noise, thus achieving the constant noise figure circles in the Smith chart, we obtain:

$$Bsopt = -\frac{f}{2 f_T . Rn} = -\left(\frac{f}{f_T}\right)\frac{gm}{1 + 2.gm.(r_e + r_b)} \quad (11)$$

$$Gsopt = \frac{f}{f_T . Rn} \cdot \sqrt{\frac{Ic}{2.V_T} . (r_e + r_b)\left(1 + \frac{f_T^2}{\beta o . f^2}\right) + \left(1 + \frac{f_T^2}{\beta o . f^2}\right)} \quad (12)$$

3.3 LNA design

When multistage amplifiers are designed, input amplifiers are required to have high gain and low noise performance. In order to meet the gain requirement, in multistage amplifiers, usually two stages are employed. The cascode amplifier, comprising a CE and a CB stage,

can be regarded such a two-stage amplifier. Its properties are as listed below:

1. The current is fed from the common base to the common emitter by the same bias line;
2. It has a high voltage gain;
3. The cascode LNA has the advantage of variable control;
4. The use of a cascode improves the LNA's reverse isolation;
5. The LNA's stability is improved whereas it might be compromised without the cascode, due to interaction between the inductive load of the first stage and the input-matching network through C_{bc}.

Thus, in this way, it is possible to achieve low noise, low distortion and low power consumption simultaneously. For this reason, the cascode amplifier is chosen as the basic configuration for the LNA.

Having established the LNA's topology, we now discuss selection of inductor values and transistor sizing.

Whatever the value of the input resistive term, it is important to emphasize that it does not bring with it the thermal noise of an ordinary resistor because a pure reactance is noiseless. We may therefore exploit this favorable property to provide the specified input impedance without degrading the noise performance of the amplifier.

The architecture for the input circuit is depicted in Figure 4. The advantage of this architecture over possible alternatives is the possibility of achieving the best noise performance.

Inductance *Le* is chosen to provide the desired real part of the input resistance (equal to *Rs*). Since the input impedance is purely resistive only at resonance, an additional degree of freedom, provided by inductance *Lb*, is needed to guarantee this condition.

Connecting an additional inductor *Lb* in the base effectively cancels the reactance due to the input capacitance (*Cin*) of the device and it transforms the optimum noise reactance of the amplifier to 0 Ω [8].

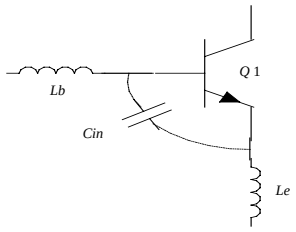

Fig. 4 – Input impedance matching

Thus, it holds:

$$Zin = Zo + j\omega(Lb + Le) - \frac{1}{j\omega Cin} \qquad (13)$$

where the input capacitance $Cin = (gm.\tau o + c_{TE}) + c_{TC.}$

We can see from this expression for the input impedance, that it is purely resistive at only one frequency (at resonance) and provides a narrow-band LNA.

The value for the emitter inductance (*Le*) is given by:

$$Le = \frac{Zo}{2.\pi.f_T} \qquad (14)$$

Note that *Le* affects the optimum source reactance *Xsopt*, by adding a term proportional to $-2.\pi.f.Le$.

Finally, the desired value for the base inductance (*Lb*) can be described by [2]

$$Lb \cong \frac{1}{\omega^2.Cin} - Le \qquad (15)$$

The circuit diagram of the complete LNA is depicted in Fig.5. *Q*1 and *Q*2 form the common-emitter and the common-base stages of the cascode topology, respectively. *Q*3, *Q*4 and the two 5-kΩ resistors implement the bias circuit of the LNA. *Cs* couples the RF signal into the LNA. The collector-substrate capacitance of *Q*5 acts as a decoupling capacitor. Subsequently, the geometry of the transistors and the numerical values of the inductors can be calculated, in line with the design procedure, unfolded above.

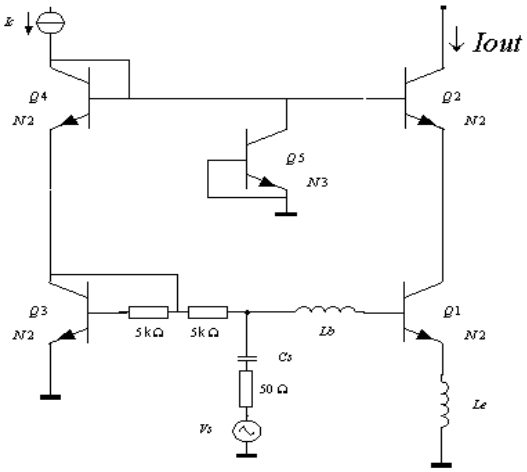

Fig.5 – Circuit diagram of the implemented LNA

4. Simulation

To validate the design procedure outlined above, the LNA circuit was designed for GSM applications (f ≈ 950 MHz), to be implemented in our in-house bipolar semi-custom IC process, SIC3A [9,10]. Typical transistor parameters are $f_{T,\mathrm{npn,max}}$ = 15GHz and $\beta_{F,\mathrm{npn}}$ = 150 (smallest emitter size). Three types of npn transistors are available, differing in emitter area only, being N1 (Re=8Ω), N2 (Re=1Ω) and N3 (Re=0.125Ω). The noise factor, noise resistance and input impedance for minimum noise as a function of the bias current *Ic* and the emitter resistance were derived, thus enabling us to choose the proper emitter length.

The equivalent real and imaginary parts of the input impedance as function of the bias collector current were simulated and are plotted in Figure 6.a and Figure 6.b, respectively.
Some numerical values are given in Table 1. We can see from Table 1 that the input impedance is both constant and close to 50Ω in the range of 0.125mA to 2mA for the bias current.

Ic (mA)	Zin (Ω)	Re(Zin)	Im(Zin)
0.125	74.00	31.06	-67.17
0.25	60.90	37.82	-47.73
0.5	46.31	39.78	-23.70
0.75	42.46	40.75	-11.92
1	42.33	42.03	-5.10
1.25	43.43	43.42	-0.52
1.5	44.94	44.84	2.91
1.75	46.28	46.23	5.687
2	48.25	47.58	8.04

Tab.1 – Input impedance parameters for *f* = 950 MHz

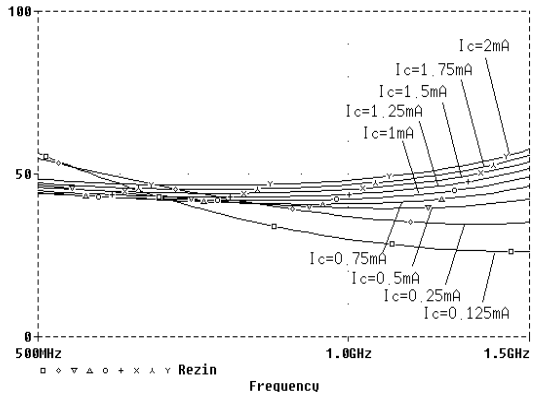

Fig. 6.a – Real part of the input impedance for different collector currents

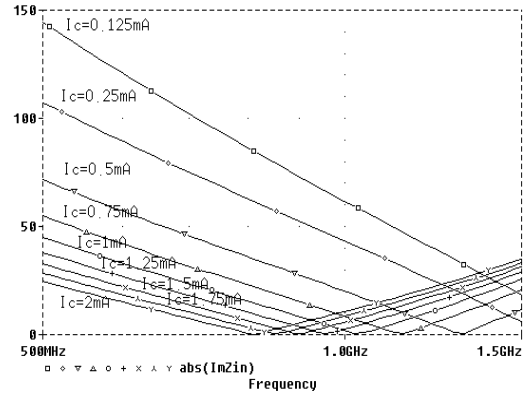

Fig. 6.b – Imaginary part of the input impedance, for different collector currents

Employing Equations (14) and (15), for Ic = 1mA and scaling factor of 3, we obtain the values for the emitter inductance, *Le* = 5.6 nH and for the base inductance, *Lb* = 4.2 nH, respectively.

Table 2 depicts the equivalent input noise voltage, the noise factor and the noise figure, respectively, as a function of the collector current. Please note that these values are not optimal because of the limited choice of the emitter geometry in the chosen semi-custom IC design process.
Finally, we have evaluated the linearity of this particular LNA. Although there are many measures of linearity, the most commonly used are the third-order intercept point (IP3) and the 1-dB compression point (P_{1dB}) [11,12]. From PSPICE simulations, we derived the linearity parameters P_{1dB} and IP3 to be equal to –14 dBm and 35 dBm, respectively.

Ic (mA)	en (input)/√Hz	Noise Factor	Noise Figure
0.125	4.34e-9	24.6	13.9
0.25	2.19e-9	6.99	8.44
0.5	1.30e-9	3.11	4.92
0.75	1.13e-9	2.58	4.11
1	1.09e-9	2.47	3.92
1.25	1.10e-9	2.51	3.99
1.5	1.12e-9	2.56	4.08
1.75	1.14e-9	2.63	4.19
2	1.17e-9	2.72	4.34

Tab.2 – Noise parameters for *f* = 950 MHz

5. Conclusion

An alternative methodology to LNA design for low-power adaptive narrow-band communications systems has been proposed in this paper. The design methodology introduces a noise optimization technique, that maintains a good input impedance matching by employing inductance source degeneration and emitter area scaling of the bipolar transistor in a cascode topology. The resulting circuit operates at 950 MHz, exhibits good input impedance, close to 50 Ω, and constant noise factor, 2.5, in the range of 1mA to 2mA for the bias current.

6. References

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