A Novel Chip Design for Real-Time Measuring of Neural Signals

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Objectives

Development, use and testing of a new Neural Response Amplifier (NRA) to support neural response measurements in cochlear implants (i.e. NRI, NRT, ART of I/O curves, refractivity, pulse trains adaptivity) with high stimulation rates, low noise levels and sufficient dynamic range (>120dB) that allows for real-time continuous measurements of eCAPs.

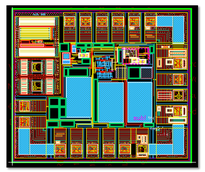

Fig 1. Chip v2: development layout

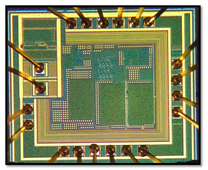

Fig 2. Chip v2: micrograph of the actual chip

Background

Potentially, eCAP data could provide insight in what the optimal stimulation strategy should be, and how to program the current levels of the implant for the individual patients.
However, currently used NRA systems are not equipped to handle the large dynamic range that is necessary to simultaneously measure the small potential of the eCAP (10 µV) in conjunction with the large potential of the pulse (up to 10V).

Other shortcomings of currently used NRAs are that:

- they are bulky and are not energy efficient
- they are not able to read out multiple electrodes at the same time
- they have a high internal noise level, requiring averaging, and thus cannot be used in real-time closed-loop devices.
- they are not able to cope with the electromagnetic interference caused by the RF signal used for the energy and transcutaneous data transfer.

Ultimately, we expect the NRA chip design to be able to record neural responses (i.e. eCAPs) during continuous stimulation by means of additive companding, a process in which the dynamic range of a signal is reduced for recording purposes and then expanded to its original value.

Methods

System design
The system design is based on an additive companding output system that is able to record the eCAPs from the stimulated auditory nerve with a high dynamic range, thereby covering both stimulus artefact (up to 10V) and the neural response (down to 10µV).
The chip uses stepwise compression, each step provides a trigger signal. These triggers can be used for signal reconstruction.
The first 4 bits in analog-to-digital conversion are generated by the chip, the other 18-bits are provided by the analog-to-digital converter (ADC).
There are three proposed stages of NRA chip design
V1: basic chip design with external controller and ADC. For proof of principle purposes only.
V2: chip design with internal controller with external ADC. This chipset will be validated *in vitro*.
V3: based on validation results improved chip design with internal ADC. Will be used *in vivo* (guinea pig) experiments.

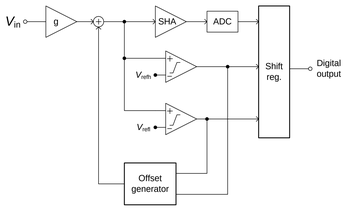

Figure 3: circuit schematic of initial NRA chip design:
- V_{in} chip input (stimulus artefact + neural response)
- V_{refh}/V_{refl}: high and low offsetting for additive signal companding

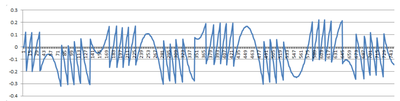

Figure 4: example of additive companding of a sine wave signal of 1V

Chip validation:
Chip validation is performed *in vitro* at the LUMC
Setup:

- LabView® software
- Board with v2 NRA chip design
- External ADC: NI PCI-6040E
- Test signals for *in vitro* validation (2 channels)
  - Sine wave 2000 Hz 1-9V
  - Combined signal, trapezoid pulse, sine wave 3000 Hz amp 10mV

Results

Signal reconstruction
The first generation of the chip was hampered by the external control system. Currently the second chip is being validated. The system functions under certain input signal constrictions.
MATLAB® was used to optimize the reconstruction algorithm for the compressed sine wave output signal (fig. 5/6).

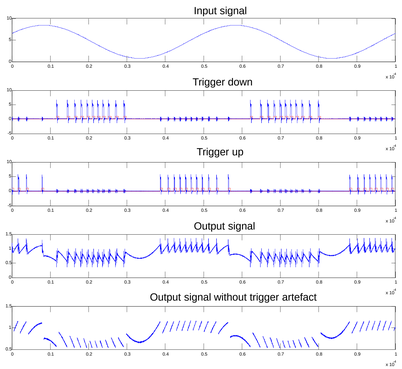

Figure 5: The sine wave output signal, combined with digital trigger pulse data was used to reconstruct a sine wave signal which was processed through additive companding by chip v2.

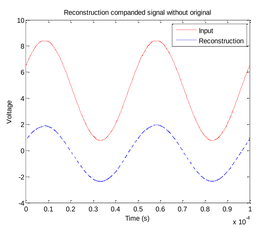

Figure 6:The input data was compared to the reconstructed signal. A decrease in amplitude was seen in the reconstructed sine wave signal.

In vitro testing
To test if the chip v2 would work with an approximation of a neural response signal with pulse artefact, two separate signals (pulse/tone burst waveform) were created using Labview® and combined after decreasing the amplitude of the second (tone burst) signal by 0.001 (-30 dB) (fig. 7).

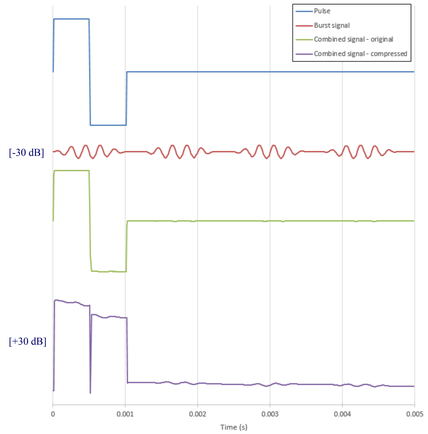

Figure 7: From top to bottom: pulse 1ms, tone burst waveform (4x 1 ms) 5000 Hz, combined signal: pulse + tone burst (4x) 5000 Hz amp reduced -30 dB, compressed combined signal amplified +30 dB.

The stimulus pulse, containing a tone burst waveform was processed by the chip v2. After processing the large stimulus artefact was cut by the triggered additive companding, the tone burst wave however, was clearly visible by reducing the total amplitude of the signal (fig 8). For use with our 12-bit ADC, the compressed chip output was 1000x amplified (+30 dB)

Because the current hardware was not able to record the trigger information, further reconstruction of the signal was not possible. New hardware is currently used for this purpose.

Conclusions

During validation testing of the second generation chip design, the chip was able to compress the input signals. However, there were some limitations in the v2 chip design, the input signal is not yet able to handle negative input voltages and steep slopes in the input signal. There also is an variable offset during stepwise compression, which makes signal reconstruction and averaging more difficult.

These limitations will be resolved in the third generation that will also fully integrate the control systems and ADC in a single design.
With adjustments to the current (v2) chip design based on the validation results we aim to use the v3 chip design to enable eCAP recordings during continuous (speech) stimulation over the whole dynamic range.

Further development

Based on the validation results of the second (v2) NRA chip design, a third generation chip design is currently developed at the TU Delft (fig. 9).
This design will be able to cope with negative input voltages, as well with steep slopes in the input signal.
By using two coupled chips simultaneously, the offset during stepwise compression will be more stable, to provide improved signal reconstruction.

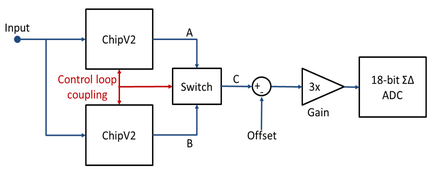

Figure 8: Third generation chip design with integrated analog-to-digital converter (ADC) and use of two coupled chips.