The design of Low-Voltage Low-Power Analog Integrated Circuits and their Applications in Hearing Instruments

Wouter Serdijn

The design of Low-Voltage Low-Power Analog Integrated Circuits and their Applications in Hearing Instruments

PROEFSCHRIFT

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A change of speed
A change of style
A change of scene
With no regrets

A chance to watch
Admire the distance
Still occupied
Though you forget

Joy Division: New dawn fades

to Marjo

Contents

Chapter 1

Introduction

"What do you like doing best in the world, Pooh ?"
"Well," said Pooh, "what I like best –" and then he had to stop and think.
Because although Eating Honey was a very good thing to do,
there was a moment just before you began to eat it
which was better than when you were,
but he didn't know what it was called.

A.A. Milne: The house at Pooh corner

Low-voltage low-power circuit techniques are applied in the area of battery-operated systems. In particular, they are of crucial importance for implantable devices, such as pacemakers, blood flowmeters and auditory stimulators [1, 2, 3, 4, 5, 6, 7]. Also, as more and more complex systems are being integrated on the same chip, area minimization is becoming of primary importance. Typical examples are portable radios, hand-carried radiotelephones, pagers and hearing instruments [8, 9, 10, 11, 12, 13]. As the size of batteries is now becoming the limiting factor, it is not sufficient to reduce the size of bulky components by integrating them; the reduction of the power dissipation is also very important. As a consequence, the key point is to develop, simultaneously, both low-voltage and low-power operating integrated circuits in order to reduce the battery size and chip area.

There is, however, no general design theory available for the design of low-voltage low-power integrated circuits. In most cases we have met in literature, the design is started by choosing a suitable circuit implementation from the large variety of conventional electronic circuits. Then, this circuit is adapted in order to fit within its new environment. As an example we mention an ordinary differential pair equipped with bipolar transistors.

When used in practical circuits, the differential pair needs an extra DC voltage reference. Especially in low-voltage circuits, this source must be quite accurate in order to fully exploit the possible output voltage swing of the differential pair

[14]. Further, if the stage has to be biased individually, both base connections need a resistive path to ground, to make the flow of base current possible. This measure affects the small-signal behavior and noise properties. Apart from this, in low-power circuits very large resistors are needed, which entails a large chip-area consumption. In [15] it has been shown that a differential pair is only one of four configurations that exist for the implementation of a single differential CE stage and that one of the other configurations, the 'alternative differential pair', is much better suited for application in low-voltage low-power analog integrated circuits.

Another example concerns the design of a class-AB output stage. In most conventional output stages, e.g., in op amps or audio amplifiers, this output stage contains two complementary output transistors in CC configuration (i.e. with their emitters tied together) driving the load. This circuit, however, requires a minimum supply voltage that is larger than the sum of the base-emitter voltages of both transistors. For circuits that use a 1-V power supply other solutions had to be found [16, 17, 18].

Various definitions of the term 'low-voltage' can be found in literature. Designers of digital circuitry often think of 3.3 V as being low voltage. This is not surprising, as today most of the digital circuits operate at 5 V. From this point of view 3.3 V, which is about to become the new world standard, is indeed low voltage. From the application side, a circuit or system is often denoted as low voltage when it operates on a single battery. This, of course, depends on the type of battery one uses. A single zinc-air or mercury battery cell at the end of its lifetime delivers only 1 V, whereas a single lithium cell delivers as much as 3 V. For this reason we have chosen for a more design-driven definition: **low-voltage analog circuits do not have two or more junctions in series between two supply rails**. All the circuits described in this work comply with the above definition.

In defining the expression 'low-power' the situation is more complicated. Preferably, a circuit should require as little power as possible: and every power reduction of a circuit, with respect to its earlier version while maintaining its functionality, makes it more 'low-power'. Of course, this process cannot go on forever. A lower bound is formed by the information capacity C of the electronic circuitry:

$$C = B \log \left(1 + \frac{S}{N} \right) \tag{1.1}$$

B being the bandwidth of the circuit and S/N the ratio of the signal power to noise power under the assumption of Gaussian noise [19].

In most cases, the bandwidth properties of an electronic circuit depend on those of the transistors used inside. A quantity serving as a figure of merit for the bandwidth properties of a transistor is the transit frequency f_T. In Figure 1.1, the transit frequency has been depicted as a function of the bias current for a typical small integrated bipolar transistor in a high-frequency process. We can see that

f_T has a maximum at about 100 μA, while it becomes proportional to the bias current for lower bias currents.

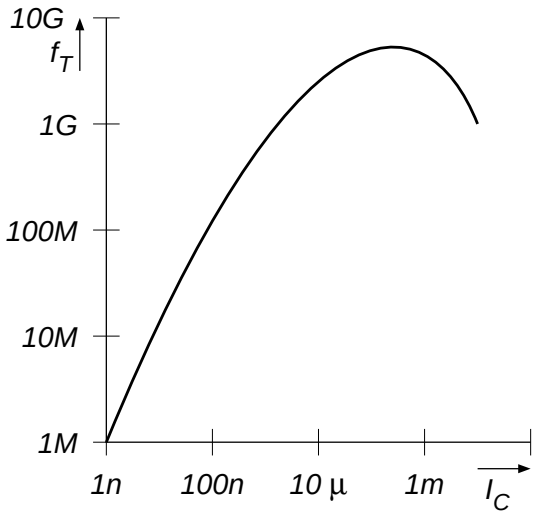

Figure 1.1: Transit frequency f_T versus the bias current I_C of a typical integrated bipolar transistor

An important source of noise in electronic circuits is related to the stochastic nature of the flow of charge carriers that pass a potential barrier. Because of the discrete nature of the emitted charge carriers, mostly electrons, the current is quantized [19]. As a consequence, the maximal signal-to-noise ratio also is approximately proportional to the bias current.

Since both the bandwidth and the maximal signal-to-noise ratio are proportional to the bias current, we thus have to face the fact that low-power integrated circuits have a smaller information capacity than conventional integrated circuits that do not have this 'low-power' constraint.

Since 1986, the Electronics Research Laboratory of the Delft University of Technology, Faculty of Electrical Engineering has had a project group 'low-voltage low-power electronics'. To date, the main research field has been the development of circuits for hearing instruments and the underlying design theory. This work has been carried out partly under the group's own control and partly in cooperation with industry, and has resulted in two new generations of hearing instruments, both now in production. Moreover, these research efforts have increased both knowledge and insight into the problems which specifically concern this specialized branch of electronics. They, in turn, have resulted in specific design methodologies, device modeling and circuit architectures.

This thesis deals with the design of low-voltage low-power analog integrated circuits and their applications in hearing instruments. Its purpose is twofold: to offer a design procedure for low-voltage low-power circuits in general, and to give a

new concept for a hearing instrument. It is assumed that the principal performance requirements of the circuits are dictated by the overall system requirements, which cannot be compromised in achieving low-voltage low-power operation. In view of the foregoing, it becomes clear that a low-voltage low-power design constraint entails special-purpose rather than general-purpose circuits. For this reason, the typical general-purpose integrated circuit is not the focal point of this work. As, at the start of the research, low-threshold BiCMOS IC processes were not yet well specified for our purpose, there is an emphasis on implementations in bipolar realizations. However, many of the ideas expressed here are also valid for other processes.

In Chapter 2, it is shown that low-voltage low-power electronics operate best in 'the current domain'. In Chapter 3, transistor models for the large-signal, the small-signal, and the noise behavior, are discussed for bipolar transistors in a low-voltage low-power environment. With these tools various important low-voltage low-power functional blocks can be designed. These are: amplifiers (Chapter 4), automatic gain controls (Chapter 5) and filters (Chapter 6). These three functions are the main functions that can be found in a hearing instrument. Their application in a universally applicable IC for hearing instruments is presented in Chapter 7.

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Chapter 2

Ports

Et duodecim portae duodecim margaritae sunt,
et singulae portae erant ex singulis margaritis.
Et platea civitatis aurum mundum
tamquam vitrum perlucidum.

Apocalypsis Ioannis, 21:21

2.1 Introduction

In this chapter we look at low-voltage low-power analog integrated circuits from a mainly network-theoretical point of view.

All electrical circuits or networks can be characterized by two fundamental quantities. Although other quantities like energy and charge are equally well possible, they are usually taken to be voltages and currents. The properties of the network are then completely specified by the relationships among these voltages and currents and the network itself can be considered to be 'a black box' with terminals connected to the external electrical world.

The simplest networks are two-terminal networks or one-ports. Because of the charge conservation, the current flowing into one terminal equals the current flowing out from the other terminal. This condition is called the port constraint. Examples of one-ports are:

- ideal resistors
- ideal capacitors
- ideal inductors
- independent sources (e.g. voltage or current sources)

- series and parallel connections of one-ports

In Figure 2.1, a one-port and its sign conventions are given.

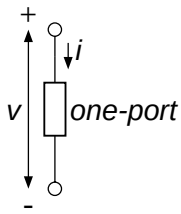

Figure 2.1: A one-port together with its sign conventions

In a linear system, for all these one-ports, the relationship between the current and the voltage, usually given by a complex impedance, at the network terminals specifies the behavior of the one-port completely.

When we are interested in the transmission of information from one point to another, the number of pairs of terminals becomes important. An important example of this class of network is the two-port. A two-port is a network with two pairs of terminals connected to the external electrical world, provided that these pairs of terminals behave as ports. There are some basic network elements that behave as two-ports, no matter how the terminal pairs are connected to the remainder of the circuit. These are:

- controlled sources, i.e.,
  - current-controlled voltage sources
  - voltage-controlled voltage sources
  - current-controlled current sources
  - voltage-controlled current sources
- ideal transformers and gyrators
- nullors
- connections of two-ports, i.e.,
  - series-series connections
  - parallel-parallel connections
  - series-parallel connections
  - parallel-series connections
  - cascade connections

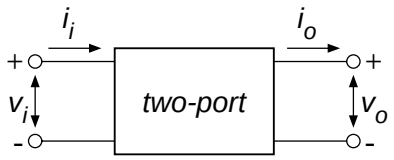

Figure 2.2: A two-port together with its sign conventions

In Figure 2.2 a two-port and its sign conventions are given.

The relationships between the two currents and the two voltages at the terminal pairs specify the two-port completely. Although there are many ways of writing these equations, we use the transmission parameters in this work [1]. The two-port equations here express the input quantities as functions of the output quantities and take the form

$$v_i = Av_o + Bi_o \tag{2.1}$$
$$i_i = Cv_o + Di_o \tag{2.2}$$

or in matrix notation

$$\begin{pmatrix} v_i \\ i_i \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_o \\ i_o \end{pmatrix}$$

in which A, B, C and D are the transmission parameters or the chain parameters. The last name indicates that these parameters are natural ones to describe the cascade or chain connection of two-ports. The transfer parameters μ, γ, ζ and α are their reciprocal values and are defined as follows:

voltage gain factor	$=$	μ	$=$	$1/A$	$=$	$v_o/v_i\|_{i_o=0}$
transconductance factor	$=$	γ	$=$	$1/B$	$=$	$i_o/v_i\|_{v_o=0}$
transimpedance factor	$=$	ζ	$=$	$1/C$	$=$	$v_o/i_i\|_{i_o=0}$
current gain factor	$=$	α	$=$	$1/D$	$=$	$i_o/i_i\|_{v_o=0}$

When the source impedance Z_S and the load impedance Z_L are known, then the input impedance Z_i and the output impedance Z_o of the two-port are given by

$$Z_i = \frac{AZ_L + B}{CZ_L + D} \tag{2.3}$$
$$Z_o = \frac{B + DZ_S}{A + CZ_S} \tag{2.4}$$

A special two-port which has proved to be very useful for modeling and designing circuits containing feedback is the nullor [2]. A nullor can be considered

to be an ideal two-port of which the transmission parameters all equal zero, or all transfer parameters are infinite. The active part of a circuit with overall feedback can often be considered as an approximation of a nullor, thereby making it easier to estimate its behavior in a feedback configuration.

2.2 Reducing errors

Any transmission of information from the input of a network to the output is perturbed by both stochastic and systematic errors. By stochastic errors we mean inaccuracies in the input-output relation caused by noise or interference. Though impossible to eliminate, their influence can be minimized by a proper design strategy. Systematic errors arise from network imperfections, such as offset, non-linearity, inaccuracy, drift and temperature dependence. Their influence can be reduced by means of:

- compensation
- error feedforward
- negative feedback (including indirect negative feedback)

2.2.1 Compensation

When the actual input-output relation of a network differs from the desired input-output relation, but in such a way that there is a unique relation between the input and the output quantities, there is no irretrievable loss of information. It is therefore possible to pass the signal through a second network which compensates for the error in the original input-output relation.

Compensation with one-ports

When two one-ports are connected in series, the currents in both one-ports are equal while the voltage across the connection is the sum of the voltages across each one-port. Compensation of even-order terms in the voltage-current relation occurs when two identical one-ports are connected in anti-series.

When two one-ports are connected in parallel, the voltages across each of them are equal, while the total current equals the sum of the currents flowing through each one-port. Compensation of even-order terms in the current-voltage relation occurs when two identical one-ports are connected in anti-parallel.

Compensation with two-ports

Two two-ports can be combined to obtain a new two-port with different characteristics. Like one-ports, the ports of a two-port can be connected in series or in parallel. We thus have four possibilities:

- the input ports are connected in series and the output ports are connected in series
- the input ports are connected in parallel and the output ports are connected in parallel
- the input ports are connected in series, while the output ports are connected in parallel
- the output ports are connected in parallel, while the input ports are connected in series

If we define the transmission parameters of the first and the second two-port as indicated by their indices, we are able to express the transmission parameters (without indices) of the connection as follows [3]:

series – series connection

$$A = \frac{A_1 C_2 + A_2 C_1}{C_1 + C_2} \tag{2.5}$$

$$B = B_1 + B_2 + \frac{(A_1 - A_2)(D_2 - D_1)}{C_1 + C_2} \tag{2.6}$$

$$C = \frac{C_1 C_2}{C_1 + C_2} \tag{2.7}$$

$$D = \frac{D_1 C_2 + D_2 C_1}{C_1 + C_2} \tag{2.8}$$

parallel – parallel connection

$$A = \frac{A_1 B_2 + A_2 B_1}{B_1 + B_2} \tag{2.9}$$

$$B = \frac{B_1 B_2}{B_1 + B_2} \tag{2.10}$$

$$C = C_1 + C_2 + \frac{(D_1 - D_2)(A_2 - A_1)}{B_1 + B_2} \tag{2.11}$$

$$D = \frac{D_1 B_2 + D_2 B_1}{B_1 + B_2} \tag{2.12}$$

series − parallel connection

$$A = A_1 + A_2 + \frac{(B_1 - B_2)(C_2 - C_1)}{D_1 + D_2} \tag{2.13}$$

$$B = \frac{B_1 D_2 + B_2 D_1}{D_1 + D_2} \tag{2.14}$$

$$C = \frac{C_1 D_2 + C_2 D_1}{D_1 + D_2} \tag{2.15}$$

$$D = \frac{D_1 D_2}{D_1 + D_2} \tag{2.16}$$

parallel − series connection

$$A = \frac{A_1 A_2}{A_1 + A_2} \tag{2.17}$$

$$B = \frac{B_1 A_2 + B_2 A_1}{A_1 + A_2} \tag{2.18}$$

$$C = \frac{C_1 A_2 + C_2 A_1}{A_1 + A_2} \tag{2.19}$$

$$D = D_1 + D_2 + \frac{(C_1 - C_2)(B_2 - B_1)}{A_1 + A_2} \tag{2.20}$$

When identical or complementary two-ports are used it is possible to obtain a proper compensation. These compensation techniques are commonly known as balancing techniques.

If a second two-port is connected in cascade with another two-port, the transmission parameters of the cascade connection can be expressed as follows:

cascade connection

$$A = A_1 A_2 + B_1 C_2 \tag{2.21}$$

$$B = A_1 B_2 + B_1 D_2 \tag{2.22}$$

$$C = C_1 A_2 + D_1 C_2 \tag{2.23}$$

$$D = C_1 B_2 + D_1 D_2 \tag{2.24}$$

Now, in order to accomplish a proper compensation, the input-output relation of the second two-port should be the inverse function of the first one.

2.2.2 Error feedforward

Circuits that use the error-feedforward technique all have in common that they first obtain an error signal by subtracting an accurately known fraction of the output signal of a network (or a copy of the output signal) from the input signal (or a copy of the input signal), then pass this error signal through a network with characteristics similar to the first network, and finally add the output signals of both networks to obtain a corrected output signal. A block diagram of a system using the error-feedforward technique is shown in Figure 2.3.

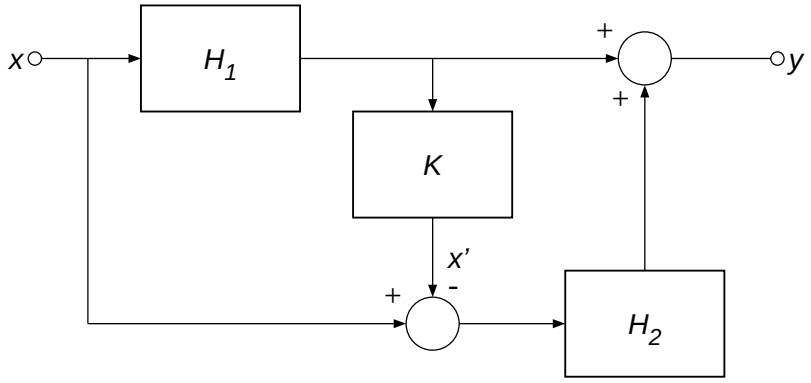

Figure 2.3: Block diagram of a system using the error-feedforward technique

Though this technique seems attractive, its use is restricted to some special cases only, because its implementation is not without some difficulties. We do not deal with circuits using error feedforward in this work.

2.2.3 Negative feedback

A system is a feedback system if some variable, either the output variable or an internal one, is used as an input to a part of the system in such a way that it is able to affect its own value. A block diagram of a system using the negative-feedback technique is shown in Figure 2.4.

In the case of negative feedback, when the transmission around the loop Hf has a negative sign, it is possible to nullify the error between the input signal x and a signal x' which is obtained by passing the output signal through a subsystem with well-known characteristics f. If Hf (which often is called the loop gain) approaches infinity, the output y is related to the input x as the inverse input-output relation of that subsystem.

When H and f are two-ports, there are four ways of applying (single-loop) feedback by means of two two-ports:

- series-series connection

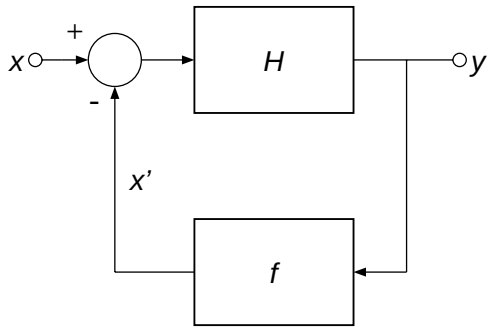

Figure 2.4: Block diagram of a system using the negative-feedback technique

- parallel-parallel connection
- series-parallel connection
- parallel-series connection

The transmission parameters of these four feedback configurations can be derived from (2.5) to (2.20), with one major difference: the input ports of the feedback network are connected to the *output* ports of the active two-port. Therefore, for the parameters of the second two-port we use those of the feedback network, of which the input and output ports have been exchanged [4]:

$$A_2 = \frac{D_f}{\Delta_f} \tag{2.25}$$

$$B_2 = -\frac{B_f}{\Delta_f} \tag{2.26}$$

$$C_2 = -\frac{C_f}{\Delta_f} \tag{2.27}$$

$$D_2 = \frac{A_f}{\Delta_f} \tag{2.28}$$

with $\Delta_f = A_f D_f - B_f C_f$ (the determinant of the transmission matrix of the feedback network).

Series-series connection

When used as a feedback configuration, this connection is designed to set the transconductance factor γ. See Figure 2.5. If the first (active) network H approaches a nullor, we find for the transmission parameters of the total network

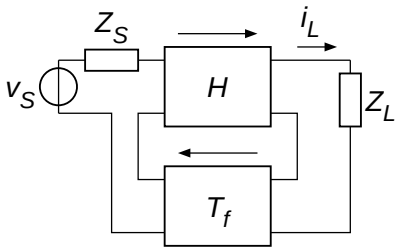

Figure 2.5: A transconductance amplifier with direct negative feedback

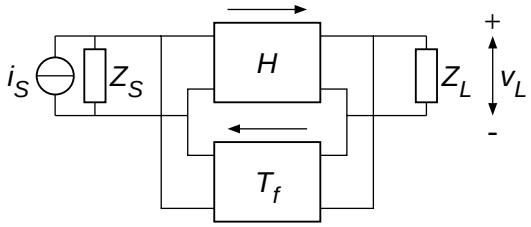

Figure 2.6: A transimpedance amplifier with direct negative feedback

$$A = 0 \tag{2.29}$$
$$B = -1/C_f \tag{2.30}$$
$$C = 0 \tag{2.31}$$
$$D = 0 \tag{2.32}$$

and for the transconductance factor

$$\gamma = i_L/v_S = -C_f \tag{2.33}$$

Parallel-parallel connection

This way of connecting an active two-port and a feedback network is designed to set the transimpedance factor ζ. See Figure 2.6. Under the same assumption that the first (active) network H approaches a nullor, we find for the transmission parameters of the total network

$$A = 0 \tag{2.34}$$
$$B = 0 \tag{2.35}$$
$$C = -1/B_f \tag{2.36}$$
$$D = 0 \tag{2.37}$$

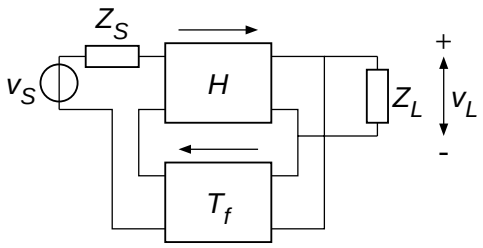

Figure 2.7: A voltage amplifier with direct negative feedback

and for the transimpedance factor

$$\zeta = v_L/i_S = -B_f \tag{2.38}$$

Series-parallel connection

In order to set the voltage gain μ of a circuit with negative feedback, a series-parallel connection is required. See Figure 2.7. When the first two-port H again approaches a nullor, we get for the transmission parameters of the total network

$$A = 1/D_f \tag{2.39}$$
$$B = 0 \tag{2.40}$$
$$C = 0 \tag{2.41}$$
$$D = 0 \tag{2.42}$$

and for the voltage gain

$$\mu = v_L/v_S = D_f \tag{2.43}$$

Parallel-series connection

By connecting the input of the active two-port in parallel with the output of the feedback network, and the output of the first in series with the input of the latter, we are able to set the current gain α. See Figure 2.8. With the active two-port H being a nullor we get

$$A = 0 \tag{2.44}$$
$$B = 0 \tag{2.45}$$
$$C = 0 \tag{2.46}$$
$$D = 1/A_f \tag{2.47}$$

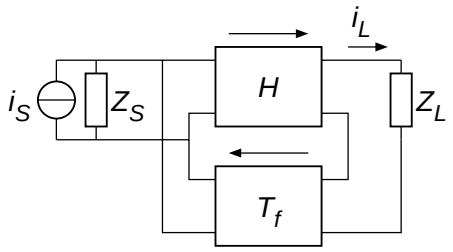

Figure 2.8: A current amplifier with direct negative feedback

and for the current gain

$$\alpha = i_L/i_S = A_f \tag{2.48}$$

2.2.4 Indirect negative feedback

In low-voltage circuits, due to the restricted voltage swing, it is often not possible to sense the output current of a circuit, and/or to compare an input voltage directly. Only the transimpedance amplifier does not have this problem. To realize voltage, current and transconductance amplifiers, a useful alternative then may be a technique called indirect negative feedback. In an indirect-negative-feedback circuit the output and/or the input stage is copied, so that it has an equivalent input-output relation, and the feedback signal is taken from and/or fed back to that copy. Thus, it is possible to obtain a response of the circuit which is determined by the feedback network only, assuming that the copying does not introduce errors.

Setting the voltage gain by means of indirect feedback

A voltage amplifier with negative feedback and indirect voltage comparison is depicted in Figure 2.9.

T_1 is the first input stage which serves as the input for the input signal. T_2 is the second input stage, which is used to compare the voltage of the feedback network indirectly. T_f is the feedback network and T_r is the remainder of the active circuitry. All networks are two-ports. When T_r approaches a nullor we obtain for the transmission parameters of the total circuit

$$A = -\frac{B_1}{A_f B_2 + B_f D_2} \tag{2.49}$$

$$B = 0 \tag{2.50}$$

$$C = -\frac{D_1}{A_f B_2 + B_f D_2} \tag{2.51}$$

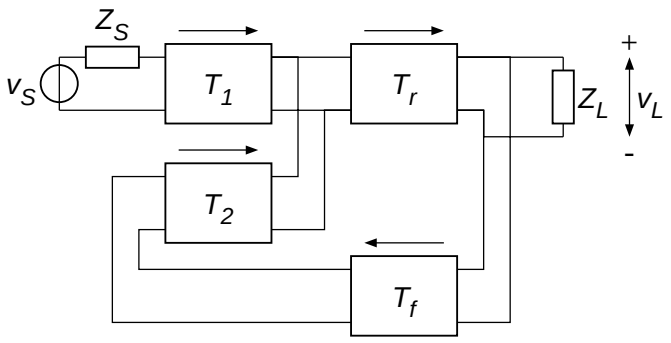

Figure 2.9: A voltage amplifier with negative feedback and indirect voltage comparison

$$D = 0 \tag{2.52}$$

For the voltage gain of the total circuit we can write [2]

$$v_L/v_S = \frac{1}{A + B/Z_L + CZ_S + DZ_S/Z_L} = -\frac{A_f B_2 + B_f D_2}{B_1 + D_1 Z_S} \tag{2.53}$$

We see that various other parameters have entered the expression of the voltage gain compared with the expression derived earlier for the 'direct-feedback' voltage gain. When, for example, T_1 and T_2 are identical (e.g. two well-matched transistors in the same operating point), the influence of Z_S can be counteracted by making Z_S equal to B_f/A_f, which is, in fact, the output impedance of the feedback network. This results in

$$v_L/v_S = -A_f \tag{2.54}$$

Setting the current gain by means of indirect feedback

A current amplifier with negative feedback and indirect current sensing is depicted in Figure 2.10.

T_1 is the first output stage which serves as the output of the total circuit. T_2 is the second output stage, which is used to sense the output current indirectly. T_f again is the feedback network and T_r is the remainder of the active circuitry. When T_r approaches a nullor, we get for the transmission parameters of the total circuit

$$A = 0 \tag{2.55}$$

$$B = 0 \tag{2.56}$$

$$C = -\frac{A_1}{A_2 B_f + B_2 D_f} \tag{2.57}$$

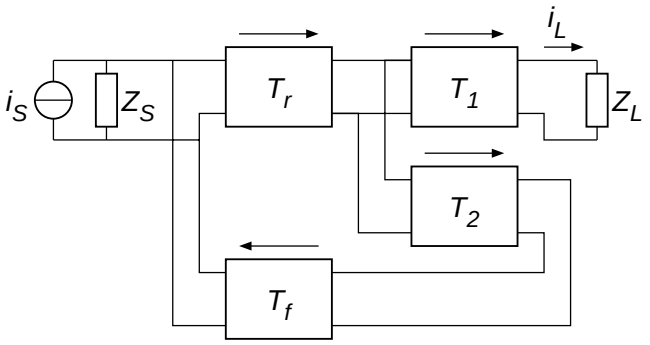

Figure 2.10: A current amplifier with negative feedback and indirect current sensing

$$D = -\frac{B_1}{A_2 B_f + B_2 D_f} \tag{2.58}$$

For the current gain of the total circuit we can write [2]

$$i_L/i_S = \frac{1}{AZ_L/Z_S + B/Z_S + CZ_L + D} = -\frac{A_2 B_f + B_2 D_f}{A_1 Z_L + B_1} \tag{2.59}$$

Once again various additional parameters have entered the expression of the current gain compared with the expression derived earlier for the 'direct-feedback' current gain. When for example T_1 and T_2 are identical, the influence of Z_L can be counteracted by making Z_L equal to B_f/D_f, which is, in fact, the input impedance of the feedback network. Hence

$$i_L/i_S = -D_f \tag{2.60}$$

Setting the transconductance factor by means of indirect feedback

It is also possible to realize a voltage-current transfer by means of indirect feedback. This can be done in three different ways:

- sensing the output current indirectly and comparing the input voltage directly
- sensing the output current directly and comparing the input voltage indirectly
- sensing the output current and comparing the input voltage, both indirectly

These three possibilities are shown in Figures 2.11, 2.12 and 2.13, respectively. When T_r again approaches a nullor we get for the transmission parameters of

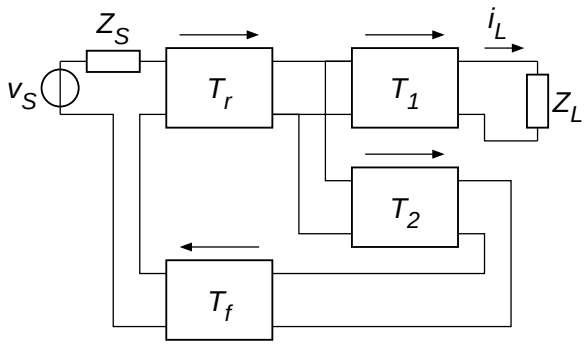

Figure 2.11: A transconductance amplifier with negative feedback and *indirect* current sensing and *direct* voltage comparison

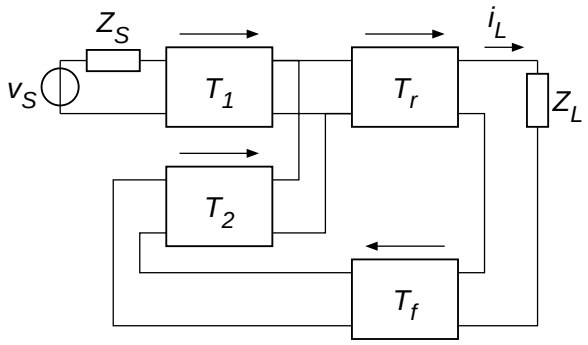

Figure 2.12: A transconductance amplifier with negative feedback and *direct* current sensing and *indirect* voltage comparison

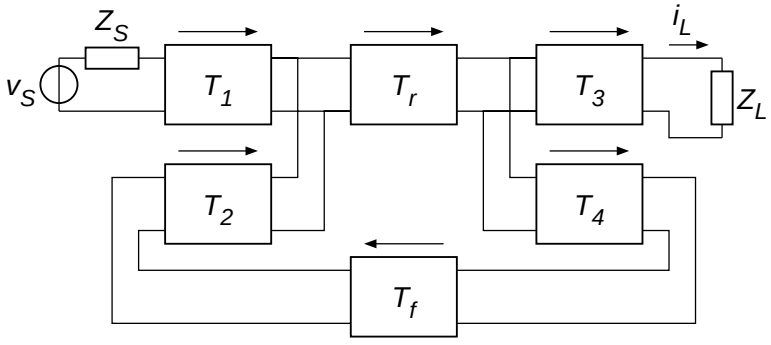

Figure 2.13: A transconductance amplifier with negative feedback and *indirect* current sensing and *indirect* voltage comparison

the transconductance amplifier with *indirect* current sensing and *direct* voltage comparison

$$A = -\frac{A_1}{A_2 A_f + B_2 C_f} \tag{2.61}$$

$$B = -\frac{B_1}{A_2 A_f + B_2 C_f} \tag{2.62}$$

$$C = 0 \tag{2.63}$$

$$D = 0 \tag{2.64}$$

And for the transconductance of the total circuit we can write [2]

$$i_L/v_S = \frac{1}{AZ_L + B + CZ_S Z_L + DZ_S} = -\frac{A_2 A_f + B_2 C_f}{A_1 Z_L + B_1} \tag{2.65}$$

When for example T_1 and T_2 are identical, the influence of Z_L can be counteracted by making Z_L equal to A_f/C_f, which is, in fact, the input impedance of the feedback network. Hence

$$i_L/v_S = -C_f \tag{2.66}$$

When T_r again approaches a nullor, we get for the transmission parameters of the transconductance amplifier with *direct* current sensing and *indirect* voltage comparison

$$A = 0 \tag{2.67}$$

$$B = -\frac{B_1}{C_f B_2 + D_f D_2} \tag{2.68}$$

$$C = 0 \tag{2.69}$$

$$D = -\frac{D_1}{C_f B_2 + D_f D_2} \tag{2.70}$$

And for the transconductance of the total circuit we can write

$$i_L/v_S = -\frac{C_f B_2 + D_f D_2}{B_1 + D_1 Z_S} \tag{2.71}$$

When, for example, T_1 and T_2 are identical, the influence of Z_S can be counteracted by making Z_S equal to D_f/C_f, which is, in fact, the output impedance of the feedback network. Hence

$$i_L/v_S = -C_f \tag{2.72}$$

Following the same procedure as above in order to find the transmission parameters of the circuit of Figure 2.13, we see that none of these parameters is zero, which means that both the source impedance and the load impedance enters into the expression for the transconductance factor. For this reason we do not deal with this circuit any further.

2.3 Operating in the current domain

Generally, it is not possible to choose the input and output quantities of a circuit freely. Their choice depends on:

- the transducers at the input and/or output
- the desired topology
- the available technology
- the available power supply

2.3.1 Source and load

When the input signal for a circuit comes from a transducer, the input quantity has to be chosen to have the best reproducing relation to the physical input quantity of the transducer. When the output signal of a circuit has to drive a transducer, the output quantity has to be chosen to have the best reproducing relation to the physical output quantity of the transducer [2].

2.3.2 The desired topology

Inside the circuit, when signals coming from several subcircuits with a common terminal have to be added, current is a better choice for the information-carrying quantity than voltage. Currents can be added by simply connecting the output terminals of the subcircuits in parallel. When a signal has to be distributed to several subcircuits, voltage is a better choice for the information-carrying quantity than current. Voltages can be distributed by simply connecting the input terminals of the subcircuits in parallel.

2.3.3 The available technology

When there is no adding or distributing inside a circuit, a preference for either voltage or current may depend on the available technology. Let us therefore consider the influence of parasitic immitances. The influence of parasitic *admittances* in

parallel with the signal path can be reduced by terminating the signal path with a *low* impedance. The parasitic admittances then have no voltages across their terminals and thus no current flows in them. The influence of parasitic *impedances* in series with the signal path can be reduced by terminating the signal path with a *high* impedance. Then no current flows in the parasitic impedances and thus there is no voltage across their terminals.

In low-power integrated circuits, often the parasitic admittances, i.e., the node capacitances, have more influence on the signal behavior than the parasitic impedances, i.e., the branch inductances and resistances. Therefore it is convenient to terminate the signal paths with low impedances as much as possible. In this situation it is best to choose current as the information-carrying quantity. Circuits that have a current as the information-carrying quantity are from now on denoted as 'operating in the current domain'.

In literature, this technique is often recommended to improve the high-frequency performance of a system, resulting in socalled 'current-mode' circuits [5, 6]. However, it must be noted that the expression 'current mode' has no rigorous meaning: the behavior of electrical networks is always the product of an interplay between voltages and currents.

2.3.4 The available power supply

When we apply feedback to a circuit, the preference for either voltage or current may depend on the available power supply. Let us therefore consider the case of series feedback at the input or output. Generally, the active network must have floating input or output ports. If the input voltages with respect to a common reference are not zero, or the output currents are not equal, this may result in offset, inaccuracy or distortion.

In order to overcome these imperfections, it may be attractive to use

- compensation (by an anti-series connection of identical stages), or
- indirect feedback

A major disadvantage of the use of stages connected in anti-series at the input (voltage comparison) is that the power density spectrum of the equivalent noise voltage is doubled. The anti-series connection of stages at the output results in a deterioration of the power efficiency.

The second possibility uses indirect feedback. Applied at the input (indirect voltage comparison) this again produces a doubled noise spectrum, while when applied at the output (indirect current sensing) only the power efficiency may deteriorate slightly. Another major disadvantage of indirect voltage comparison is that it requires two input stages with *symmetrical* or *opposite non-linearities*,

in order to compensate for the non-linearities. In practice, this requires either two balanced input stages or two complementary stages in a complementary IC process. The use of two balanced input stages again doubles the power density spectrum of the equivalent noise voltage. A complementary IC process is often not available and, moreover, exact complementarity can never be accomplished. Indirect feedback at the output, however, calls for two *identical* output stages, to compensate for the non-linearities. These can easily be made in any ordinary IC process. For this reason it is preferable that low-voltage analog integrated circuits operate in the current domain, i.e., have a current as the information-carrying quantity, as much as possible.

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Chapter 3

Modeling the bipolar transistor at low voltages and low currents

No minority has a right to block a majority
from conducting the legal business of the organization.

No majority has a right to prevent a minority
from peacefully attempting to become a majority.

Robert M. Pirsig: Lila

3.1 Introduction

In this chapter we look for mathematical models that describe the terminal behavior of bipolar transistors in low-voltage low-power circuits. These models can vary from coarse to refined, depending on the purpose for which they are needed. For example, when formulating an initial concept, a designer uses only those models that describe the major function of the components. It is only at a later stage that models are used that describe the components in more detail.

For an active component, usually two kinds of models are given:

- a large-signal, and
- a small-signal model

The choice depends on whether or not the signal quantities can be considered small with respect to the bias quantities. When the signal excursions are small, the nonlinear characteristics of the active devices can be regarded as being linear around a certain operating point, which facilitates the calculation of the input-output relation.

When designing a circuit in respect to its noise behavior a different model is important for the designer. We deal with this noise model in Section 3.4.

3.2 Large-signal model of a bipolar transistor

Our starting point is the well-known Ebers-Moll model [1], partly because we in this work do not deal with the physical processes, partly because this model has proved to give a sufficiently accurate description of the transistor behavior under 'normal' circumstances. The Ebers-Moll model for an NPN transistor is depicted in Figure 3.1.

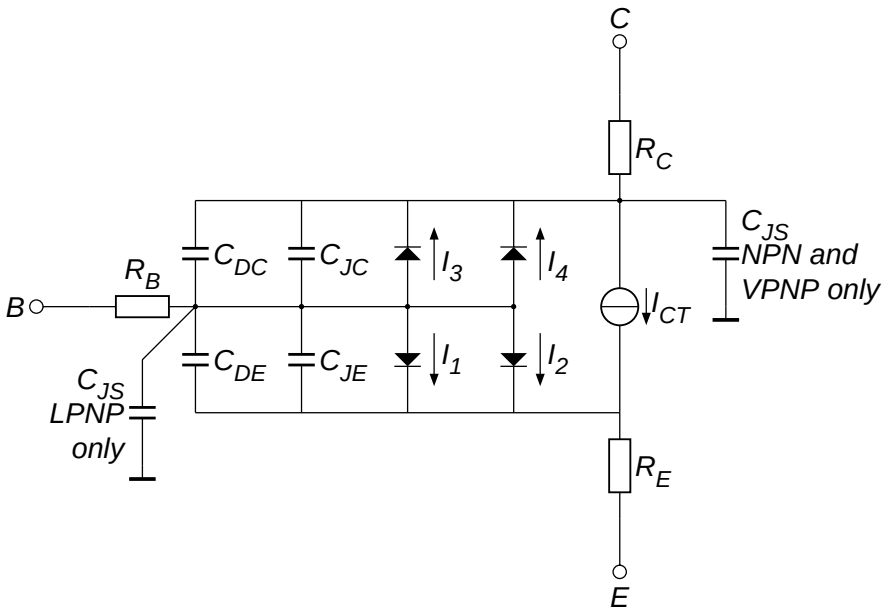

Figure 3.1: Ebers-Moll model for an NPN transistor

3.2.1 The transport current I_{CT}

The model consists of a non-linear voltage-controlled current source I_{CT} between the intrinsic collector and emitter, controlled by the intrinsic base-emitter voltage V_{BE} and the intrinsic base-collector voltage V_{BC}:

$$I_{CT} = I_{CC} - I_{EC} \tag{3.1}$$

$$I_{CC} = I_S(e^{V_{BE}/V_T} - 1) \tag{3.2}$$

$$I_{EC} = I_S(e^{V_{BC}/V_T} - 1) \tag{3.3}$$

with I_S the saturation current and V_T the thermal voltage kT/q, approximately 26 mV at 300 K.

Four leakage diodes model the base current I_B:

$$I_B = I_1 + I_2 + I_3 + I_4 \tag{3.4}$$

$$I_1 = I_{CC}/B_F \tag{3.5}$$
$$I_2 = I_{SE}(e^{V_{BE}/\eta_E V_T} - 1) \tag{3.6}$$
$$I_3 = I_{EC}/B_R \tag{3.7}$$
$$I_4 = I_{SC}(e^{V_{BC}/\eta_C V_T} - 1) \tag{3.8}$$

η_E, η_C, B_F and B_R being process parameters.

I_1 models the normal leakage base current caused by injection from the base into the emitter, while I_3 models the normal leakage base current produced by injection from the base into the collector. At low currents, however, three other contributions to I_B play an important role:

- recombination of carriers at the surface
- the formation of emitter-base surface channels
- recombination in the emitter-base depletion layer

We do not here discuss the physics of these extra base currents, but simply state that they also have an exponential dependence on V_{BE}, but that the exponential differs by a factor η_E or η_C, which can have values between one and four. These additional base currents can be included in the model by two non-ideal diodes. I_2 models the non-ideal base current from base to emitter, and I_4 models the non-ideal base current from base to collector.

At high currents, high-level injection occurs and the factor B_F decreases with increasing I_{CT}. We do not deal with this effect in this work, because we are interested in low-current behavior only.

At high voltages, there are other effects that limit the operating area of a transistor. These effects are:

- base-emitter Zener breakdown
- collector multiplication
- emitter crowding

We do not here discuss these effects, because they do not occur in low-voltage low-power applications.

The transport current also depends on the voltages across the emitter-base junction V_{EB} and the collector-base junction V_{CB}. This effect is called 'basewidth modulation' or 'Early effect', and can be modeled by making the saturation current I_S dependent on V_{EB} and V_{CB}. In approximation:

$$I_S = I_{SO}(1 + V_{EB}/V_{AR} + V_{CB}/V_{AF}) \tag{3.9}$$

in which I_{SO}, V_{AR} and V_{AF} depend on the process and the temperature only.

3.2.2 The resistances R_B, R_C and R_E

Between the intrinsic transistor and the external connections, there are three resistances:

- *the base resistance R_B:* This (parasitic) resistance can have a great effect on the small-signal and transient responses. It is a distributed element and therefore strongly depends on the operating point. A typical value for an integrated small geometry transistor is 1000 Ω.
- *the collector (bulk) resistance R_C:* This resistance depends on the collector current and voltage, and decreases the slope of the curves in the saturated region of the transistor. A typical value is 100 Ω.
- *the emitter (bulk) resistance R_E:* Because of the high doping level of the emitter, this resistance consists mainly of the contact resistance, which is small (a typical value is 1 Ω). The emitter bulk resistance mainly affects the V_{BE}-I_C relation at higher operating currents.

For these three resistances, it is valid that they do not have any influence on the transistor behavior when the currents used are small (e.g. 1 μA) and the frequency range of interest is less than the transit frequency f_T.

3.2.3 The junction capacitances C_{JE} and C_{JC}

The capacitances C_{JE} and C_{JC} model the incremental fixed charges stored in the transistor's depletion layers for incremental changes in the junction voltages. Each capacitance is a non-linear function of the voltage across the junction:

$$C_{JE} = \frac{C_{JEO}}{(1 + V_{EB}/V_{JE})^{M_E}} \text{ and} \tag{3.10}$$

$$C_{JC} = \frac{C_{JCO}}{(1 + V_{CB}/V_{JC})^{M_C}} \tag{3.11}$$

in which C_{JEO} is the small-signal depletion capacitance at zero base-emitter (bias) voltage and C_{JCO} the equivalent capacitance at zero base-collector (bias) voltage. V_{JE} and V_{JC} are the built-in voltages of the base-emitter and base-collector junction and M_E and M_C are their grading coefficients, which usually lie between 0.3 and 0.5.

In integrated circuits, there is also another junction capacitance present: a substrate capacitance, C_{JS}, which for (vertical) NPN and PNP transistors is connected between the intrinsic collector and substrate. For lateral IC transistor structures, this capacitance is connected between the intrinsic base and the substrate.

$$C_{JS} = \frac{C_{JSO}}{(1 + V_{SJ}/V_{JS})^{M_J}} \tag{3.12}$$

where C_{JSO} is the small-signal depletion capacitance at zero bias voltage, V_{SJ} the voltage across the junction and V_{JS} is the built-in voltage of the junction. M_J again is a grading coefficient.

3.2.4 The diffusion capacitances C_{DE} and C_{DC}

The diffusion capacitances model the charges Q_{DE} and Q_{DC} which are associated with the transport currents I_{EC} and I_{CC} respectively.

$$Q_{DE} = \tau_F I_{CC} \tag{3.13}$$
$$Q_{DC} = \tau_R I_{EC} \tag{3.14}$$

These relations indicate that the diffusion capacitances are proportional to the current. In practice, the diffusion capacitances are only dominant when the currents exceed hundreds of micro-amps. Therefore they can be neglected in low-power circuits.

3.2.5 Low-voltage low-power large-signal transistor model

Having now dealt with all the elements of the Ebers-Moll transistor model, we are able to state a simplified model which is valid for low-voltage low-power circuits with a frequency range of interest which does not exceed the transit frequency f_T. This model is depicted in Figure 3.2.

3.3 Small-signal model of a bipolar transistor

At this stage, it is possible to extract a linearized (small-signal) model from the large-signal model shown in Figure 3.2, which is valid when the transistor is biased

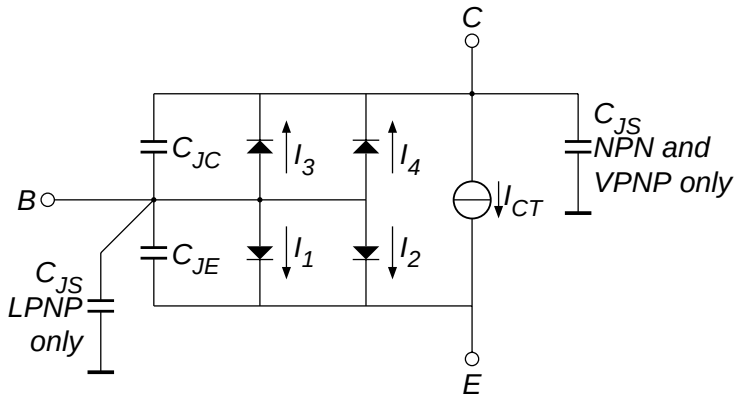

Figure 3.2: Simplified Ebers-Moll transistor model valid for low-voltage low-power applications

in its forward active region. When the signal quantities are small compared to the bias quantities, we are able to describe the signal behavior of any non-linear network as a linear network. The circuit shown in Figure 3.2 then linearizes to the circuit shown in Figure 3.3, with

$$
\begin{aligned}
g_m &= dI_C/dV_{BE} \approx I_C/V_T \text{ , the transconductance} \\
I_C &= \text{the collector current in a certain operating point} \\
\beta_F &= dI_C/dI_B \text{ , the current gain} \\
I_B &= \text{the base current in a certain operating point} \\
r_\pi &= \beta_F/g_m \\
r_o &= dV_{CE}/dI_C \text{ , which accounts for the Early effect}
\end{aligned}
$$

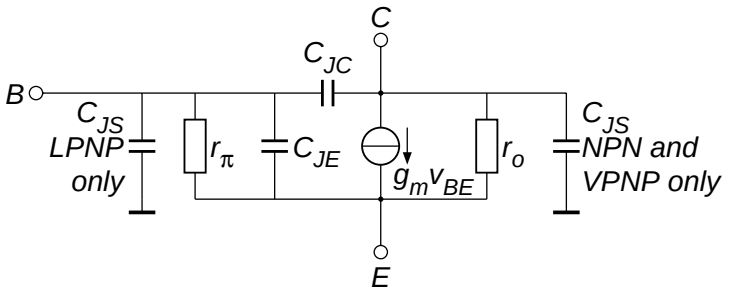

Figure 3.3: Small-signal transistor model derived from the simplified Ebers-Moll model

3.4 Noise

3.4.1 Noise sources in the bipolar transistor

In a bipolar transistor biased in its forward active region, we are able to indicate three noise sources among the three terminals whose power density spectra are proportional to the currents flowing from one terminal to another. These sources produce shot noise, and are uncorrelated:

- the shot noise of the intrinsic collector-emitter current, between collector and emitter, has a power density spectrum $S(i_C) = 2qI_{CT} \approx 2qI_C$.
- the shot noise of the intrinsic base-emitter current, between base and emitter, has a power density spectrum $S(i_B) = 2qI_F \approx 2qI_B$.
- the shot noise of the intrinsic base-collector current, between base and collector, has a power density spectrum $S(i_{CO}) = 2qI_R \approx 0$.

Further, the base resistance R_B produces thermal noise, of which the power density spectrum (in V^2/Hz) equals $4kTR_B$.

Finally, we are able to indicate a low-frequency (1/f) noise current source connected between the intrinsic base and emitter, which is the product of a process-dependent noise mechanism. It has been found (experimentally) that the spectrum of this noise current generator equals

$$S(i_{Bf}) = KI_B^a/f \tag{3.15}$$

(with a between 1 and 2) over a wide and useful range of collector bias currents [2, 3, 4]. K is a process-dependent constant. Alternatively, it is possible to write [4, 5]:

$$S(i_{Bf}) = 2qI_B f_l/f \tag{3.16}$$

in which f_l is a representation of the noise corner frequency and is proportional to I_B^{a-1}. Because a lies between 1 and 2, the noise corner frequency decreases when the base current decreases. We therefore suppose that low-frequency noise makes only an insignificant contribution to the total noise in most low-power circuits.

3.4.2 Transformation of noise sources to the input

When the signal quantities are kept small with respect to the bias quantities, the noise sources can be considered stationary and therefore the noise is additive to the signal. We are now able to replace the noisy transistor with a noise-free transistor together with two external noise sources at the input [6], which usually

are correlated. In a bipolar transistor, only the collector shot noise source i_C needs to be transformed. This transformation results in two correlated noise sources Bi_C and Di_C (B and D are the transistor transmission parameters), Figure 3.4.

Note: the noise sources in this figure are represented by their Fourier transforms in order to account for correlations because of the transformations.

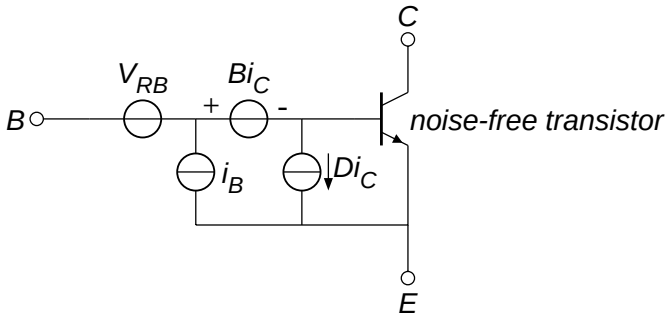

Figure 3.4: Noisy transistor replaced with a noise-free transistor and four noise sources

When we consider that for a bipolar transistor

$$B = 1/\gamma = -1/g_m \tag{3.17}$$
$$D = 1/\alpha = -(1/\beta_F + jf/f_T)\ [5] \tag{3.18}$$
$$I_C = g_m V_T \tag{3.19}$$
$$B_F \approx \beta_F \tag{3.20}$$

we find that the influence of R_B is negligible, if

$$R_B < \frac{1}{2g_m} \tag{3.21}$$

In practice, this is true when the collector current does not exceed several tens of microamps, so it can be stated that in most low-power circuits the noise caused by R_B is negligible.

Finally the influence of Di_c is negligible, if

$$f < \frac{f_T}{\sqrt{B_F}} \tag{3.22}$$

Now we are able to state a simple noise model of a bipolar transistor, valid for low-voltage low-power circuits and a frequency range of interest lower than $f_T/\sqrt{B_F}$. This model is depicted in Figure 3.5.

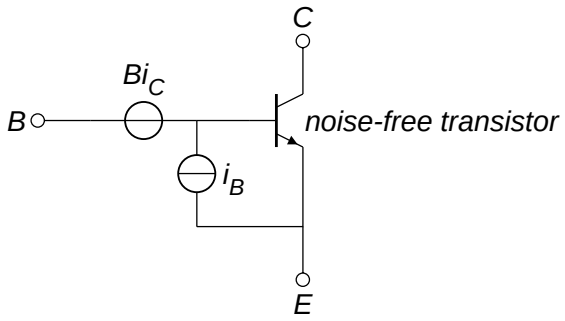

Figure 3.5: Simplified noise model valid for low-voltage low-power applications

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Chapter 4

Negative-Feedback Amplifiers

This example serves to illustrate how feedback
– plugging the system's output back into the system as input –
ushers you to the fixed points.
Why should this be so?
Why could the system not trash about randomly,
somehow avoiding all fixed points?

Douglas R. Hofstadter: Metamagical themas

4.1 Introduction (outline of the design method)

In almost any electronic system some kind of signal amplification can be identified. Amplification is obviously an indispensable function [1]. The aim of an amplifier is to bring the information of the source signal to a higher energy level. This information must be transferred as accurately as possible, e.g., with minimal distortion, maximum speed and with minimal addition of interfering signals and noise. In Chapter 2 we saw that these requirements can be met by applying negative feedback.

Negative feedback is a principle that can be seen in many technical, biological and social processes. It implies that a driving quantity, based on the result of the driven quantity, is corrected in such a way that the desired result is obtained [2]. Negative feedback allows us to exchange the large gain provided by the (highly non-linear) active devices for quality.

According to the *asymptotic-gain model* [3] the transfer function A_f of almost any negative-feedback amplifier can be described in terms of an ideal amplification factor $A_{f\infty}$ (the asymptotic gain), i.e., the transfer if the amplifying block has nullor properties, and an error factor comprising the loop gain $A\beta$, or

$$A_f = A_{f\infty}\frac{-A\beta}{1-A\beta} \tag{4.1}$$

The error factor $-A\beta/(1-A\beta)$ describes the influence of the non-ideal nature of the amplifier. Ideally, this factor should assume unity value as closely as possible.

For the designer, this means that the design of A_f can be done in two successive and independent design steps. The first step is the determination of $A_{f\infty}$, which can be considered as the design aim, and the second step is the realization of an adequate loop transfer function $A\beta$.

For each design step, various quality aspects must be considered:

- **noise.** Being a random signal, noise already present in the incoming signal cannot be reduced by using negative feedback. However, the addition of extra noise can be kept to a minimum. Therefore, both the noise contribution of the feedback network and of the active part of the amplifier have to be considered.

- **distortion.** The parameter values of active devices always vary with signal quantities and, therefore, the input-output relation of an amplifier is nonlinear and distorted. The best method to reduce these imperfections is to make the transfer independent of the parameters of the active devices as much as possible by applying negative feedback with a linear feedback network. At large values of the loop gain $A\beta$, $A_f \approx A_{f\infty}$ and the transfer will be almost independent of the characteristics of the active devices.

- **accuracy.** The accuracy of an amplifier depends on the spread in device parameters caused by fabrication tolerances and aging. Similar to distortion, the inaccuracy is reduced in a negative-feedback amplifier when the feedback network is accurate and the loop gain is high.

- **bandwidth.** In low-power integrated circuits, the bandwidth is limited because of the existence of parasitic capacitances. In Chapter 2 we found that their influence can be minimized by operating in the current domain as much as possible. Expression (4.1) demonstrates an additional possibility: in negative-feedback amplifiers the bandwidth can be enlarged by choosing a larger loop gain.

- **output capability.** In low-voltage low-power integrated circuits both the voltage and current swing are limited. Special attention therefore has to be paid to their maximum values. Often these appear at the output of an amplifier.

- **power efficiency.** Obviously, power efficiency is of major interest in low-power integrated circuits.

- **integratability.** Since we are dealing with integrated circuits, we have to make sure that all the required components are integratable. This means that we cannot make use of transformers or inductors and that the sum of the capacitor values and the sum of the resistor values are limited.

An ideal design strategy would be one in which all quality aspects can be treated independently of each other (also called orthogonal). Unfortunately, this is only seldom possible. An example: suppose we want to obtain an output current of 100 nA (peak value). In view of the power efficiency, the bias current of the (class-A) output stage is best chosen to be exactly 100 nA. Unfortunately, this conflicts with the designability of the amplifier with respect to its high-frequency behavior; the poles of the output stage would sweep over a wide range, eventually leading to instability of the total amplifier. However, following a hierarchic design strategy (see for example [3]) keeps the interaction between the various quality aspects small.

This hierarchic design strategy comes down to the following steps:

- **choose a proper basic amplifier configuration.** This choice is based on the kind of electrical quantity we have at both input and output.
- **choose the character and numerical values of the (passive) feedback network.** This choice is based on noise, accuracy, output capability and integratability.
- **choose a proper input stage.** This choice is based on noise. In low-power circuits also the power efficiency is important.
- **choose a proper output stage.** This choice is based on the output capability and power efficiency.
- **evaluate the loop gain.** The other quality aspects, viz, distortion, accuracy and bandwidth are mainly determined by the loop gain as a function of frequency. These aspects determine whether an amplifier should have one stage (if the input stage can be the output stage as well), two stages (an input and an output stage) or more stages (the intermediate stages then have to be chosen on the grounds of these quality aspects **and** power efficiency).
- **realize the desired high-frequency behavior.** Especially oscillation has to be avoided under all circumstances.
- **choose a proper bias circuit.** Because the design of the signal path is completed in the foregoing stages, this bias circuit is not permitted to have a major influence on the signal transfer.

These steps are the subjects of the following sections.

4.2 The basic amplifier configuration and the feedback network

From the large class of negative-feedback amplifiers (using either direct, indirect or active feedback [3]) we restrict ourselves to those that sense the output current indirectly. It was shown in Chapter 2 that this leads to configurations that are especially suitable for low-voltage integrated circuits. Although multi-loop configurations may be important in characteristic impedance systems, where the interconnections are made by transmission lines, we deal only with single-loop configurations in this chapter. An extensive description of multi-loop negative-feedback amplifiers can be found in [3] and [4]. A practical example of a two-loop negative-feedback amplifier with indirect current sensing is discussed in Chapter 7.

4.2.1 Current amplifiers

In Chapter 2, it was found that low-voltage low-power electronic circuits should preferably operate in the current domain insofar as possible. As they have a current at both input and output, current amplifiers thus are the natural amplifiers to use in such an environment.

Basic amplifier configuration

The basic configuration of a current amplifier with an indirect output is depicted in Figure 4.1. In this circuit, the output current is sensed indirectly by means of Q_1 and partially (by means of the impedances Z_1 and Z_2) fed back to the input. Q_2 provides the output current. When all the transfer parameters of the op amp are infinite, $\mu \gg g_m Z_2$ and $\mu \gg g_m Z_L$ we can write for the ideal transfer $A_{f\infty}$ of this *two-impedance current amplifier*:

$$A_{f\infty} = -\frac{Z_1 + Z_2}{Z_2} \tag{4.2}$$

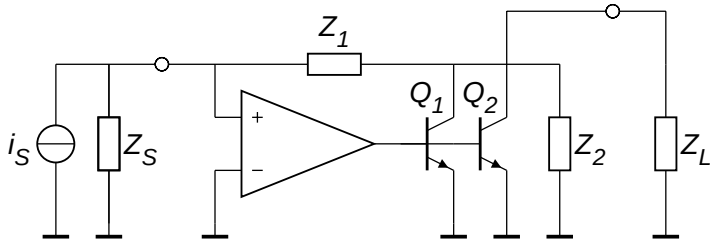

Figure 4.1: A current amplifier with an indirect output

Alternatively it is possible to choose Z_1 and Z_2 to be equal to zero and infinite, respectively, and vary the current gain by means of varying the scaling factor n of transistor Q_2. This amplifier, which from now on is called a *scaling current amplifier* is shown in Figure 4.2. With $\mu_{Q_2} \gg g_{m,Q_2} Z_L$ we are able to write for $A_{f\infty}$:

$$A_{f\infty} = -n = -\frac{g_{m,Q_2}}{g_{m,Q_1}} \tag{4.3}$$

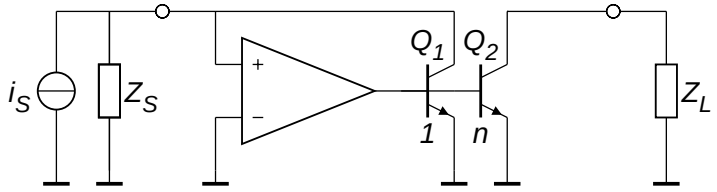

Figure 4.2: A scaling current amplifier

A well-known scaling current amplifier is obtained when the op amp is replaced by a short circuit: a *current mirror* [5]. Its circuit diagram is depicted in Figure 4.3. We deal with this amplifier in a later section.

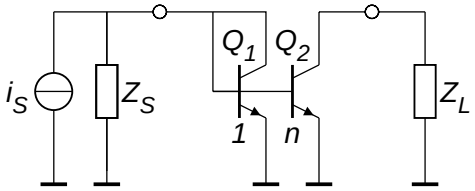

Figure 4.3: A current mirror

A special case: the two-resistance amplifier

When the impedances of the two-impedance amplifier (Figure 4.1) are real, i.e. resistances, we obtain an amplifier type that we can call a *two-resistance amplifier*. A problem arises when we have to decide whether to choose this amplifier or to choose a scaling current amplifier to obtain a real transfer function. We therefore take a look at the noise production of both amplifiers.

The feedback network

Even if the op amps are noise free, both amplifier types add some noise to the signal. This noise contribution originates from the two resistances R_1 and R_2 together with the noise from transistors Q_1 and Q_2. These noise sources can be

shifted towards the input and summed in a noise current source $S(i_{n,\mathrm{eq}})$ in parallel with the signal source. We obtain:

$$S(i_{n,\mathrm{eq}}) = \left(\frac{R_1}{R_1+R_2}\right)^2 S(i_{n,R_1}) + \left(\frac{R_2}{R_1+R_2}\right)^2 \left(S(i_{n,R_2}) + S(i_{n,Q_1}) + S(i_{n,Q_2})\right) \tag{4.4}$$

With $S(i_{n,R_1}) = 4kT/R_1$, $S(i_{n,R_2}) = 4kT/R_2$, $S(i_{n,Q_1}) = 2qI_{C,Q_1}$, $S(i_{n,Q_2}) = 2qI_{C,Q_2}$ and $I_{C,Q_1} = I_{C,Q_2} = I_C$ this can be rewritten as

$$S(i_{n,\mathrm{eq}}) = \left(\frac{R_1}{R_1+R_2}\right)^2 \frac{4kT}{R_1} + \left(\frac{R_2}{R_1+R_2}\right)^2 \left(\frac{4kT}{R_2} + 4qI_C\right) \tag{4.5}$$

Note that only the collector shot noise of Q_1 and Q_2 is of importance. The base shot noise is short-circuited by the op amp and does not make any contribution to the output signal of the amplifier. If for I_C the minimal value (efficiency !) which equals $(R_1+R_2)/R_2$ times the peak value $i_{S,p}$ of the signal current of the source is chosen, this results in

$$S(i_{n,\mathrm{eq}}) = \left(\frac{R_1}{R_1+R_2}\right)^2 \frac{4kT}{R_1} + \left(\frac{R_2}{R_1+R_2}\right)^2 \frac{4kT}{R_2} + \frac{R_2}{R_1+R_2} 4qi_{S,p} \tag{4.6}$$

For the scaling current amplifier, the input noise spectrum equals

$$S(i_{n,\mathrm{eq}}) = 2qI_{C,Q_1}\frac{n+1}{n} = 2qi_{S,p}\frac{n+1}{n} \tag{4.7}$$

We are now able to compare both noise spectra. Substituting $-(R_1+R_2)/R_2$, the gain of the two-resistance current amplifier, for $-n$, the gain of the scaling current amplifier, (4.7) results in

$$S(i_{n,\mathrm{eq}}) = 2qi_{S,p}\frac{R_1+2R_2}{R_1+R_2} \tag{4.8}$$

Comparing (4.6) and (4.8) it follows that we do best to choose for a two-impedance amplifier only if R_1 can be chosen larger than $2V_T/i_{S,p}$ ($V_T = kT/q$). In low-power design this is only seldom possible. For example, if the signal current at the input equals 25 nA (peak value) — this is a quite practical value in, e.g., filter circuits (see Chapter 6) — R_1 must be larger than 2 MΩ. Even in full-custom IC design, because of the restricted chip area, this value is not easily realized. Other advantages of using scaling amplifiers are that they have a better efficiency and their current gain is not limited by the maximum voltage swing over R_1.

4.2.2 Transconductance amplifiers

Another class of indirect-negative-feedback amplifiers that is useful in low-voltage low-power electronic circuits is the class of transconductance amplifiers. In Chapter 6, it is shown that these are the natural building blocks when it comes to designing low-voltage low-power controllable filters. For this reason we discuss them here.

Basic amplifier configuration

The basic configuration of a transconductance amplifier with an indirect output is depicted in Figure 4.4. In this circuit, the output current is sensed indirectly by means of Q_1, transformed into a voltage (by means of impedance Z) and fed back to the input. When all the transfer parameters of the op amp are infinite, $\mu_{Q_1} \gg g_{m,Q_1} Z$ and $\mu_{Q_2} \gg g_{m,Q_2} Z_L$ we can write for the ideal transfer $A_{f\infty}$:

$$A_{f\infty} = \frac{g_{m,Q_2}}{g_{m,Q_1}} \frac{1}{Z} \tag{4.9}$$

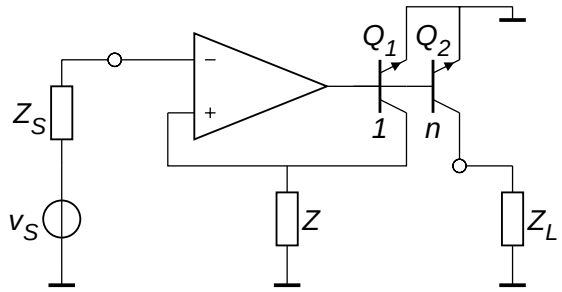

Figure 4.4: A transconductance amplifier with an indirect output

From this expression it can be seen that the transconductance can be varied by varying Z or the scaling factor n, which equals $g_{m,Q_2}/g_{m,Q_1}$.

The feedback network

Even if the op amp is noise free the amplifier adds some noise to the signal. This noise contribution originates from the impedance Z and transistors Q_1 and Q_2. These noise sources can be shifted toward the input and summed in a noise voltage source $S(v_{n,\text{eq}})$ in series with the signal source. We obtain:

$$S(v_{n,\text{eq}}) = S(v_{n,Z}) + |Z|^2 \left(S(i_{n,Q_1}) + \frac{S(i_{n,Q_2})}{n^2} \right) \tag{4.10}$$

The noise from Q_1 and Q_2 equals the collector shot noise $2qI_{C,Q_1}$ and $2qI_{C,Q_2}$, respectively. If for I_{C,Q_1} the minimum value (efficiency!) which equals the maximum of the ratio of the peak value $v_{S,p}$ of the signal voltage of the source and Z, and $I_{C,Q_2} = nI_{C,Q_1}$ is chosen, this results in:

$$S(v_{n,\mathrm{eq}}) = 4kT\mathrm{Re}(Z) + |Z|^2 \frac{n+1}{n} 2q \ \max\left(\frac{v_{S,p}}{Z}\right) \tag{4.11}$$

From this expression, we can draw the conclusion that it is best to choose Z as small as possible. However, for values of Z less than the reciprocal value of the desired transfer function, it can be shown that the power efficiency is seriously degraded. Z therefore has to be chosen in such a way that

- the equivalent input noise voltage source $S(v_{n,\mathrm{eq}})$ is less than the maximum acceptable noise contribution, and
- the feedback impedance Z is larger than $1/A_{f\infty}$, if possible, and
- Z is integratable

In low-power integrated circuits, these demands often conflict and an acceptable compromise has to be found.

4.2.3 Transimpedance amplifiers and voltage amplifiers

The basic configurations of a transimpedance amplifier and a voltage amplifier are depicted in Figures 4.5 and 4.6, respectively. Because they are dealt with extensively in [3], and both have a voltage output, which makes them less suitable for low-power applications, we do not discuss them here.

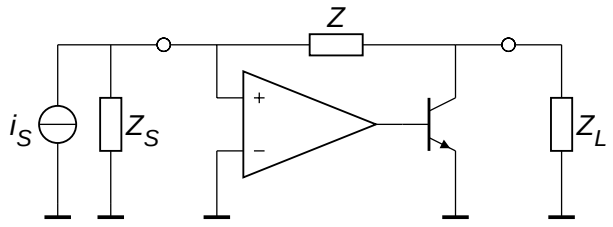

Figure 4.5: A transimpedance amplifier

4.3 The input stage

To here the op amp has been treated as if it were noise free. In practice, an op amp always contributes some noise. However, this contribution can be kept sufficiently

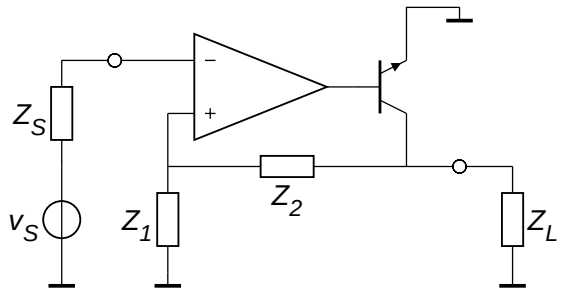

Figure 4.6: A voltage amplifier

small, as shown subsequently. All the noise sources in the op amp can be shifted toward the input of the op amp and modeled as a noise voltage source v_n in series with the input of the op amp and a noise current source i_n in parallel with the op amp's input. This is depicted in Figure 4.7. These noise sources, in turn, can be shifted toward the input of the amplifier and transformed into one noise source.

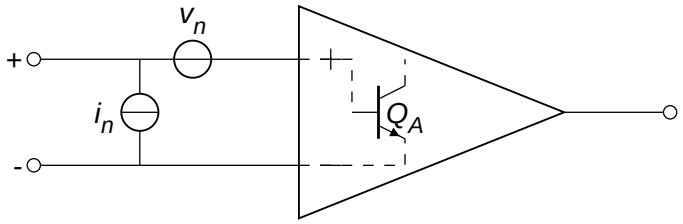

Figure 4.7: Noisy op amp modeled by a noise-free op amp and two noise sources at the input

For the current amplifier depicted in Figure 4.1, this results in an equivalent noise current source $i_{n,\mathrm{eq}}$ with a power density spectrum $S(i_{n,\mathrm{eq}})$:

$$S(i_{n,\mathrm{eq}}) = S(i_n) + S(v_n)\left|Y_S + \frac{Y_1 Y_2}{Y_1 + Y_2}\right|^2 \tag{4.12}$$

in which $Y = 1/Z$.

For the transconductance amplifier shown in Figure 4.4, an equivalent noise voltage source $v_{n,\mathrm{eq}}$ is found.

$$S(v_{n,\mathrm{eq}}) = S(v_n) + S(i_n)|Z_S + Z|^2 \tag{4.13}$$

When we integrate these two spectra over the frequency range of interest, we obtain an expression for the equivalent noise power at the input, $P_{n,\mathrm{eq}}$, which is a function of the collector current of the first stage of the op amp I_{C,Q_A}. As the spectrum of the noise current source i_n is proportional to this collector current ($S(i_n) \approx 2qI_{C,Q_A}/B_F$) and the noise voltage source v_n is inversely proportional to

this collector current ($S(v_n) \approx 2qV_T^2/I_{C,Q_A}$) a minimum can be found for the noise power [3].

In practice, however, in many situations the source signal already contains some noise and we are able to vary the collector current of the first stage of the op amp over various decades around this optimum without seriously affecting the noise behavior of the complete amplifier. We discuss the use of this favorable property in a later section with relation to the amplifier loop gain. From the efficiency point of view, we should better not choose I_{C,Q_A} to be larger than the sum of the collector currents of Q_1 and Q_2 or smaller than the base current of the next stage.

4.4 The output stage

The next step in our design of low-voltage low-power integrated negative-feedback amplifiers is the choice of a proper output stage. This choice depends on the output capability and the power efficiency. In both the current amplifiers and the transconductance amplifier, this output stage is Q_2. In view of the output capability, Q_2 must be biased at a collector current, I_{C,Q_2}, which equals at least the peak value of the signal current coming from Q_2. This signal current, in turn, equals $A_{f\infty}$ times the source signal. Thus for the current amplifiers

$$I_{C,Q_2} \geq A_{f\infty} i_{S,p} \tag{4.14}$$

and for the transconductance amplifier

$$I_{C,Q_2} \geq A_{f\infty} v_{S,p} \tag{4.15}$$

From the power efficiency point of view, however, this collector bias current should better not be chosen to be much larger than the peak value of the signal current. Thus, a compromise must be found: a practical value of 1.2 times as large will do.

4.5 Loop gain

The next aspects in the design of amplifiers to be addressed are distortion, accuracy and bandwidth, mainly determined by one parameter, viz. the loop gain $A\beta$. We evaluate the loop gain for both amplifier types.

4.5.1 Current amplifiers

Now suppose the op amp can be modeled as a current amplifier with a current gain G, an input impedance Z_{in} and an output impedance Z_{out} (Figure 4.8). This is a

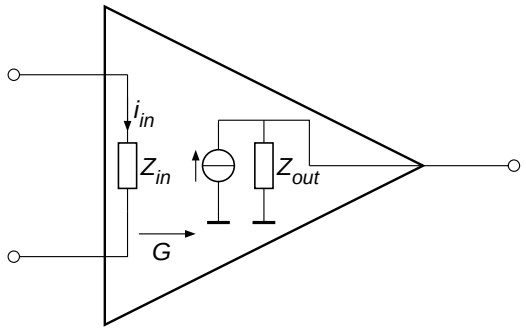

Figure 4.8: The op amp modeled as a current amplifier with a current gain G, an input impedance Z_{in} and an output impedance Z_{out}

quite practical situation. For example, if the op amp is realized by two transistors in cascade, $G = \beta_F^2$, $Z_{\text{in}} = \beta_F/g_m$ and $Z_{\text{out}} = \mu/g_m$. When $Z_{\text{out}} \gg \beta_F/g_m$, we find for the loop gain $A\beta$ of the two-impedance amplifier ($\mu \gg g_m Z_2$):

$$A\beta = -\frac{1}{2}\frac{Z_2}{Z_2 + Z_1 + Z_S//Z_{\text{in}}}\frac{Z_S}{Z_S + Z_{\text{in}}}G\beta_F \tag{4.16}$$

With $A_{f\infty} = -\frac{Z_2+Z_1}{Z_2}$ this can be rewritten as

$$A\beta = \frac{1}{2}\frac{1}{A_{f\infty}}\frac{Z_2 + Z_1}{Z_2 + Z_1 + Z_S//Z_{\text{in}}}\frac{Z_S}{Z_S + Z_{\text{in}}}G\beta_F \tag{4.17}$$

Replacing Z_1 and Z_2 by R_1 and R_2, respectively, this results in an expression for the loop gain of the two-resistance amplifier:

$$A\beta = \frac{1}{2}\frac{1}{A_{f\infty}}\frac{R_2 + R_1}{R_2 + R_1 + Z_S//Z_{\text{in}}}\frac{Z_S}{Z_S + Z_{\text{in}}}G\beta_F \tag{4.18}$$

For $A\beta$ of the scaling current amplifier we find ($\mu_{Q_1} \gg g_{m,Q_1}(Z_S//Z_{\text{in}})$):

$$A\beta = -\frac{g_{m,Q_1}}{g_{m,Q_1} + g_{m,Q_2}}\frac{Z_S}{Z_S + Z_{\text{in}}}G\beta_F \tag{4.19}$$

With $A_{f\infty} = -\frac{g_{m,Q_2}}{g_{m,Q_1}}$ this can be rewritten as:

$$A\beta = \frac{1}{A_{f\infty} - 1}\frac{Z_S}{Z_S + Z_{\text{in}}}G\beta_F \tag{4.20}$$

Now we are able to compare the two-resistance amplifier and the scaling amplifier with respect to their loop gains. For this purpose we calculate the ratio F, defined as

$$F = \frac{\left|A\beta_{\text{scaling current amplifier}}\right|}{\left|A\beta_{\text{two-resistance current amplifier}}\right|} \tag{4.21}$$

This results in

$$F = 2\frac{A_{f\infty}}{A_{f\infty}-1}\left|\frac{R_2+R_1+Z_S//Z_{\text{in}}}{R_2+R_1}\right| > 2\frac{A_{f\infty}}{A_{f\infty}-1} > 1 \;\forall(A_{f\infty} < -1) \tag{4.22}$$

This expression indicates that F is larger than one as long as the absolute value of the asymptotic gain (the ideal transfer) is larger than one. However, the asymptotic gain of the two-resistance amplifier equals $(R_1 + R_2)/R_2$ and thus always meets this condition. Therefore F is always larger than one. For this reason, the scaling current amplifier is always the best choice with regard to loop gain.

From both (4.17) and (4.20) it also follows that the input impedance of the op amp, Z_{in}, is best chosen to be as small as possible. For a bipolar input stage, this comes down to choosing the collector current of the first stage, I_{C,Q_A}, to be as large as possible. Again, in view of the efficiency, we had better not choose I_{C,Q_A} to be larger than the sum of the collector currents of Q_1 and Q_2 or smaller than the base current of the next stage.

4.5.2 Transconductance amplifiers

Following the same procedure as that given in the former subsection, an expression is found for the loop gain $A\beta$ of the transconductance amplifier:

$$A\beta = -\frac{g_{m,Q_1}}{g_{m,Q_1}+g_{m,Q_2}}\frac{Z}{Z+Z_S+Z_{\text{in}}}G\beta_F \tag{4.23}$$

With $g_{m,Q_2} = g_{m,Q_1}ZA_{f\infty}$ this can be rewritten as:

$$A\beta = -\frac{1}{1+ZA_{f\infty}}\frac{Z}{Z+Z_S+Z_{\text{in}}}G\beta_F \tag{4.24}$$

From this expression, it follows that also for a transconductance amplifier, Z_{in} is best chosen to be as small as possible, and thus I_{C,Q_A} as large as possible. In the interests of efficiency we had better not choose I_{C,Q_A} to be larger than the sum of the collector currents of Q_1 and Q_2 or smaller than the base current of the next stage.

4.6 High-frequency behavior

In this section, we deal with some aspects of the high-frequency behavior of low-voltage low-power negative-feedback amplifiers. As the common-emitter (CE) stage can be considered as a basic amplifier stage, we take a closer look at the small-signal diagram of this stage connected between source (i_S, Z_S) and load (Z_L). See Figure 4.9. For the current gain A_i we find

$$A_i = \frac{i_L}{i_S} = -\frac{g_m Z_f Z'_S}{Z_f + Z'_S + Z_L + g_m Z'_S Z_L} \tag{4.25}$$

with $Z_f = 1/j2\pi f C_\mu$, $Z'_S = Z_S // r_\pi // (1/j2\pi f C_\pi)$ and $Z'_L = Z_L // r_o$.

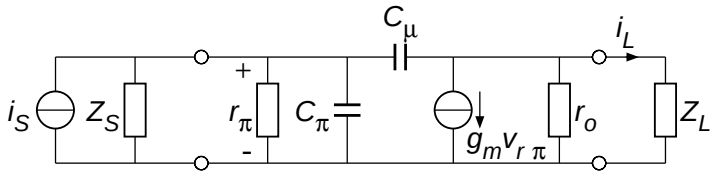

Figure 4.9: Simplified small-signal diagram of a CE stage

From this expression, it can be concluded that there is a strong interaction between source and load due to the local (shunt) feedback by C_μ, which degrades the designability of the high-frequency behavior. This interaction can be prevented by shunting the output with a low impedance. We thus need a current follower. Often, the demands made on this subcircuit can be much less than those made on the total amplifier, and it may be possible to use a single-stage solution. A well-known example is the common-base (CB) stage. The combination of a CE and a CB stage is also known as a 'cascode' stage. Another one-stage implementation of a current follower is the current mirror (CM), which can be regarded as the 'low-voltage counterpart' of the CB stage. We call the latter solution a 'cascade' stage. Both solutions are depicted in Figure 4.10.

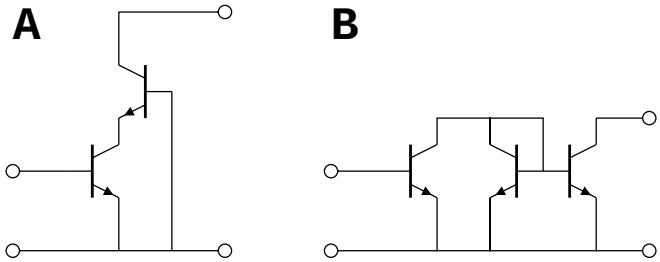

Figure 4.10: Two ways of shunting the output of a CE stage with a low impedance: a cascode (CE + CB) stage (A) and a cascade (CE+CM) stage (B)

Note that the cascode stage has an inverting transfer, while the cascade stage is non-inverting. Compared to a single CE stage, both stages also have a slightly deteriorated noise behavior . However, this does not often pose a problem.

If all the transistors are supposed to have the same parameters and to be in the same operating point, if the influence of r_o and the substrate capacitances is negligible and if g_m is much larger than $g_\pi (= 1/r_\pi)$, then the transmission parameters of the CE, CB and CM stage are given by

$$A_{CE} = \frac{sC_\mu}{sC_\mu - g_m} \tag{4.26}$$

$$B_{CE} = \frac{1}{sC_\mu - g_m} \tag{4.27}$$

$$C_{CE} = \frac{sC_\mu(g_m + sC_\pi)}{sC_\mu - g_m} \tag{4.28}$$

$$D_{CE} = \frac{g_\pi + s(C_\pi + C_\mu)}{sC_\mu - g_m} \tag{4.29}$$

$$A_{CB} = \frac{sC_\mu}{g_m} \tag{4.30}$$

$$B_{CB} = \frac{1}{g_m} \tag{4.31}$$

$$C_{CB} = \frac{sC_\mu(g_m + sC_\pi)}{g_m} \tag{4.32}$$

$$D_{CB} = \frac{g_m + sC_\pi}{g_m} \tag{4.33}$$

and

$$A_{CM} = \frac{sC_\mu}{sC_\mu - g_m} \tag{4.34}$$

$$B_{CM} = \frac{1}{sC_\mu - g_m} \tag{4.35}$$

$$C_{CM} = \frac{sC_\mu(2g_m + 2sC_\pi)}{sC_\mu - g_m} \tag{4.36}$$

$$D_{CM} = \frac{g_m + s(2C_\pi + C_\mu)}{sC_\mu - g_m} \tag{4.37}$$

Now we are able to find the transmission parameters of the cascode (CE+CB) stage and the cascade (CE+CM) stage (Chapter 2). For the cascode stage we obtain

$$A_{CE+CB} = \frac{g_m + s(C_\pi + C_\mu)}{g_m(sC_\mu - g_m)} sC_\mu \tag{4.38}$$

$$B_{CE+CB} = \frac{g_m + s(C_\pi + C_\mu)}{g_m(sC_\mu - g_m)} \tag{4.39}$$

$$C_{CE+CB} = \frac{(g_m + sC_\pi)(g_\pi + s(C_\pi + 2C_\mu))}{g_m(sC_\mu - g_m)} sC_\mu \tag{4.40}$$

$$D_{CE+CB} = \frac{(g_m + sC_\pi)(g_\pi + s(C_\pi + 2C_\mu))}{g_m(sC_\mu - g_m)} \tag{4.41}$$

and for the cascade stage

$$A_{CE+CM} = \frac{sC_\mu(2g_m + s(C_\pi + C_\mu))}{(sC_\mu - g_m)^2} \tag{4.42}$$

$$B_{CE+CM} = \frac{g_m + s(2C_\pi + 2C_\mu)}{(sC_\mu - g_m)^2} \tag{4.43}$$

$$C_{CE+CM} = \frac{sC_\mu(g_m + sC_\pi)(2g_\pi + s(2C_\pi + 3C_\mu))}{(sC_\mu - g_m)^2} \tag{4.44}$$

$$D_{CE+CM} \approx \frac{(g_\pi + s(C_\pi + 2C_\mu))(g_m + s\frac{2C_\pi^2 + 4C_\pi C_\mu + C_\mu^2}{C_\pi + 2C_\mu}))}{(sC_\mu - g_m)^2} \tag{4.45}$$

The reciprocals of these transmission parameters are the more commonly known transfer parameters (μ, γ, ζ and α) whose asymptotic Bode plots are plotted (up to ω_T) in Figures 4.11, 4.12 and 4.13 for the CE, cascode and cascade stage, respectively.

In low-power circuits C_μ and C_π are both merely the result of fixed charges stored in the transistor's space-charge layers rather than charges associated with the mobile carriers in the transistor (Chapter 3). They therefore lie in the same order of magnitude. We see that up to $\omega_T/2$, the transfer parameters μ, γ and α are the same for all stages. This means that in situations where the transfer is determined mainly by these parameters, i.e., when the source or load impedance is small, there is no preference for either a CE, cascode or cascade stage.

For the trans-impedance factor ζ the situation is rather different. From (4.40) and (4.44) we see that ζ_{CE+CB} and ζ_{CE+CM} exceed ζ_{CE} by a factor between 1 and β_F up to frequencies of almost ω_T. The interaction between source and load is decreased and both the cascode and the cascade stage behave as single, nearly unilateral, amplifier stages. From the viewpoint of designability this is an enormous advantage.

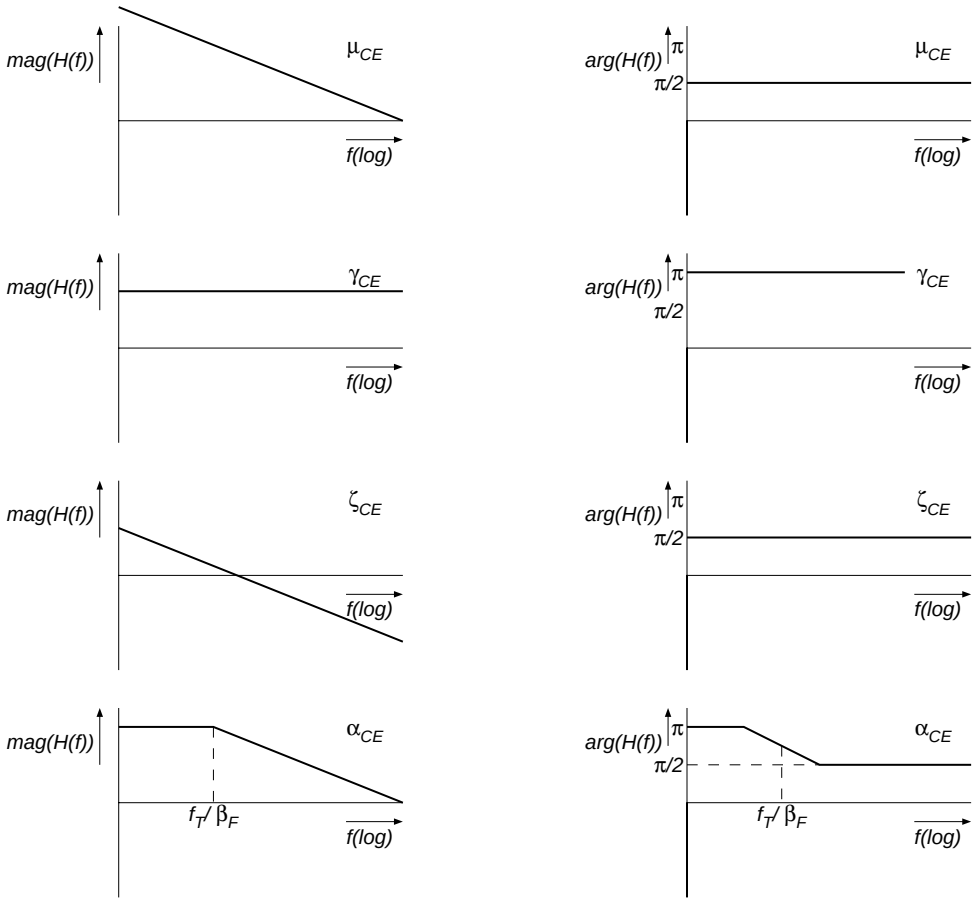

Figure 4.11: Bode plots of the CE stage as function of the frequency up to ω_T

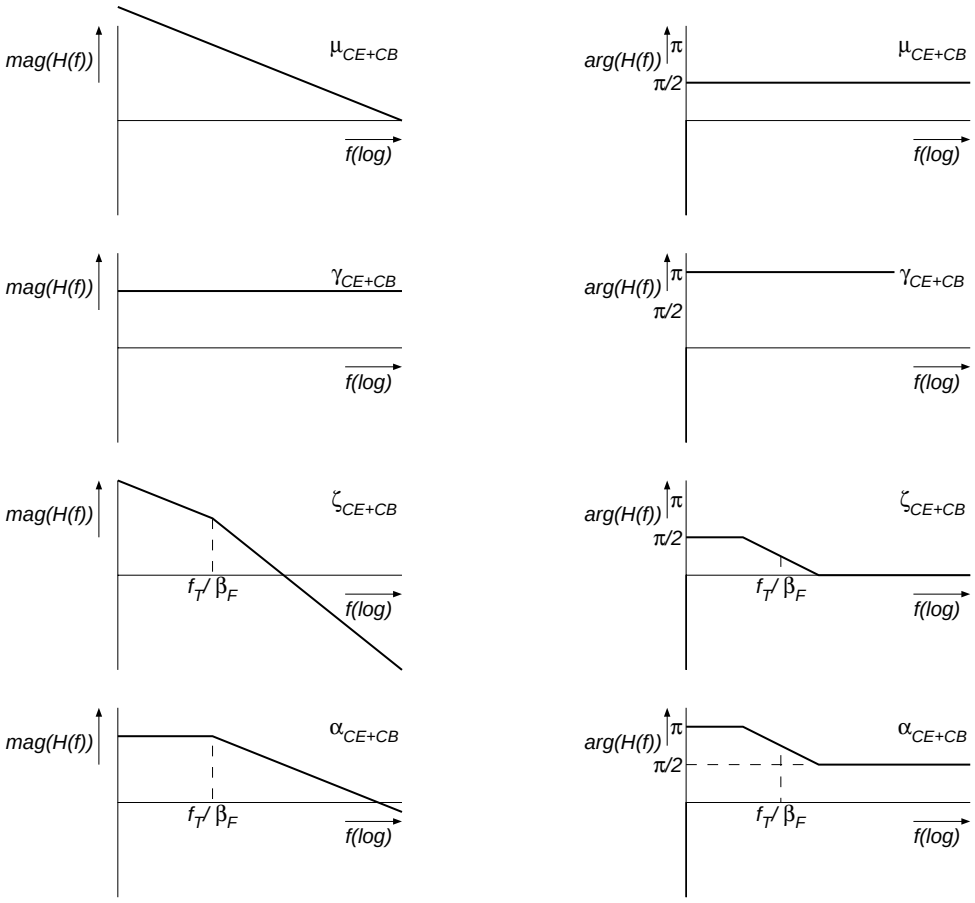

Figure 4.12: Bode plots of the cascode (CE+CB) stage as function of the frequency up to ω_T

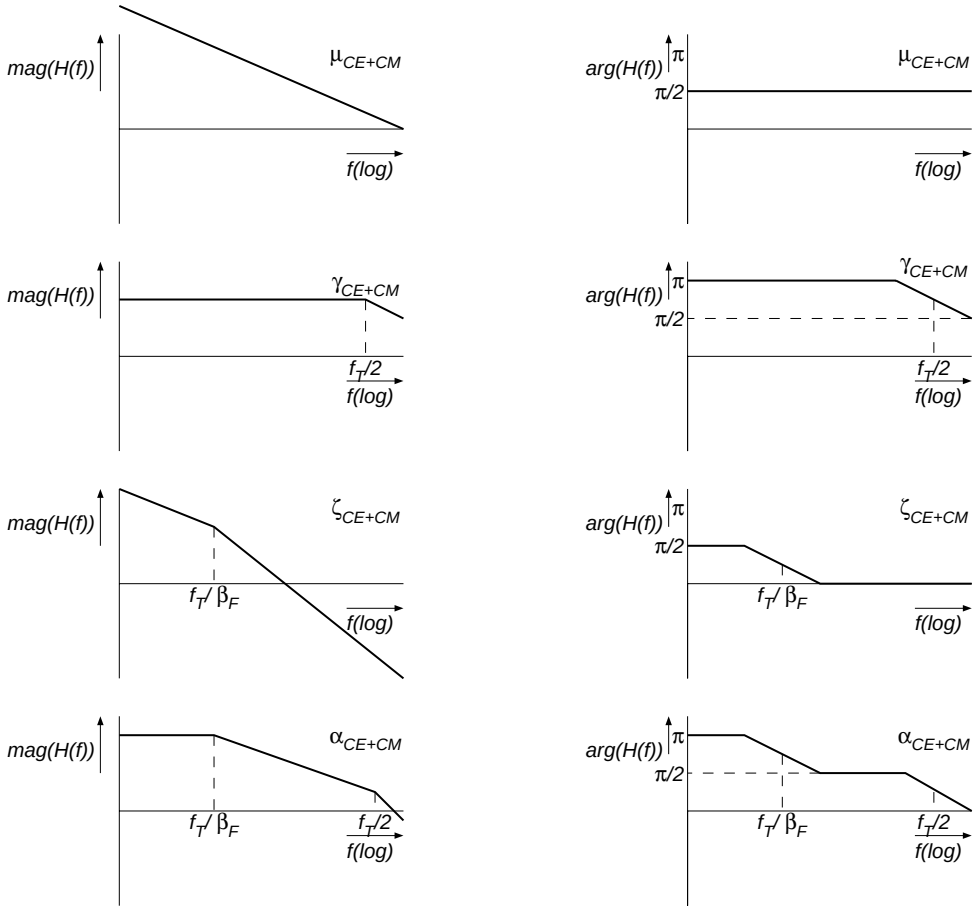

Figure 4.13: Bode plots of the cascade (CE+CM) stage as function of the frequency up to ω_T

The cascode stage, however, is of less practical use in low-voltage circuits. To clarify this we consider Figure 4.14. Two possible implementations of a cascode stage together with an appropriate biasing circuit are depicted.

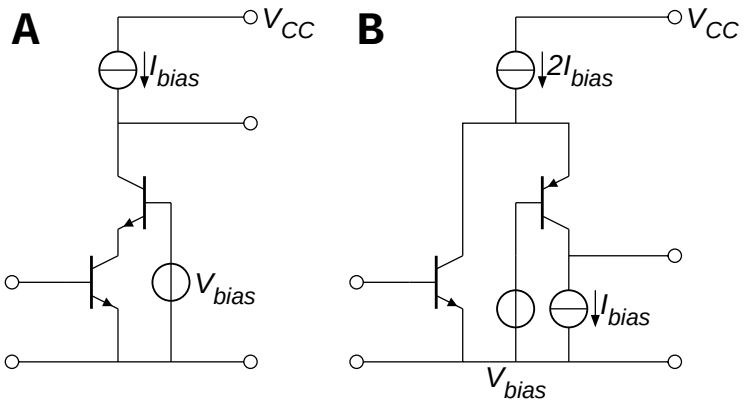

Figure 4.14: Biasing the cascode stage

From Figure 4.14A, we observe that the output voltage swing is limited by the supply voltage V_{CC}, the voltage across the terminals of the current source I_{bias} and the sum of the saturation voltages of both transistors, while in Figure 4.14B the output voltage swing is limited by the supply voltage, the saturation voltage of the CB stage and twice the voltage across the two current sources.

Apart from that an extra voltage source V_{bias} is required, which must be rather accurate to prevent both transistors from saturating.

The cascade stage does not have these major drawbacks (Figure 4.15A and B). In neither circuits is there a need for an extra voltage source, and the maximum output voltage swing is limited by the supply voltage, only one voltage across the terminals of a current source and only one saturation voltage. It is for this reason that this stage is supposed to be superior with respect to the designability of the high-frequency behavior in low-power low-voltage circuits.

4.7 Biasing

In this section, we deal with the various biasing schemes, and attempt to select the one that is most suited for low-power, low-voltage integrated negative-feedback amplifiers.

If we assume that the design of the signal path was completed in the foregoing stages, then the bias circuit is not permitted to have any influence on the signal transmission. This means that either the signal can be superposed on the bias quantities by connecting a voltage source in series with the signal source, or the signal can be superposed on the bias quantities by connecting a current source

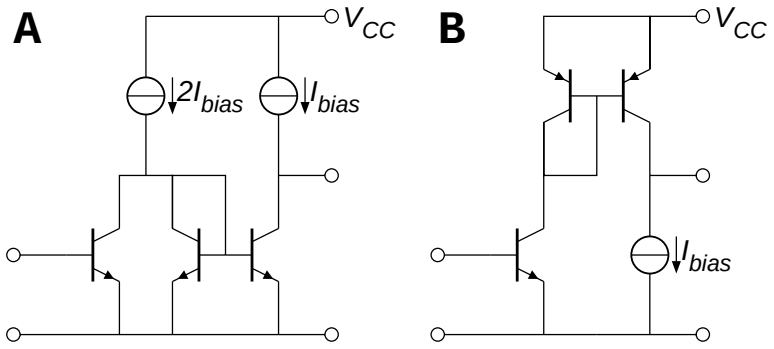

Figure 4.15: Biasing the cascade stage

in parallel with the signal source. However, the first solution implies that either the signal source or the bias source must have floating output ports. Further, the connection of two (voltage) sources in series restricts the possible voltage swing of the signal source, and therefore its dynamic range. Since the latter solution does not have these disadvantages, it obviously is the better one, especially for low-voltage circuits.

4.7.1 Four fundamental ways of biasing

Generally, there are four ways to accomplish the correct biasing of one or more stages in a negative-feedback amplifier.

First, there is the possibility of making no distinction between the bias quantities and the signal quantities. The circuit already contains a negative feedback loop which can assure proper biasing. Very often, this introduces unpredictable and undesired signal components which cannot be distinguished from the actual information (temperature drift, offset). As an example, we consider a negative feedback transimpedance amplifier (the simplest one being a shunt stage). Here, the base-emitter voltage and the voltage drop over the feedback resistor determine the output voltage. It is clear that this kind of biasing is suited for restricted applications only.

Another possibility is the separation of the bias and signal quantities in the frequency domain. In this case, a bias circuit can have an additional feedback loop, which is active only at very low frequencies. We therefore need a network of which the transfer parameters depend on the frequency (e.g. a lowpass filter). Of course, this technique can be applied only when the signal quantities do not have a DC component

The third possibility is the separation of the bias and signal quantities in the time domain. As an example we mention auto-zero techniques. In general, these techniques can be applied only when the input signal shows a time-discrete char-

acter. During the time when there is no relevant information in the input signal, a feedback loop is made active (by means of a switch) and restores the output quantity at a reference level.

The final possibility is the separation of the bias and signal quantities in common-mode (CM) and differential-mode (DM) signals. The DM quantities refer to the ideally isolated situation, where the circuit can be considered as a twoport. The CM quantities refer to ground or one of the other supply rails. These quantities are called orthogonal when they do not influence each other, as is the case with balanced circuits. Although, in practice, this is never completely true, the main advantage of this biasing technique is that there is no need for a lowpass filter or switches. Therefore, this technique is assumed to be superior and very well suited for integrated circuits. For this reason we adopt it as the basis for the design of bias circuitry.

Other advantages of separating the signal and bias quantities in DM and CM signals are that all even-order distortion generated in the circuit ideally appears as a CM signal. It, therefore, is not present in the output signal. Further, when the source impedance approaches infinity, the dynamic range improves 3 dB.

A major disadvantage of this technique is that twice as many components are required, which doubles the power consumption. Only passive components connected to ground can be replaced by floating components with a doubled impedance.

Because the CM signal ideally does not contain any information, our design aim for the CM circuit is not to realize a low-noise, accurate signal transfer, with a large bandwidth and low distortion, but to realize a circuit that is unconditionally stable and reaches the expected operation point.

4.7.2 Biasing in the current domain

Just as for the signal behavior, it can be very attractive for the bias behavior of a circuit to operate as much as possible in the current domain. This means, that at the output of the amplifier the output current is compared with a reference (bias) current and by means of the error signal the common-mode current sources at the input are adjusted.

Our starting point is a symmetrical amplifier the signal path of which was earlier completed. This amplifier can be considered as a *series-series connection of two two-ports* (Chapter 2). See Figure 4.16. The common-mode nodes can be found on the axis of symmetry and will be used for the biasing. As both source and load can be either floating or fixed to some voltage, there are four possible biasing schemes:

- for a symmetrical amplifier with floating source and floating load,

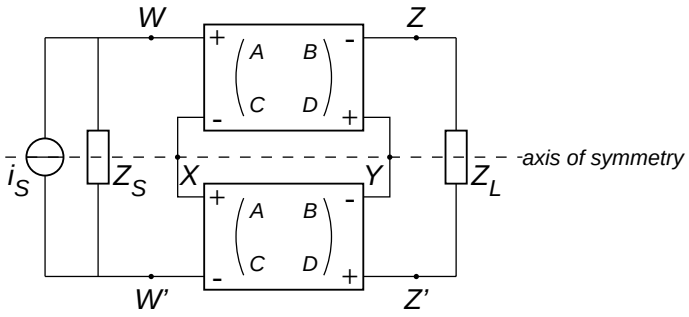

Figure 4.16: A symmetrical amplifier

- for a symmetrical amplifier with floating source and fixed load,
- for a symmetrical amplifier with fixed source and floating load, or
- for a symmetrical amplifier with fixed source and fixed load.

These biasing schemes are the subject of the following subsections.

4.7.3 Biasing a symmetrical amplifier with floating source and floating load

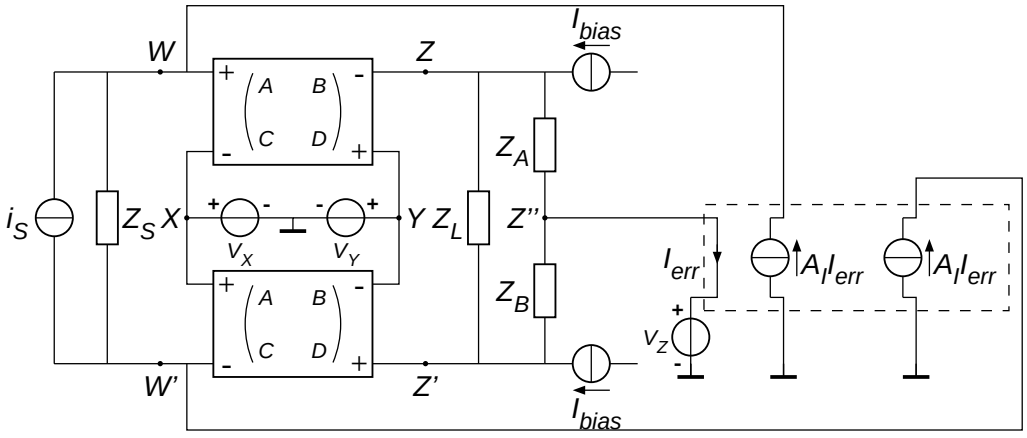

Figure 4.17: The biasing scheme for a symmetrical amplifier with floating source and floating load

The general solution for low-voltage low-power symmetrical amplifiers with floating source and floating load is shown in Figure 4.17. The operation is as follows. Nodes X and Y are biased by means of the voltage sources V_X and V_Y. In practice, in many situations, these voltage sources can be zero or some supply voltage, in which case X and Y can be tied directly to ground or one of the other supply rails.

The currents through Z and Z' originate from two current sources I_{bias} and set the proper bias currents of the last stages of the amplifier. The output voltages of node Z and Z' are compared with a reference voltage V_Z and the difference is transformed into two currents by means of impedances Z_A and Z_B (Z_A and $Z_B \gg Z_L$). These currents together form the common-mode error signal I_{err}. This current is amplified by a non-inverting current amplifier with double outputs and is fed to nodes W and W', thus setting their voltages. If the absolute value of the common-mode loop gain is much larger than one (for DC), then the error signal is nullified and the complete amplifier is biased correctly.

An example of an amplifier using this biasing technique can be found in [7].

4.7.4 Biasing a symmetrical amplifier with floating source and fixed load

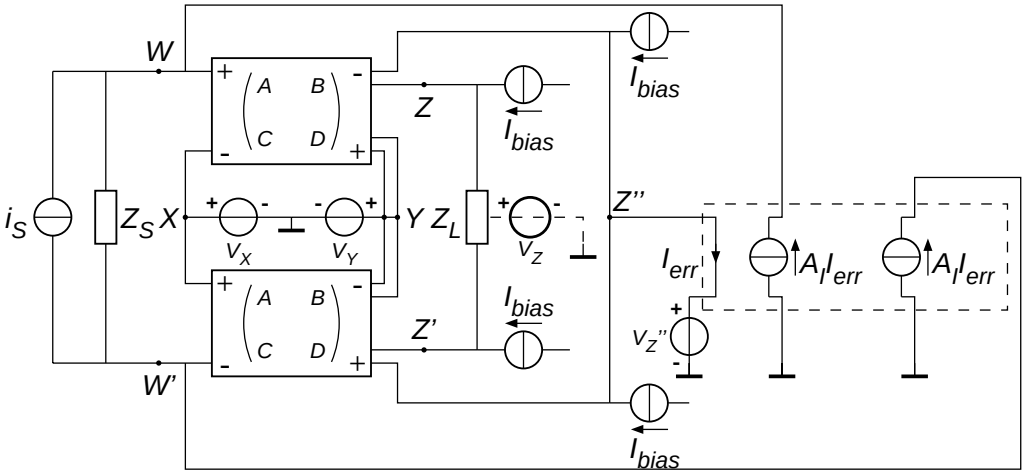

Figure 4.18: The biasing scheme for a symmetrical amplifier with floating source and fixed load

The general biasing scheme for symmetrical amplifiers with floating source and fixed load is given in Figure 4.18. The operation is as follows. In order to set the output bias currents, an identical output is formed inside the amplifier. The voltage of nodes Z and Z' are already set by the voltage of the load (V_Z in Figure 4.18) so we only need to take care of the output bias currents. Therefore all four outputs are biased by a current source I_{bias}. The difference between the currents coming from the dummy outputs and these bias currents is summed in node $Z"$, thereby forming a common-mode error signal I_{err}. $V_{Z''}$ sets the output voltage of both dummy outputs. I_{err} is then amplified by a non-inverting current amplifier with double outputs and fed to nodes W and W', thus setting their voltages. If the

absolute value of the common-mode loop gain is much larger than one (for DC), then the error signal is nullified and the complete amplifier is biased correctly. V_X and V_Y set the voltage of nodes X and Y, respectively. Again, in practice, these voltages often can be zero or some supply voltage.

An example of an amplifier using this biasing technique can be found in [6].

4.7.5 Biasing a symmetrical amplifier with fixed source and floating load

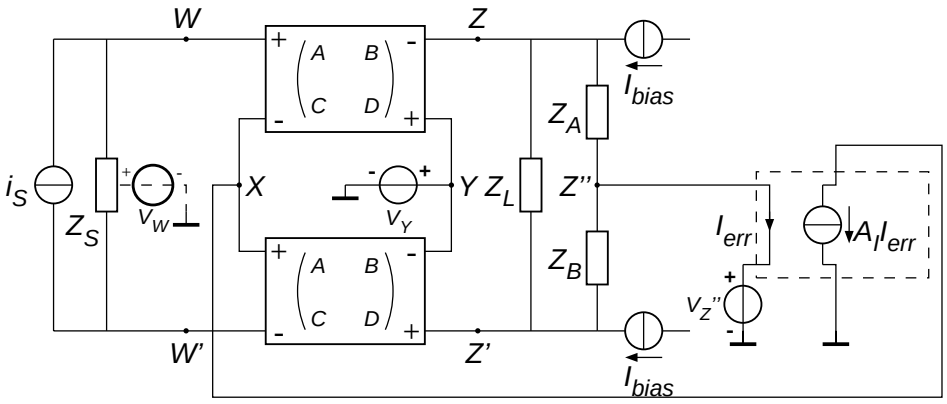

Figure 4.19: The biasing scheme for a symmetrical amplifier with fixed source and floating load

Now the situation is just the opposite. The general biasing scheme for symmetrical amplifiers with fixed source and floating load is depicted in Figure 4.19. The operation is as follows. Similar to that of the amplifier with floating source and floating load, the output is set by two bias sources I_{bias}, and an error signal containing information about the difference between the common-mode output voltage and the reference voltage $V_{Z''}$ is generated. However, now this current is amplified by an inverting amplifier and fed back to node X, as the voltages of nodes W and W' had already been set by the voltage of the source (V_W in Figure 4.19). If the absolute value of the common-mode loop gain is much larger than one, the amplifier is biased correctly. V_Y sets the voltage of node Y. In practice, often this voltage can be zero or some supply voltage.

4.7.6 Biasing a symmetrical amplifier with fixed source and fixed load

Last but not least, we give the biasing scheme of a symmetrical amplifier with both the source and load fixed at a certain reference level. This is shown in Figure

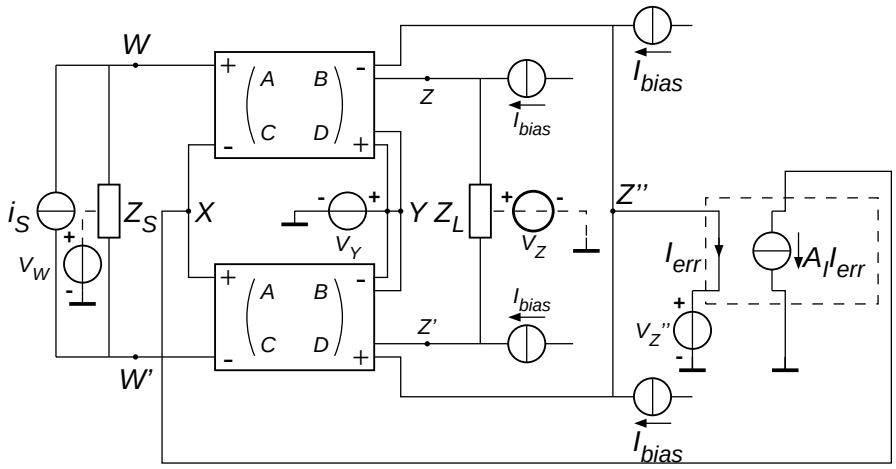

Figure 4.20: The biasing scheme for a symmetrical amplifier with fixed source and fixed load

4.20. The operation is as follows. Similar to that of the amplifier with floating source and fixed load, the output is set by four bias sources I_{bias}, and an error signal containing information about the difference between the output currents of the dummy outputs and these bias sources is generated. Similar to that of the preceding amplifier, this current is amplified by an inverting amplifier and fed back to node X, as the voltages of nodes W and W' had already been set by the voltage of the source (V_W in Figure 4.20). If the absolute value of the common-mode loop gain is much larger than one, the amplifier is biased correctly. V_Y sets the voltage at node Y. Often this voltage can be zero or some supply voltage.

4.8 An example: a microphone preamplifier for use in hearing instruments

An example of a circuit that has been designed using the design theory as presented in the foregoing sections can be found in [7]. It concerns an amplifier that amplifies the output quantity of an electret microphone. The amplifier itself is part of a hearing instrument that further consists of: a controllable attenuator [8], an automatic gain control [9], a filter [10], a controllable amplifier [11] and a power amplifier [12]. Although the output *voltage* of the electret microphone is proportional to the air pressure, the linearity of the transfer of the microphone is not essentially different when using either *voltage* or *current* sensing. Therefore, on that ground neither is preferable to the other.

4.8.1 The basic amplifier configuration

As the electret represents a capacitive source for the preamplifier of about 5 pF, the microphone is, preferably, short-circuited to reduce the influence of the connection wires to a minimum. For this reason, current sensing at the input has been chosen. For the same reason, the output quantity of the amplifier is a current. This brings us to the following basic amplifier configuration: the two-impedance current amplifier (Figure 4.21).

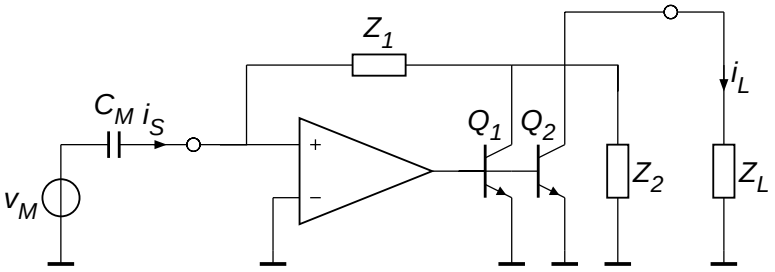

Figure 4.21: Basic configuration of the microphone preamplifier (I)

For the output current i_L, we find

$$i_L = A_{f\infty} i_S = \frac{Z_1 + Z_2}{Z_2} i_S = \frac{Z_1 + Z_2}{Z_2} s C_M v_M \tag{4.46}$$

v_M and C_M being the microphone voltage (which is proportional to the air pressure) and the microphone capacitance, respectively.

4.8.2 The feedback network

In order to have an output current that is proportional to the microphone voltage, the amplifier must perform an integrating transfer function. This can be achieved by choosing a capacitor for Z_1 and a resistor for Z_2 (Figure 4.22). The output current then equals

$$i_L = \frac{1 + sRC}{RC} C_M v_M \tag{4.47}$$

The transfer function also contains a zero at $s = -1/RC$. However, in practice, this zero is well above the audio band, so its influence can be neglected and the former equation can be simplified to

$$i_L = \frac{C_M}{RC} v_M \tag{4.48}$$

The noise contribution of the feedback network originates from the thermal noise generated in the feedback resistor R and the noise generated in Q_1 and Q_2.

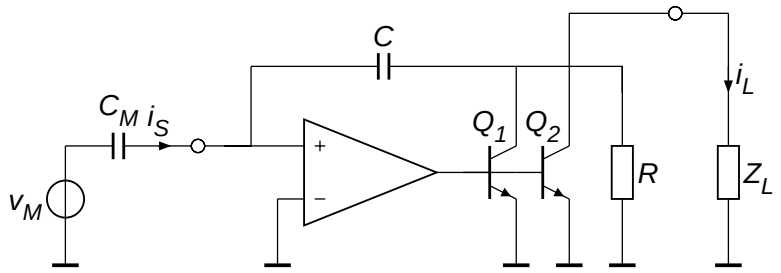

Figure 4.22: Basic configuration of the microphone preamplifier (II)

These noise sources can be transformed into an equivalent input voltage source $v_{n,\mathrm{eq}}$ with a power density spectrum $S(v_{n,\mathrm{eq}})$ in series with the microphone.

$$S(v_{n,\mathrm{eq}}) = \left(4kT/R + 2qI_{C,Q_1} + 2qI_{C,Q_2}\right)\left(\frac{R^2C^2}{C_M^2}\right) \tag{4.49}$$

From this expression we can see that a small value of the feedback capacitor C gives the best noise performance. However, its value is limited by the maximum voltage swing across R, which equals

$$v_R = \frac{C_M}{C}v_M \tag{4.50}$$

The maximum output voltage of the microphone is about 80 mV (peak value). With $C_M = 5$ pF and $C = 4$ pF this results in a maximum peak voltage swing across R of about 100 mV, which is acceptable in this design. With regard to the power efficiency of the total hearing instrument, the output current is chosen to be equal to 10 μA (peak value). R thus equals 10 kΩ.

4.8.3 The input stage

In order to fulfill the noise requirements, we first assume that the noise contribution of the active part of the amplifier is determined by the first stage only and can be modeled as a noise voltage source v_n in series with the input of the op amp and a noise current source i_n in parallel with the input of the op amp. These noise sources are then shifted towards the input of the amplifier and transformed into one noise voltage source in series with the microphone. An equivalent noise voltage source, $v_{n,\mathrm{eq}}$, with a power density spectrum $S(v_{n,\mathrm{eq}})$, is found.

$$S(v_{n,\mathrm{eq}}) = S(v_n)\left(1 + \frac{C}{C_M}\right)^2 + \frac{S(i_n)}{4\pi^2 f^2 C_M^2} \tag{4.51}$$

Since for bipolar transistors $S(v_n) \approx 2kT/g_m$ and $S(i_n) \approx 2kTg_m/B_F$ (Chapter 3), we can draw the conclusion that the noise behavior is mainly determined by

the noise current source i_n for practical values of g_m. This is often the case with a small capacitive source [3]. In order to achieve an acceptable noise behavior, a MOSFET is taken for the input transistor. Now $S(i_n) = 2qI_G$, I_G being the gate leakage current, which is very small. Thus, the noise contribution from the active part of the amplifier is determined by the noise voltage only and can be made sufficiently small by choosing the bias current though the MOSFET to be as high as needed. In this design satisfactory results were obtained using a $800\mu/3\mu$ MOSFET in weak inversion [13], biased at 9 μA.

4.8.4 The output stage

In view of the noise contribution of the output stage (see (4.49)) and the power efficiency the (bipolar) output stages are biased at 10 μA.

4.8.5 Loop gain

The loop gain of the amplifier designed so far can be estimated using (4.16)

$$A\beta = -\frac{1}{2}\frac{Z_2}{Z_2 + Z_1 + Z_S//Z_{\text{in}}}\frac{Z_S}{Z_S + Z_{\text{in}}}G\beta_F \tag{4.52}$$

and results in

$$A\beta \approx -\frac{1}{2}g_{m,\text{MOSFET}}\frac{C}{C + C_M}R\beta_F \tag{4.53}$$

This value is about -84 over the total audio band, giving an inaccuracy of only 1.2 %.

4.8.6 High-frequency behavior

In order to improve the designability of the total amplifier, and to obtain a negative loop — the use of a common-source input stage and a double common-emitter output stage results in a positive loop — an extra current mirror, the low-voltage counterpart of a CB stage, is added. As the feedback loop contains only one dominant pole, no further frequency compensation is necessary.

4.8.7 Biasing

Since the amplifier must be fully integrated and connected to both floating source and load, we have chosen for the biasing scheme as presented in Figure 4.17. This yields the circuit shown in Figure 4.23.

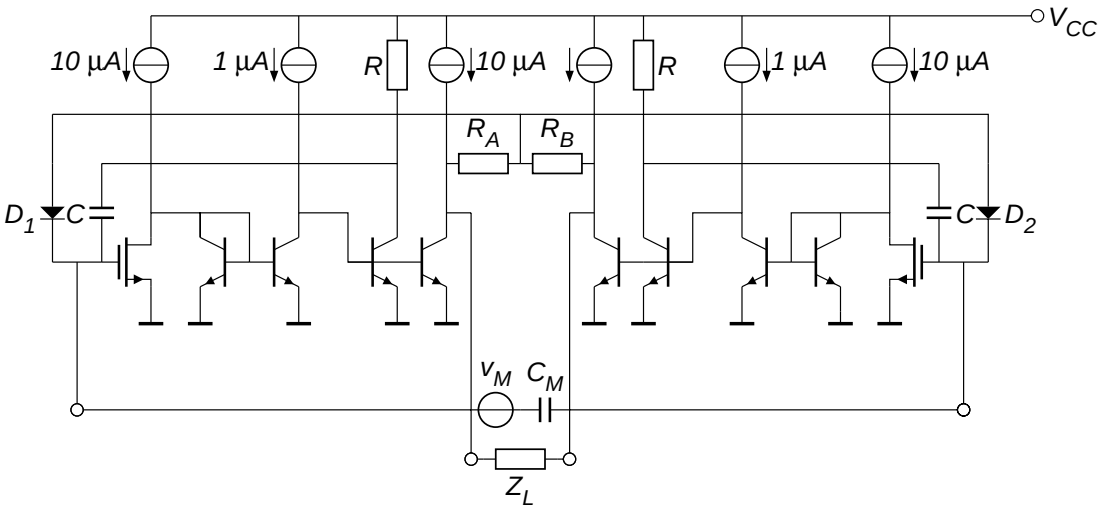

Figure 4.23: The microphone preamplifier with ideal bias circuitry

Resistors R_A and R_B perform the voltage-to-current conversion and must be chosen to be much larger than the load impedance to avoid signal loss. Diodes D_1 and D_2 split this error signal into two and set the voltage at both the inputs. The voltage across these diodes is determined by the gate leakage current of the MOSFETs and the protection circuitry, and is very small. The common-mode output voltage therefore equals the gate-source voltage of both MOSFETs.

In [7] the biasing has been realized using two common-mode feedback loops; one that sets the output voltage at the correct value and one that sets the voltage of both inputs. Although both solutions are very much alike, the biasing circuit proposed here does not influence the signal transfer of the preamplifier and is less complex. Therefore, it is assumed to be superior.

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Chapter 5

Automatic Gain Controls

Kw'éi

Above the marsh there is fire.
The superior man allows variations
Within the normal.

The I Ching

5.1 Introduction

Automatic gain controls (AGCs) are widely used in communication systems to modify the dynamic range of a signal. They can be found in, e.g., radio receivers and transmitters, audio amplifiers and hearing instruments.

An AGC is a circuit that automatically controls its gain in such a way that variations in the input signal result in smaller variations in the output signal. This control action is usually performed by means of a loop that contains a large time constant (e.g. several tens of milliseconds).

In the past, this large time constant was realized by means of a large (external) capacitor. However, in integrated circuit implementations, external components should be avoided as much as possible.

A typical AGC circuit is shown in Figure 5.1. The output signal E_L is compared with a reference level E_K (the knee level) by a comparator that determines whether the integrating circuit — in practice often nothing more than an RC network — is charged (by $E_{\text{att}} - E_{\text{rel}}$) or discharged (by E_{rel}). The output signal of the integrator, E_{int}, forms the control signal of the controlled amplifier. The operation is as follows: When E_{att} is larger than E_{rel}, the output signal E_L is controlled toward the knee level E_K. Variations in the input signal therefore always result in smaller or equal variations in the output signal. The control action requires some

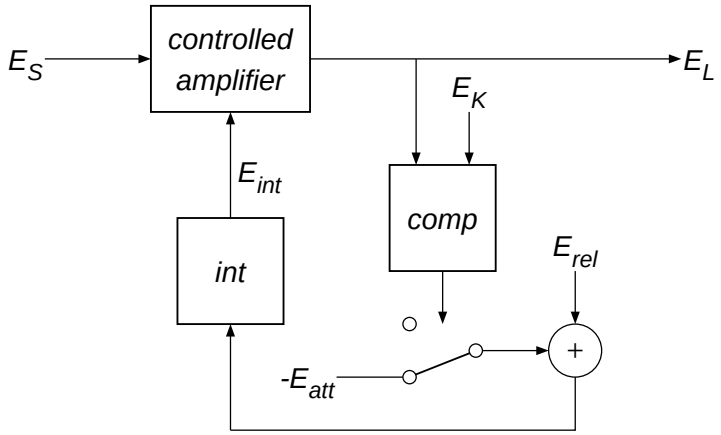

Figure 5.1: Block diagram of an automatic gain control ($C.R. = \infty$)

time. This can be described by the expressions *attack time* and *release time*. The attack time is defined as the time needed for the AGC to respond to a sudden 25 dB increase in the input signal until the output signal is within 2 dB from its final value [1]. Vice versa, the release time is defined as the time required to respond to a sudden 25 dB decrease in the input signal until the output signal is within 2 dB from its final value.

Another important parameter is the *compression ratio* ($C.R.$), defined as the ratio of the variation in the input signal and the variation in the output signal (both in dBs), or

$$C.R. = \frac{\Delta E_{S,\mathrm{dB}}}{\Delta E_{L,\mathrm{dB}}} \tag{5.1}$$

From this expression it can be seen that for $C.R. > 1$ the operation is that of a compressor and for $C.R. < 1$ of an expander.

The circuit given in Figure 5.1 realizes an infinite compression ratio. In the following section, realizations with different compression ratios are discussed.

5.2 AGCs with finite compression ratios

For AGCs with finite compression ratios, the output signal E_L cannot directly be compared with the reference level E_K. We thus need at least one additional amplifier to generate an additional signal out of E_L, E_S or E_K.

5.2.1 Controlled amplifiers in cascade

One way of obtaining a finite compression ratio is to pass the output signal of the AGC, E_L, through another controlled amplifier, which is controlled by the same control signal E_{int}. The output of this second amplifier can then be compared with E_K and thus kept constant. This situation is depicted in Figure 5.2.

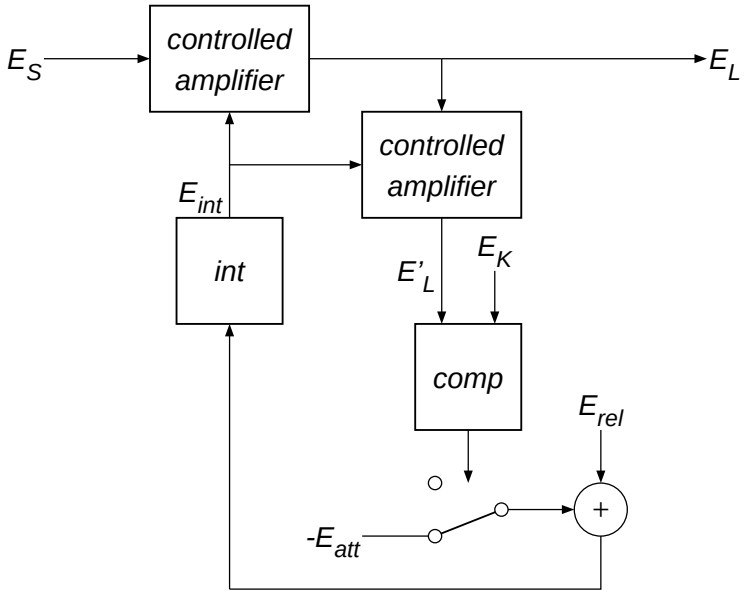

Figure 5.2: AGC with $C.R. = 2$ using two controlled amplifiers in cascade

If the controlled amplifier consists of a simple multiplier three equations can be extracted.

$$E'_L = E_K \tag{5.2}$$
$$E_L = E_S E_{\text{int}} \tag{5.3}$$
$$E'_L = E_L E_{\text{int}} \tag{5.4}$$

with E_L the output signal of the AGC, E'_L the output signal of the second controlled amplifier, which is kept equal to E_K. These equations can be rewritten as follows:

$$E'_L = E_S E_{\text{int}}^2 \tag{5.5}$$
$$E_{\text{int}} = \sqrt{E_K / E_S} \tag{5.6}$$
$$E_L = \sqrt{E_K E_S} \tag{5.7}$$

For the compression ratio of the AGC we thus can write

$$C.R. = \frac{\Delta E_{S,\mathrm{dB}}}{\Delta E_{L,\mathrm{dB}}} = \frac{20 \log E_S}{20 \log \sqrt{E_K E_S}} = 2 \tag{5.8}$$

because E_K is a constant DC level.

Realizing compression ratios other than two is done by using additional controlled amplifiers in cascade. However, because of the greater complexity, this is believed to be of little practical value.

5.2.2 Differently controlled amplifiers

Another possibility is making use of two controlled amplifiers that both have the same input signal E_S, but are controlled by different control signals. This is depicted in Figure 5.3. The output signal of the integrator, E_{int}, is passed to the controlled amplifier that generates the output signal and to a multiplier that multiplies E_{int} by a constant factor m. This multiplied version of E_{int} is then passed to the second controlled amplifier that generates the signal that is to be compared with E_K.

In order for it to operate properly, the input-output relation of the controlled amplifiers cannot be that of a multiplier for this would result in an infinite compression ratio. We therefore assume that both amplifiers realize an exponentially controlled transfer function, or

$$E_{\mathrm{out}} = E_{\mathrm{in}} \exp E_{\mathrm{control}} \tag{5.9}$$

This transfer function can easily be realized, as is shown in Section 5.4. For the circuit shown in Figure 5.3 again three expressions can be found.

$$E'_L = E_K \tag{5.10}$$
$$E_L = E_S \exp E_{\mathrm{int}} \tag{5.11}$$
$$E'_L = E_S \exp m E_{\mathrm{int}} \tag{5.12}$$

These can be rewritten as

$$E'_L = E_K \tag{5.13}$$
$$E_{\mathrm{int}} = \frac{\ln E_K/E_S}{m} \tag{5.14}$$
$$E_L = E_S \exp \frac{\ln E_K/E_S}{m} \tag{5.15}$$
$$= E_S^{1-1/m} E_K^{1/m} \tag{5.16}$$

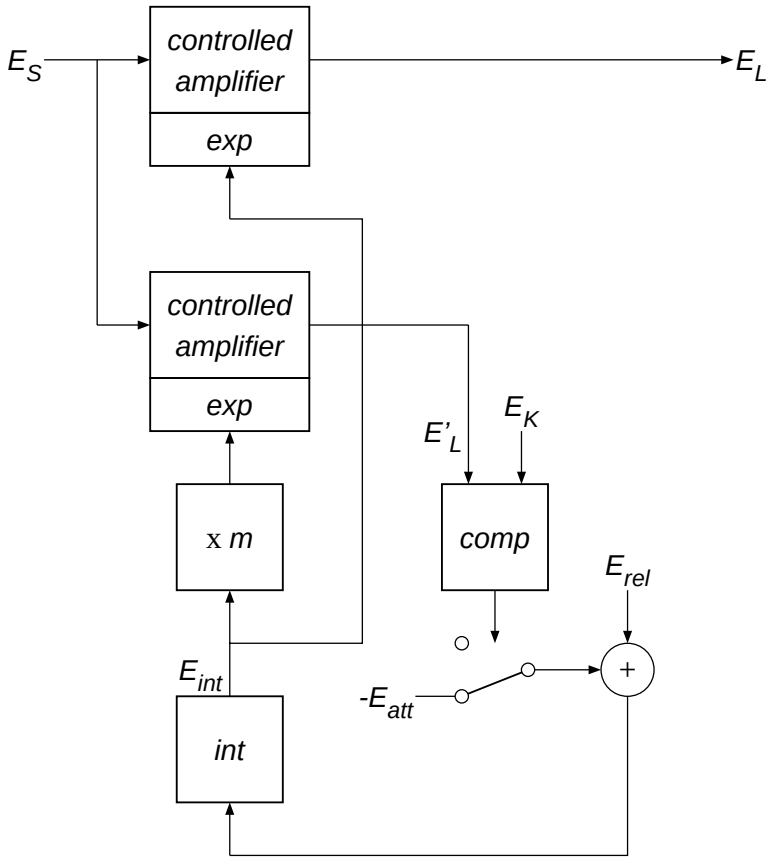

Figure 5.3: AGC with $C.R. = \frac{m}{m-1}$ using differently controlled amplifiers

For the compression ratio we then find

$$C.R. = \frac{\Delta E_{S,\mathrm{dB}}}{\Delta E_{L,\mathrm{dB}}} = \frac{1}{1 - 1/m} = \frac{m}{m-1} \tag{5.17}$$

Using this technique, all compression factors between zero and infinity can be realized. A compression ratio of two, for example, is thus obtained by choosing $m = 2$.

5.2.3 Controlled knee level

Finally there is also the possibility of passing the reference level E_K through another controlled amplifier and comparing its output signal to the output signal of the AGC. This is depicted in Figure 5.4. As E_K contains no signal information (i.e. is a constant DC level) the demands that are made upon the second controlled amplifier can be much less, thereby reducing the circuit complexity.

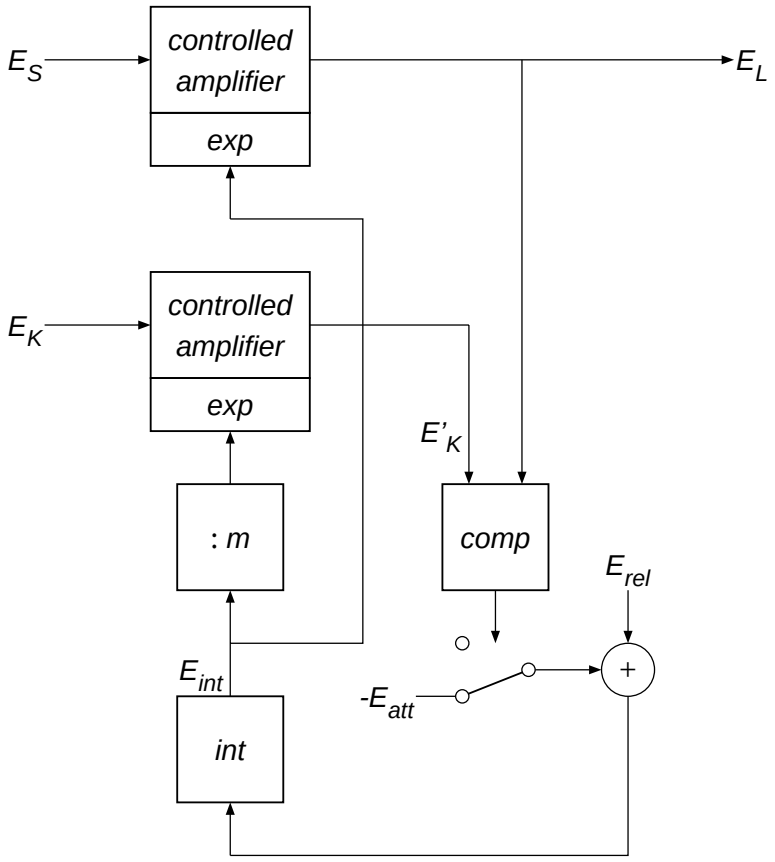

Figure 5.4: AGC with $C.R. = 1 - m$ using a controlled knee level

Again both amplifiers are exponentially controlled. The output signal of the integrator, E_{int}, is passed to the controlled amplifier that generates the output signal of the AGC and to a divider that divides E_{int} by a constant factor m. This divided version of E_{int} is then passed to the second controlled amplifier that generates the signal that is to be compared with the output signal E_L from the reference level E_K. Again three expressions can be found.

$$E'_K = E_L \tag{5.18}$$
$$E_L = E_S \exp E_{\text{int}} \tag{5.19}$$
$$E'_K = E_K \exp E_{\text{int}}/m \tag{5.20}$$

These can be rewritten as

$$E'_K = E_L \tag{5.21}$$

$$E_{\text{int}} = m \ln E'_K / E_K \tag{5.22}$$
$$= m \ln E_L / E_K \tag{5.23}$$
$$E_L = \frac{E_S^{1/(1-m)}}{E_K^{m/(1-m)}} \tag{5.24}$$

For the compression ratio this results in

$$C.R. = \frac{\Delta E_{S,\text{dB}}}{\Delta E_{L,\text{dB}}} = \frac{1}{1/(1-m)} = 1 - m \tag{5.25}$$

A compression ratio of two, for example, is obtained by choosing $m = -1$. Hence, in this situation the divider is an inverter. A practical implementation using this technique is presented in Chapter 7.

5.3 AGCs in the current domain

As low-voltage low-power integrated circuits for preference operate in the current domain (Chapter 2), all signals will be represented by currents as much as possible. However, we see in the next section that the exponentially controlled amplifiers proposed here are controlled by means of a voltage. As the only integratable integrating element is a capacitor, and its input signal is a current, whereas its output signal is a voltage, the integrator will thus consist of a capacitor followed by a voltage follower. This voltage follower generates a low-impedance version of the voltage across the capacitor to prevent interaction between the capacitor and the controlled amplifier.

5.4 Controlled current amplifiers

Controlled amplifiers can be divided into two different types. First there is the class of controlled amplifiers of which the output signal shows no significant variation, but of which the input signal varies over a wide range. As an example, we mention an AGC with infinite compression; its input signal varies significantly but the output signal is almost unchanged. Second, there are controlled amplifiers of which the input signal shows no significant variation, but of which the output signal varies over a wide range. For example, in an ordinary audio amplifier; the output signal is controlled so that the sound pressure level corresponds to the need of the listener.

A well-known and commonly used controlled amplifier is the *differential pair* of which the transconductance is controlled by varying its tail current. However, as the input signal is limited to some tens of millivolts, while the output signal

can be made to vary over a wide range by simply adjusting the tail current, it falls into the category of the second type and therefore it is clearly not the best type of controlled amplifier to use in an AGC. Apart from the above disadvantages, its input signal is a voltage which makes the differentail pair less suitable for our purposes.

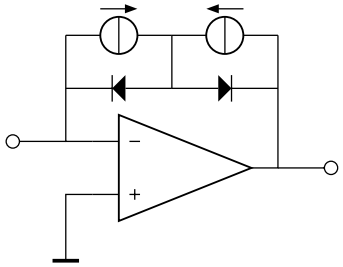

Figure 5.5: Transimpedance amplifier with two diodes in anti-series in the feedback path

Another example of a controlled amplifier is given in Figure 5.5: a transimpedance amplifier of which the feedback network consists of two diodes in anti-series. The transfer function equals the sum of the dynamic resistances of both the diodes, which can be varied by controlling the bias currents through the diodes. Although it is of the first type of controlled amplifiers, the problem with this circuit is that, apart from the bias current, also signal current flows through the diodes, thereby varying the dynamic resistances and distortion occurs. To reduce this distortion, the biasing currents must be much larger than the signal current which degrades the power efficiency. Further, its output signal is a voltage which additionally makes this type of amplifier less suitable for our purposes.

5.4.1 Four fundamental ways of controlling the gain

In the preceding chapter, we discussed a current amplifier of which the gain equals the ratio of two transconductances: the scaling current amplifier (Figure 5.6). As the transconductance of a bipolar transistor is proportional to its (DC) collector current, we can vary the gain by varying the collector current of either Q_1, I_{C,Q_1}, or Q_2, I_{C,Q_2}. We can say that the controlled amplifier is of the first type if I_{C,Q_1} is controlled (I_{C,Q_2} remains constant, thus limiting the output current swing) and to the second type if I_{C,Q_2} is controlled (I_{C,Q_1} remains constant, thus limiting the input current swing). A theoretical possibility is that both the collector currents are controlled. However, this option is believed to be of little use in practice.

Another way of controlling the ratio of the transconductances, and thus the gain of the amplifier, is by means of a controlling voltage V_C connected between the

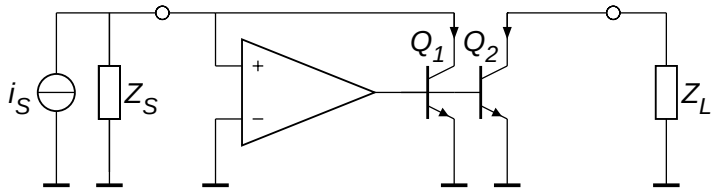

Figure 5.6: Controlling the gain of a scaling current amplifier by controlling the ratio of the collector currents of Q_1 and Q_2

emitter of Q_1 and the emitter of Q_2. We now obtain a gain A_i that is proportional to the anti-log of V_C, or

$$A_i = -g_{m,Q_2}/g_{m,Q_1} = -e^{V_C/V_T} \approx 335V_C \text{ dB}, \; V_C \text{ in volt} \tag{5.26}$$

in which V_T equals the thermal voltage kT/q, approximately 26 mV at 300 K.

The exponential relationship between the gain A_i and the control voltage V_C of the voltage-controlled amplifiers enables us to control the gain over a wide range.

As the controlled current amplifiers are either current- or voltage-controlled and are of either the first or second type, we can distinguish four different kinds:

- a current-controlled type 1 scaling current amplifier,
- a current-controlled type 2 scaling current amplifier,
- a voltage-controlled type 1 scaling current amplifier, and
- a voltage-controlled type 2 scaling current amplifier.

These four are the subject of the next four subsections. In the preceding chapter, we mentioned that unless there is the possibility of on-chip filtering, the biasing of a circuit is by preference done by setting the common-mode quantities. In order to do so, the signal path has to be symmetrical. As current- or voltage-controlled and type 1 or type 2 has nothing to do with the signal behavior of the amplifier, we assume that the design of the symmetrical signal path has been completed in an earlier stage and start our considerations from here.

It also is tacitly assumed that the source is floating and the load is tied to a certain reference level (e.g. a base-emitter voltage of the following circuit). In other situations, similar solutions can be found by using the biasing theory set out in the preceding chapter.

5.4.2 The current-controlled type 1 symmetrical scaling current amplifier

The general biasing solution for a current-controlled type 1 symmetrical scaling current amplifier is depicted in Figure 5.7. The transfer function is controlled by means of two current sources I_C. In order to make the DC collector currents of the output transistors equal to I, a common-mode output is generated by two extra output transistors. The sum of their collector currents is compared with $2I$, thus producing an error signal. The error signal is amplified by the op amp and fed back to both emitters of the input transistors, thereby setting the correct emitter current. As the absolute value of the loop gain of the common-mode loop is much larger than one, the error signal is nullified and the output transistors are biased correctly.

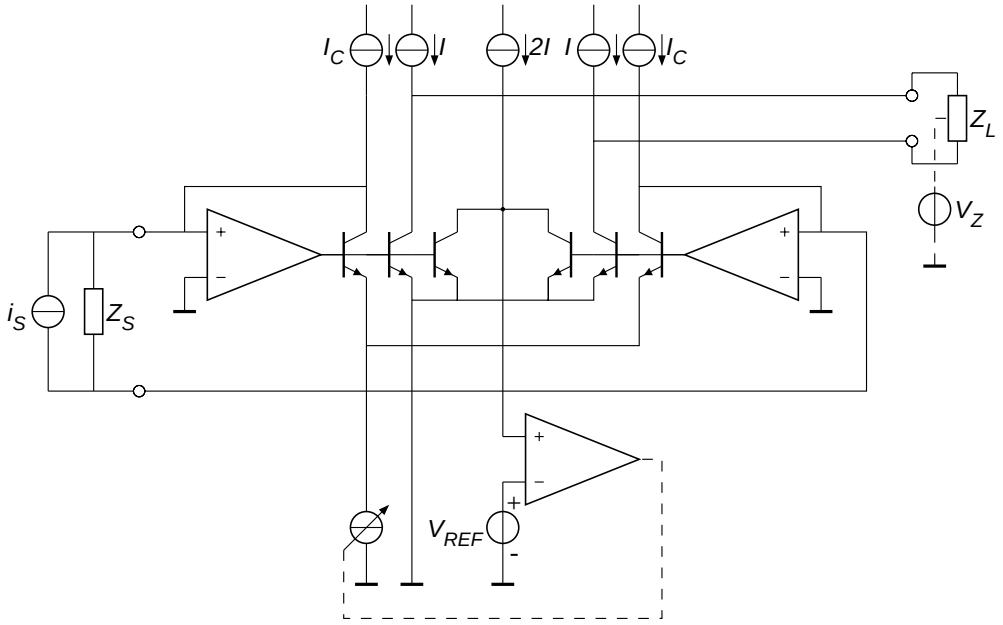

Figure 5.7: Current-controlled type 1 symmetrical scaling current amplifier

5.4.3 The current-controlled type 2 symmetrical scaling current amplifier

This situation does not differ much from the preceding one. Only now the transfer function is controlled by varying the current through the *output transistors*. The general solution for a current-controlled type 2 symmetrical scaling current amplifier is depicted in Figure 5.8. In order to set the output collector currents, again a common-mode output is generated by two extra transistors, their collectors tied

together. The common-mode current is compared with $2I_C$, producing an error signal. The error signal is amplified by the op amp and fed back to both emitters of the *output transistors*, thereby setting the correct emitter current. As the absolute value of the loop gain of the common-mode loop is much larger than one, the error signal is nullified and the output transistors are biased correctly.

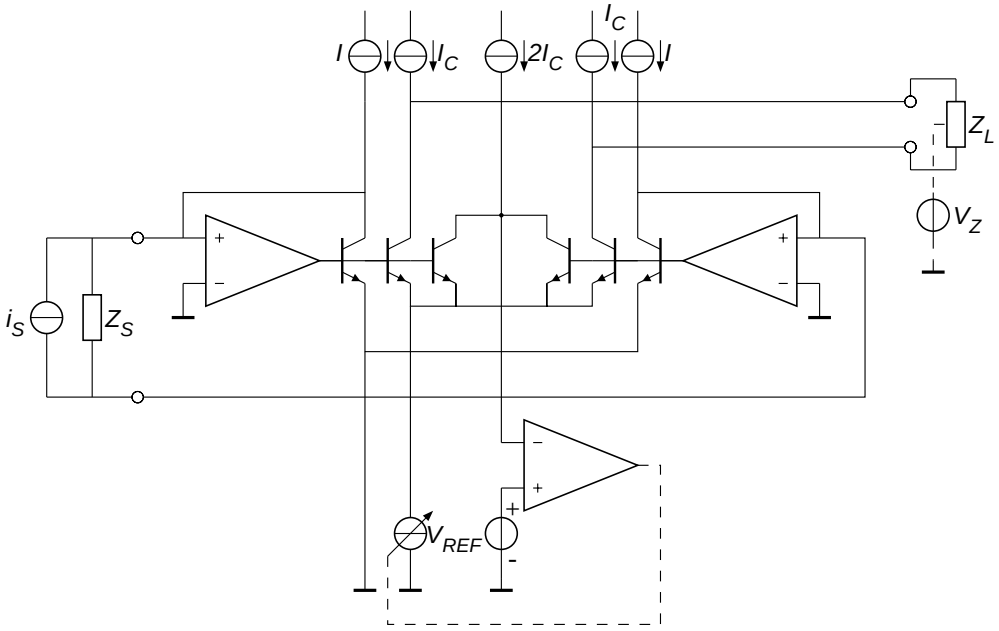

Figure 5.8: Current-controlled type 2 symmetrical scaling current amplifier

5.4.4 The voltage-controlled type 1 symmetrical scaling current amplifier

The transfer function of this type of amplifier is controlled by the control voltage V_C (see Figure 5.9). Again a common-mode replica of the common-mode collector currents through the output transistors is compared with $2I$, producing an error signal. The error signal is amplified by the op amp and controls the collector current of the input stages.

An example of the voltage-controlled type 1 symmetrical scaling current amplifier is described in [2]. This circuit is part of a hearing instrument and serves to attenuate the signal coming from the preamplifier [3] — the design example in the preceding chapter — that can vary between 40 nA and 10 μA (peak value) and drive a highpass filter [4] at maximal 25 nA.

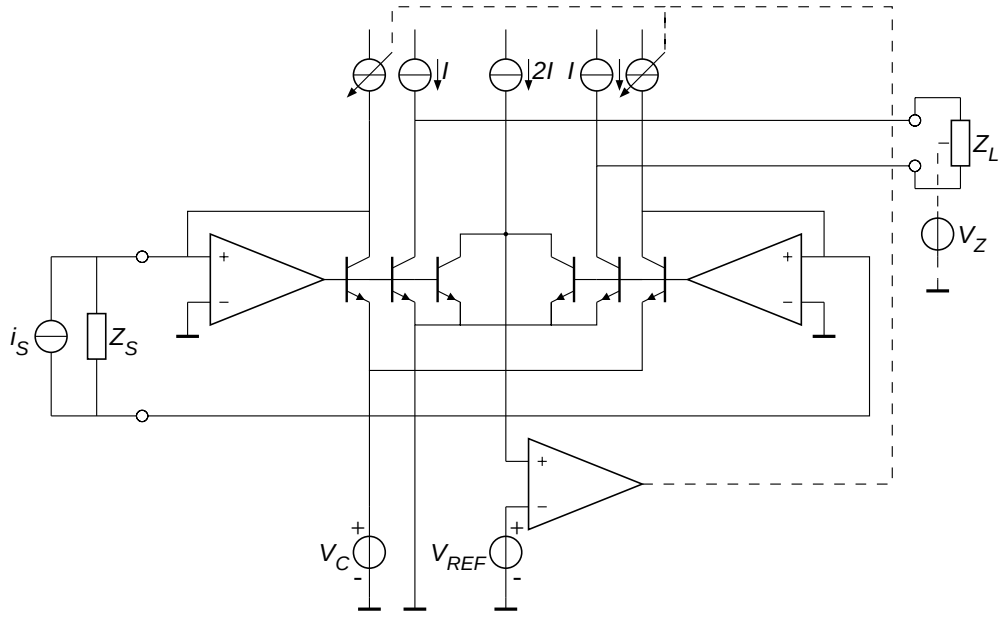

Figure 5.9: Voltage-controlled type 1 symmetrical scaling current amplifier

5.4.5 The voltage-controlled type 2 symmetrical scaling current amplifier

Finally, the voltage-controlled type 2 symmetrical scaling current amplifier, see Figure 5.10. V_C controls the gain. The common-mode loop controls the collector currents of the output transistors (including the common-mode output transistors) in such a way that they match the collector currents of the input stages.

Two examples of the voltage-controlled type 2 symmetrical scaling current amplifier can be found in [5] and [6]. The first circuit (though not strictly symmetrical) has been designed for the same hearing instrument and loads a highpass filter [4] at maximal 25 nA and drives the power amplifier. Its gain can be controlled from 0 to 60 dB. The second circuit, a controllable preamplifier, was originally designed for a different hearing instrument using the conventional electret microphone with built-in JFET [7]. It adapts input signals varying between 120 nA and 30 μA (peak value) to the maximal filter input level of 1 μA.

5.5 Comparators

The comparator is the circuit that compares the output current of the controlled amplifier with the reference level I_K by means of a highly non-linear input-output relation. Thus the comparator can be viewed as a one-bit A/D converter. Its response to a signal level higher than the reference level is a fixed output level,

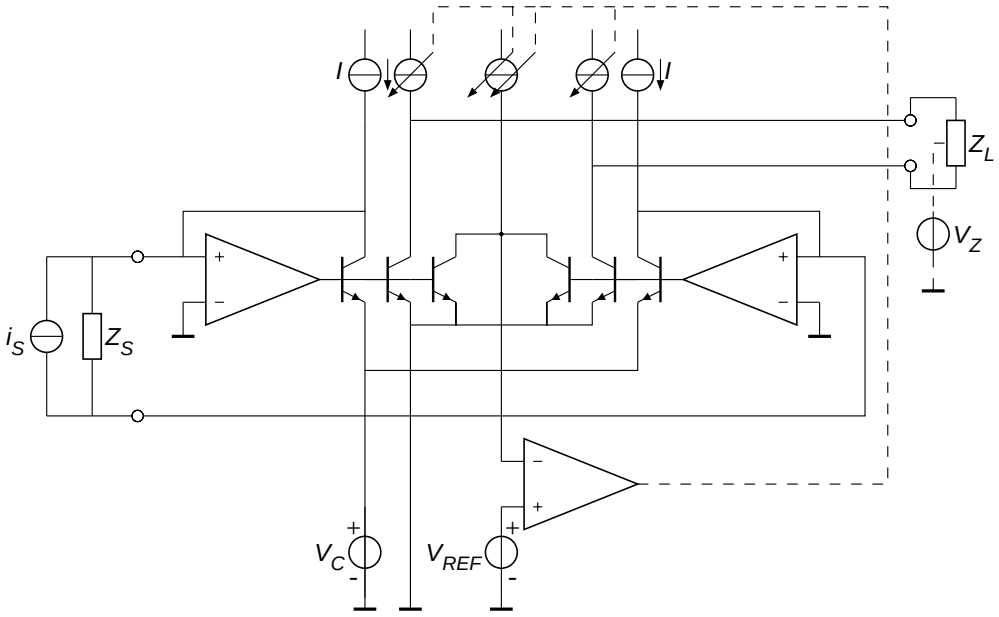

Figure 5.10: Voltage-controlled type 2 symmetrical scaling current amplifier

representing the '0' or the '1' state. Its response to a signal lower than the reference level is another fixed output level, representing the complementary state. The gain when the input equals the reference level ideally is infinite. However, it is no use making the gain much larger than the ratio of the desired output swing and the smallest input swing. In practice, there is also some common-mode-to-differential-mode conversion in the controlled amplifier, so that for large values of the comparator gain the common-mode control loop might become instable.

For a comparator which has a current-current input-output relation we can choose either a cascade connection of a non-linear one-port and a linear two-port, or an amplifier with a saturating input-output relation.

5.5.1 Cascade of a non-linear one-port and a linear two-port

Examples of (bipolar) non-linear one-ports are diodes and pinch resistors. An example of a (current) comparator consisting of a cascade of a non-linear one-port and a linear two-port is given in Figure 5.11. Both the output current of the controlled amplifier and the reference current can be supplied, with opposite signs, to the same input, and thus subtracted from eachother. If the result is positive, diode D_1 will conduct. The resulting anode-cathode voltage will vary only slightly with respect to the current and thus represent one state of the comparator. If the result is negative, diode D_2 will conduct, resulting in a complementary voltage, representing the complementary state. The resistor R transforms the voltage into

a current that is sensed by the (low-impedance input of the) next circuit. Although relatively simple, this comparator is supposed to be of less practical importance in low-power integrated circuits. If, for example, the output current of the comparator is to be as small as 25 nA, and the diode voltages are about .5 V, R must equal 20 MΩ. This value is not easily realized in an integrated circuit.

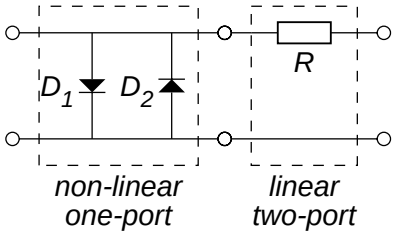

Figure 5.11: Example of a comparator consisting of a cascade connection of a non-linear one-port and a linear two-port

5.5.2 Amplifiers with a saturated input-output relation

It is not difficult to design an amplifier with a saturated input-output relation. Every practical amplifier will come into saturation if its input signal exceeds a certain level. Three examples are given in Figure 5.12. During saturation, often one or more transistors will be pinched off or be in saturation. In negative-feedback amplifiers, this might introduce extra dominant poles in the feedback loop, giving rise to instability, or lead to latch-up (see e.g. [8]). The designer must be aware of this and try to avoid both instabily and latch up under all circumstances. Often good results can be obtained from simple circuitry.

5.6 Voltage followers

The last stage in the design of low-voltage low-power automatic gain controls is the design of the voltage follower. The voltage follower forms a buffer between the capacitance C and the controlled amplifier. Since the input current of a field effect transistor (JFET or MOST) is far below the other currents that charge and discharge the integrating capacitor, these devices are very well suited for this task. When using bipolar transistors this can only be achieved by using negative-feedback techniques. The basic voltage-follower configuration and three possible implementations, with either one, two or three transistors, are given in Figure 5.13. Although the output voltage differs a base-emitter voltage from the input voltage, this is no problem here; the voltage follower is part of a loop; the effect of the base-emitter voltage will be nullified.

An example of a three-transistor voltage follower can be found in [2].

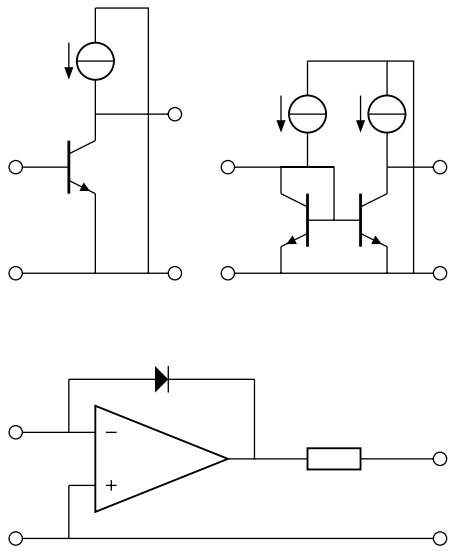

Figure 5.12: Three possible implementations of amplifiers with a saturated input-output relation

5.7 An example: an automatic gain control for hearing instruments

In this section, the design and realization of a low-voltage low-power fully-integratable automatic gain control for hearing instruments is presented.

Apart from pitch, loudness and timbre, information in the world of sound is characterized also by more or less sudden temporary changes. For someone with hearing impairment, these variations do not fit into his or her dynamic range and, therefore, there is either the lack of certain parts of the information or the pain limit is frequently exceeded. In this situation, an automatic gain control can offer certain improvement of the (speech) intelligibility. It must be noted that AGCs are only technically approximate solutions to the dynamic range problems of the hearing impaired. This also explains why optimal, generally applicable values for the AGC characteristics are not easily found.

In practice, two kinds of AGCs are found [9]: an AGC-I and an AGC-O. The AGC-I obtains its control signal from a signal in front of the volume control. Thus, the control action depends on the sound pressure level at the input of the hearing instrument. The control signal of the AGC-O is derived from the signal behind the volume control. The control action then depends on the sound pressure level that is offered to the ear.

The AGCs differ from each other insofar as that the control range of the AGC-I is always larger (for example 60 dB) while for the AGC-O often 20 dB is enough.

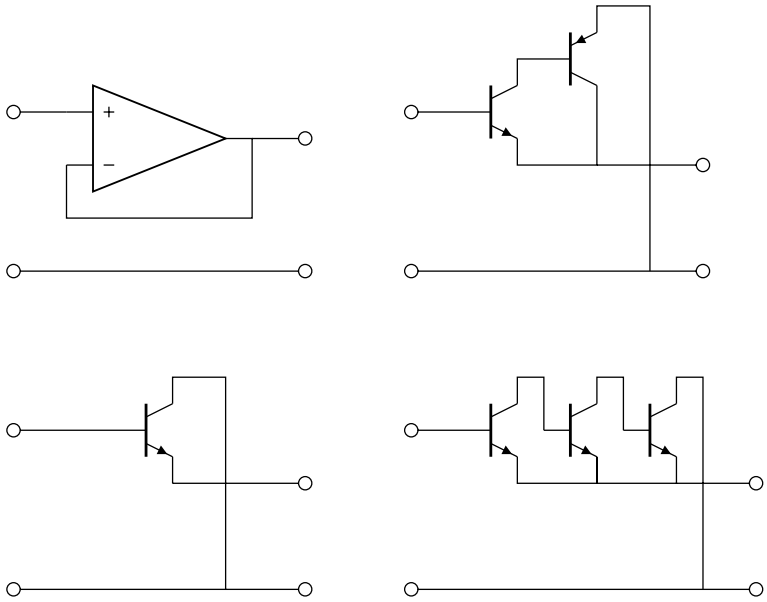

Figure 5.13: Basic voltage-follower configuration and three possible implementations

The compression ratio often is also different: e.g. between 1.5 and 10 for the AGC-I and infinite for the AGC-O. An AGC-I design is discussed in Chapter 7.

The circuit that is described here is an AGC-O with an infinite compression ratio, of which the block diagram is shown in Figure 5.1. Its *current-domain* realization is given in Figure 5.14. Apart from the integrator signal E_{int} all signals are represented by currents. The AGC amplifier obtains its input signal from a controllable attenuator [2] and drives a highpass filter [4]. The nominal signal level at both input and output amounts to 25 nA (peak value). The purpose of the AGC is to attenuate larger input signals to avoid clipping and hearing damage. The attack time and the release time must be < 5 ms and 50 ms, respectively.

To here the design has been discussed at system level. We now take a closer look at the design of its components: the controlled amplifier, the comparator (including the switch and current source I_{att}) and the voltage follower.

5.7.1 Design of the controlled amplifier

From the considerations presented in Section 5.4, it should be clear that the best choice of amplifier is a type 1 symmetrical scaling current amplifier. From the two variants, we choose the voltage-controlled one as this gives a control action in dBs, which is perceptibly the most comfortable. A possible implementation of a voltage-controlled symmetrical scaling current amplifier is given in Figure 5.15. As the absolute value of the (differential) loop gain is always larger than

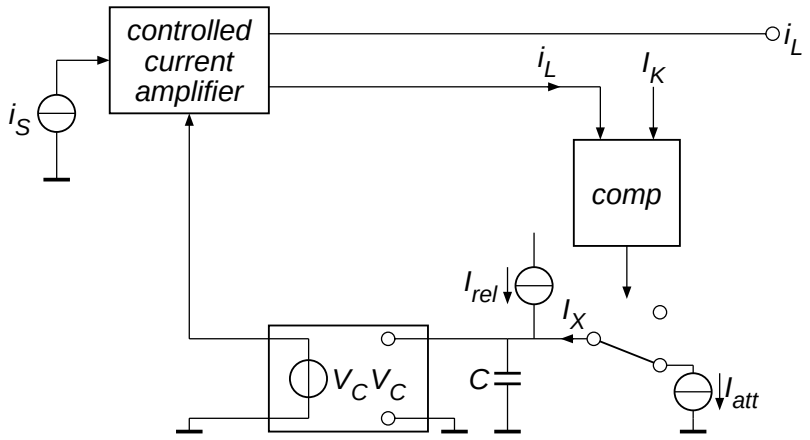

Figure 5.14: Block diagram of an AGC-O operating in the current domain

$B_F/4$, there is no need for additional loop gain; the op amps thus can be replaced by short circuits. In line with the preceding chapter, we can call this a voltage-controlled type 1 symmetrical current mirror. Transistors Q_{1a} and Q_{1b} are the input transistors. Q_{2a} and Q_{2b} deliver the output current i_L. Q'_{2a} and Q'_{2b} are the output transistors for i'_L. The common-mode loop is formed by Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a} and Q_{6b}. The collector currents of Q_{3a} and Q_{3b}, which equal the collector currents of Q_{2a} and Q_{2b}, are added and compared with a current $2I$. The error signal controls via Q_4, Q_5, Q_{6a} and Q_{6b} the collector currents of Q_{1a} and Q_{1b}. Because the gain in this loop, the common-mode loop gain, equals the current gain factor B_F of Q_{6a} and Q_{6b}, which is much larger than one, the error signal is nullified and the symmetrical current mirror is biased correctly. Q_{sa} and Q_{sb} limit the maximum gain of the amplifier to one. Q_{da} and Q_{db} shunt the input and prevent the amplifier from saturating.

5.7.2 Design of the comparator

The comparator is the subcircuit that decides whether the output current i'_L of the controlled amplifier is larger or smaller than the reference level I_K. For this purpose we can again use a symmetrical current mirror now acting as an amplifier with a saturated input-output relation. Its implementation is given in Figure 5.16. Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a}, Q_{6b} and Q_{6c} form the common-mode biasing circuitry. In this case, the common-mode loop gain is kept sufficiently small (i.e. equals 2) to prevent instability in the comparator. The output current I_X therefore switches between 0 and $\frac{2}{3}I$. The two diode-connected transistors Q_{da} and Q_{db} prevent the input transistors Q_{1a} and Q_{2a} from saturating; the comparator switches faster.

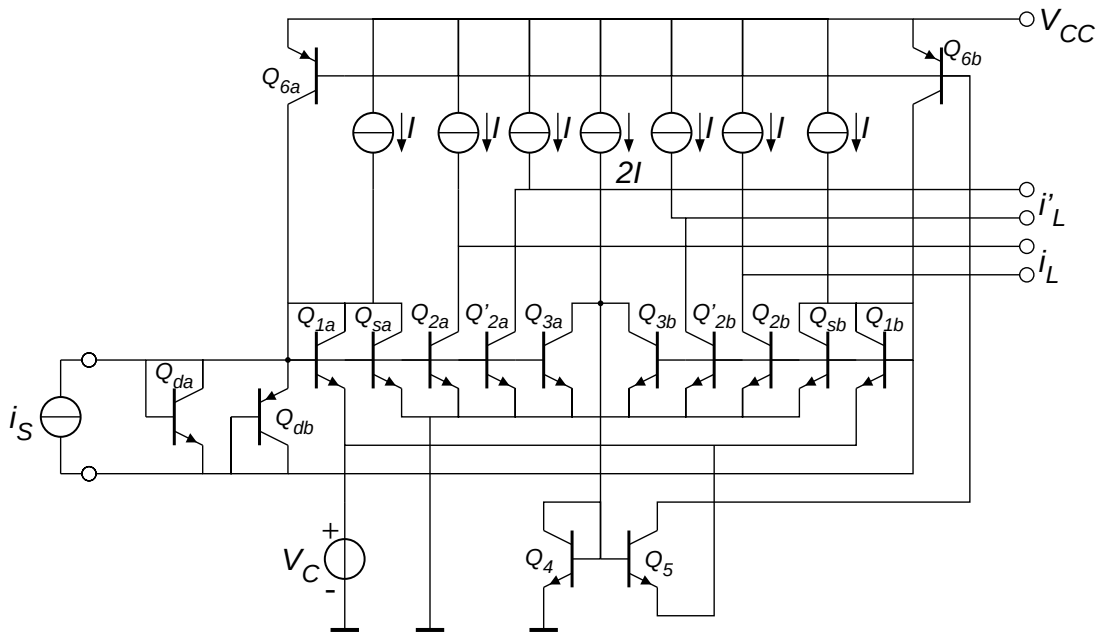

Figure 5.15: The voltage-controlled type 1 symmetrical current mirror

5.7.3 Design of the voltage follower

The chosen voltage follower is depicted in Figure 5.17. The input (offset) current equals $I_V / B_{\mathrm{F,PNP}} B_{\mathrm{F,NPN}}$ and must lie well below the release current I_{rel}. Its influence will then be small.

5.7.4 Overall design

Now that all the different parts of the AGC have been designed at circuit level, they can be linked together and we take a look at the numerical values and the remaining bias circuitry.

As the output signal is to be maximally 25 nA (peak value), the reference current I_K equals 25 nA. The current sources I as depicted in Figure 5.15 have been chosen well above this 25 nA and equal 100 nA. The values of I_{att} and I_{rel} can be derived from the attack time and the release time. Some calculation yields

$$I_{\mathrm{att}} = \frac{5.2 V_T C}{t_{\mathrm{att}}} + I_{\mathrm{rel}} \tag{5.27}$$

and

$$I_{\mathrm{rel}} = \frac{2.6 V_T C}{t_{\mathrm{rel}}} \tag{5.28}$$

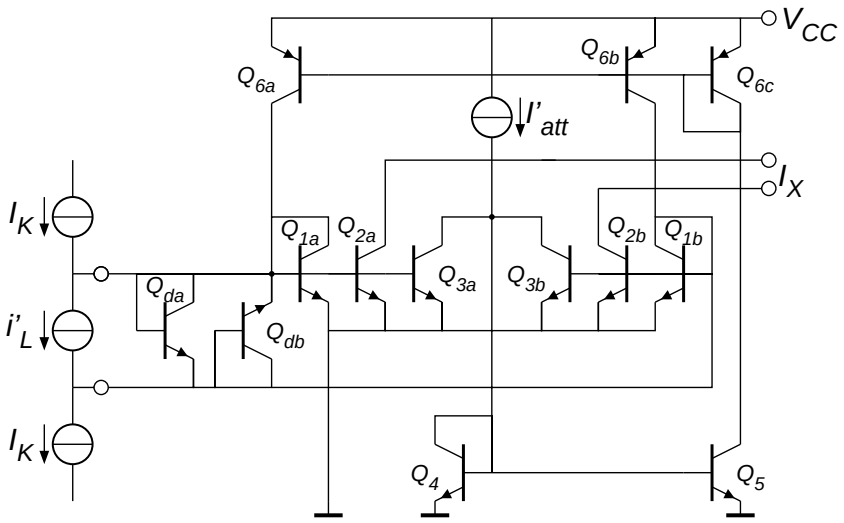

Figure 5.16: A type 1 symmetrical current mirror used as a comparator. The common-mode loop gain equals 2 to prevent instability

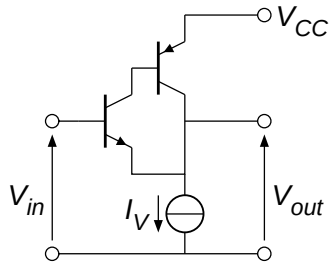

Figure 5.17: The two-transistor voltage follower

For $I'_{\rm att}$ (Figure 5.16) it follows

$$I'_{\rm att} = \frac{3}{2} I_{\rm att} = \frac{7.8 V_T C}{t_{\rm att}} + \frac{3}{2} I_{\rm rel} \tag{5.29}$$

With $t_{\rm att}$, $t_{\rm rel}$ and C equal to 4 ms, 50 ms and 400 pF, respectively, this results in 20 nA and 540 pA for $I'_{\rm att}$ and $I_{\rm rel}$. The current source I_V (Figure 5.17) supplies the current of the PNP transistor in the voltage follower and is chosen to be equal to 1 μA. All these currents can be derived by means of current mirrors with multiple outputs and convenient scaling factors. The scaling factor can be obtained by choosing either a proper emitter area ratio or by means of resistors. The latter solution yields either a *Widlar mirror* or a *gm-compensated mirror* [10].

The total circuit diagram of the AGC is depicted in Figure 5.18. Two voltage sources (V_1 and V_2) have been added to prevent the current sources I_V and I_K from saturating. V_1 has been realized by means of a saturating NPN transistor and a

resistor. V_2 contains two saturating PNP transistors in series. Thus, their voltages are well above the saturation voltages of I_V and I_K. To avoid (common-mode) instability, an integratable capacitance C_{comp} can be added.

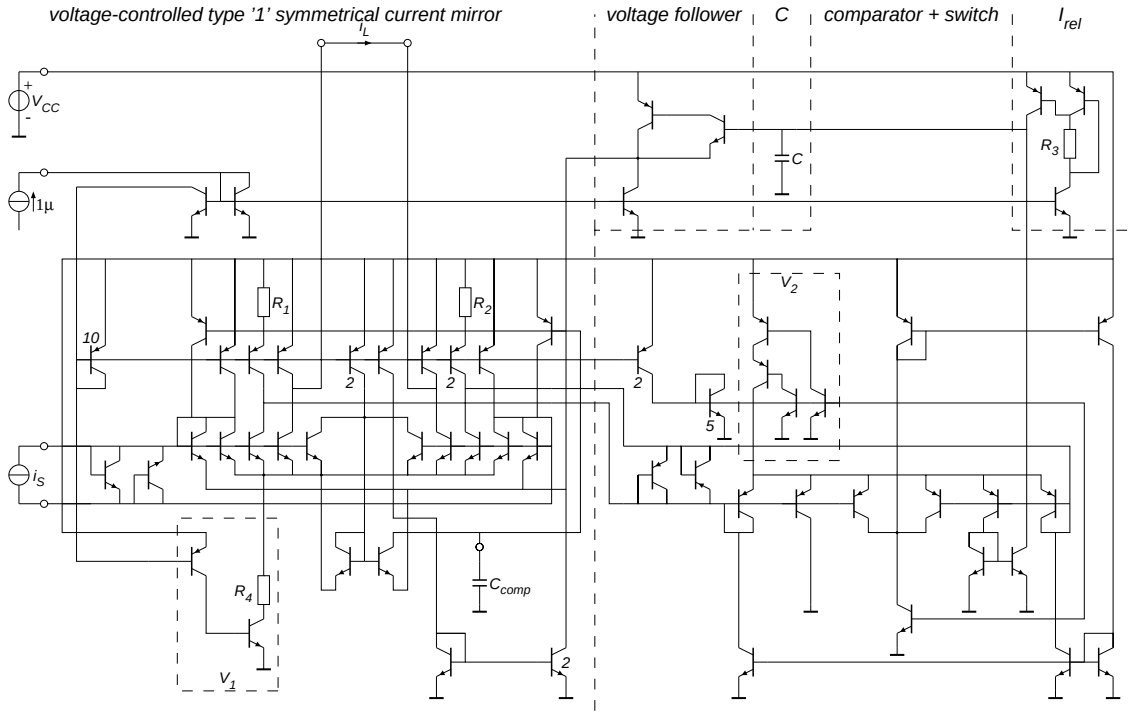

Figure 5.18: The total automatic gain control. Instability may be counteracted by C_{comp}

5.7.5 Experiment results

The active circuitry of the circuit shown in Figure 5.18 has been integrated in the DIMES01 process [11], fabricated at the Delft Institute of Microelectronics and Submicron Technology. Figure 5.19 shows a photomicrograph of the chip. Experiments proved the correct operation of the AGC. Table 1 gives the measurement results. No instability occurred. The relatively large value of the release time is caused by the base current of the first stage of the voltage follower. However, this did not pose a problem in our application.

Table 1: Measurement results of the AGC

Parameter	Value	Unit
Compression range	38	dB
Attack time, i_s=1 μA_p, 1 kHz	4.2	ms
Release time, i_s=10 nA_p, 1 kHz	58	ms
Dynamic Range, G=1, B=10 kHz	62	dB
Bandwidth	>100	kHz
Min. supply voltage	1	V
Supply current, G=1	4	μA

Figure 5.19: Photograph of the integrated circuit

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Chapter 6

Filters

In my life, I have put the descriptions of sticks and stones
and billiard balls and galaxies in one box [...]
and have left them alone.
In the other box, I put living things:
crabs, people, problems of beauty, and problems of difference.

Gregory Bateson: Mind and nature

6.1 Introduction

In Chapter 4 it was mentioned that amplification is an indispensable function when it comes to the design of electronic systems. Another fundamental operation is the separation of desired signals from other signals and noise by making use of differences in their energy-frequency spectra. The electronic circuits that perform this separation action are filters. In practice, a piece of electronic apparatus which does not contain at least one rudimentary filter can hardly be found .

A filter has passbands where the frequency components are transmitted to the output and stopbands where they are rejected. In practice, this ideal performance is not achieved; the unwanted components do produce some signal at the output, though very much reduced with respect to the desired components; the desired components, instead of being transferred as though by a direct connection, are slightly attenuated.

Traditionally, filters operated in the continuous-time domain and have been designed as resistively terminated lossless LC filters [1, 2]. An example of a second-order lowpass LC filter is shown in Figure 6.1.

A problem arises when we wish to realize the filter on chip, which implies giving up the use of inductors. Filter transfer functions that can be realized with capacitive and resisitive elements only have real poles in the left half of the complex

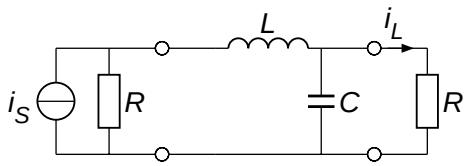

Figure 6.1: Example of a second-order lowpass LC filter

Laplace plane, while an amplitude response with steep slopes calls for a tranfer function with complex poles. These are only realizable if active circuits are added. As an example we mention the well-known Sallen & Key filter [3], of which a second-order lowpass version is shown in Figure 6.2.

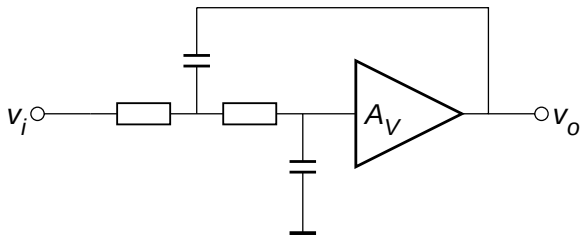

Figure 6.2: A second-order Sallen & Key lowpass filter

With the introduction of active circuits in filters, two fundamental problems were introduced. First, unlike passive reactances, active elements produce noise and distortion. For this reason, active filters are bound to exhibit a limited dynamic range. Second, unlike passive reactances, active elements dissipate energy. Thus power has to be supplied.

The integration of capacitors, resistors and active stages on chip also introduces another problem: the realization of large time constants. A time constant is the product of a capacitance and a resistance, and for large time constants large capacitors and/or large resistors are required. Both consume large amounts of chip area. For this problem two different solutions have been found.

The first solution for realizing large time constants on a chip is the simulation of a resistor by a switched capacitor [4, 5]. If a capacitance of value C_R is periodically switched at clock frequency f_S, a resistor with value $1/f_S C_R$ is simulated. Together with an integrating capacitor C_I, a time constant $C_I/f_S C_R$ can be obtained. This time constant depends only on the clock frequency and a ratio of capacitances and can therefore be very accurate. An example of a second-order switched-capacitor lowpass Sallen & Key filter is given in Figure 6.3.

Large time constants can thus be realized by choosing f_S to be small, however, theoretically at least twice, practically several times more, the signal bandwidth, and choosing the ratio of capacitances C_I/C_R to be large.

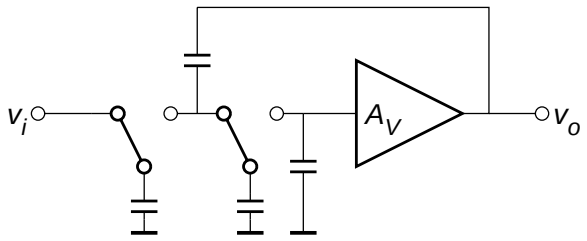

Figure 6.3: Example of a second-order switched-capacitor lowpass Sallen & Key filter

Another solution is obtained by realizing the filter as a network of integrators or differentiators. The inductances and capacitances in a passive LC filter can be considered as elements that perform mathematical operations, like integrating and differentiating. These operations on the voltages and/or currents can be performed by active circuits. As an example we mention the well-known leapfrog filter [6]. Figure 6.4 shows a second-order lowpass leapfrog filter.

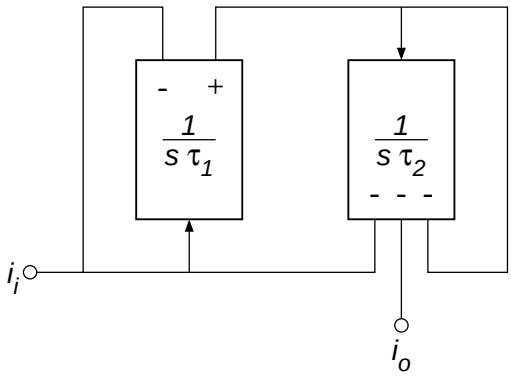

Figure 6.4: A second-order lowpass leapfrog filter

The latter continuous-time filtering is the least accurate of these two techniques with respect to its cutoff frequency. However, in contrast with switched-capacitor filters the circuits are much simpler, no additional anti-aliasing filtering is necessary and no clock feedthrough occurs. The dynamic range is limited, but generally higher than for switched-capacitor filters [7]. Another point is that as only MOS technology provides excellent switches, switched-capacitor filters can only be realized in MOS technology [2]. Unfortunately, low-threshold CMOS IC processes were not yet well specified for analog design at the start of the research. Further, continuous-time filters are the only ones able to operate at frequencies up to the transit frequency f_T of the active devices. Therefore, continuous-time filters are the best solution, and sometimes the only solution, to realize on-chip low-power filter functions (Chapter 3).

An n-th-order filter realizes an n-th-order linear differential equation. On a

chip, there is only one type of component available that can be used to realize a differential equation, namely the capacitor. The capacitor by itself realizes a first-order linear differential equation, so it can be considered as an integrating or as a differentiating component. An n-th-order filter can always be constructed by means of n integrators or differentiators. Although there is no preference for either a differentiator or an integrator from a network-theoretical point of view, in practice, in most cases, using a capacitor as a differentiator gives rise to high-frequency problems. Therefore a capacitor in a filter is almost always used as an integrator.

When designing an integratable continuous-time analog filter, often the key problem is its dynamic range, which is defined as the ratio of the largest and the smallest signal level that the filter can handle. The largest signal level is determined by clipping or distortion, the smallest by noise. In critical applications, one should optimize the dynamic range of the filter. Optimization can take place at different levels: the filter network and the building blocks, i.e. the integrators, that constitute the filter can be taken into consideration. If one wants to design high-dynamic-range filters one should therefore be able to design high-dynamic-range integrators as filter components [7].

Apart from using high-dynamic-range integrators, another way to improve the dynamic range of a filter is to make use of scaling. The purpose of scaling is to make the voltage levels inside all the integrators of the filter equal, so that there is not a single integrator that limits the maximal input signal level, while the others may still be able to handle larger signals. In a filter with an optimal dynamic range all the internal voltage levels are equal [8].

6.2 Current integrators

Traditionally, integrators are implemented as voltage integrators. With a capacitor as the integrating element, of which the input signal is a current, whereas its output signal is a voltage, a voltage integrator may consist of a cascade of a resistive voltage-to-current convertor (a transconductor) followed by an integrating current-to-voltage convertor. By interchanging the order of cascading the convertors, we obtain a current integrator.

If we now carry out scaling on the nodal variables in the signal flow graph of a filter, in general, each node will require scaling by a different factor. In low-voltage low-power circuits the scaling of currents is done much more easily than the scaling of voltages (Chapter 2).

Further, if the filter is part of a larger circuit, of which the information-carrying quantity is a current (Chapter 2), the use of voltage integrators requires two extra convertors: a current-to-voltage convertor that drives the filter and a voltage-to-current convertor that loads the filter. These convertors add noise and distortion,

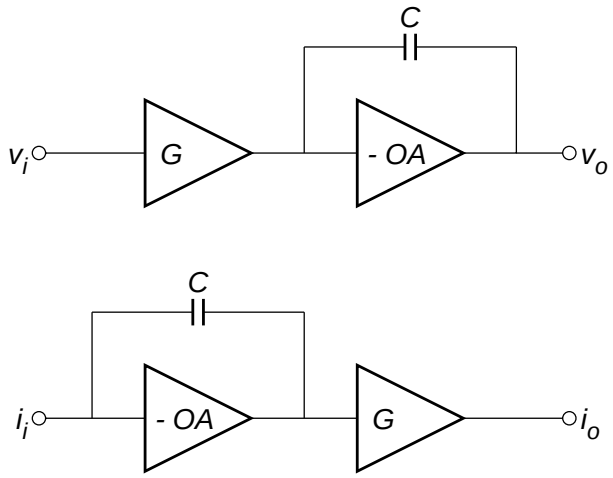

Figure 6.5: Example of a voltage integrator (a) and a current integrator (b)

consume battery power and require two extra resistors. A filter consisting of current integrators, however, has a current as the information-carrying quantity at both input and output. Because there is no need for two extra convertors it obviously is the best solution.

6.3 Low-voltage low-power current integrators

In many applications, one should be able to electronically vary the cutoff frequency of the filter. This requires the ability to control the transfer function of the integrators. There are two ways to realize this, namely by controlling the value of the capacitor or by controlling the value of the transconductor. A controllable capacitance can be realized by means of a junction capacitance with a controllable voltage source. However, with this option a control range of, e.g., a factor ten, is hard to achieve, if not impossible. We therefore have to control the transconductor part.

In [7] it is shown that to maximize the dynamic range of an integrator, the maximal voltage over the capacitance in the integrator must be maximized. This voltage, in turn, is limited by the supply voltage.

One stage that can be used to achieve maximum voltage swing over the capacitance is a current-mode equivalent of the well-known MOSFET-C integrator [9] (Figure 6.6). The MOS transistor realizes an admittance function which can be controlled by the gate voltage of the transistor. In bipolar processes, as an alternative, pinch resistors can be used. However, whether using MOSFETs or pinch resistors, it remains difficult to control the cutoff frequency over a wide frequency range.

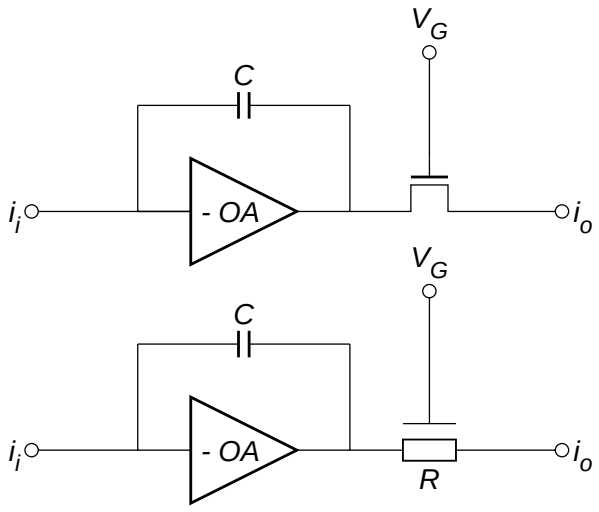

Figure 6.6: Example of a MOSFET-C current integrator and a Pinched-R–C current integrator

For this reason, most of the published designs of bipolar controllable filters are based on the transconductor-C (also known as gm-C) principle [8]. To obtain a wide control range of the integrator transfer function, an ordinary emitter-coupled pair can operate as a variable transconductor. Unfortunately, a conventional emitter-coupled pair has a linear input range that is limited to some tens of millivolts and cannot fully exploit the limited dynamic range. To overcome this problem, several linearization techniques, based on a plurality of emitter-coupled pairs [10, 11] were developed in the past, see, for example, Figure 6.7. Although with this technique a linear input swing of about 100 mV can be achieved, usually the price paid is a large complexity, a large chip area or a large current consumption.

A better solution is to use negative feedback. Negative feedback allows us to exchange the large gain provided by the non-linear transistors for the linearity of a passive feedback network. To achieve a variable transconductance factor we have two possibilities: we can either design a transconductance amplifier with a fixed transconductance factor followed by a controllable current amplifier [12, 13, 14], or we can provide the transconductance amplifier with a scaled indirect output, as described in Chapter 4. Both solutions are based on the translinear principle [15, 16] and are very much alike. The second, however, is less complex and is superior with respect to its noise behavior.

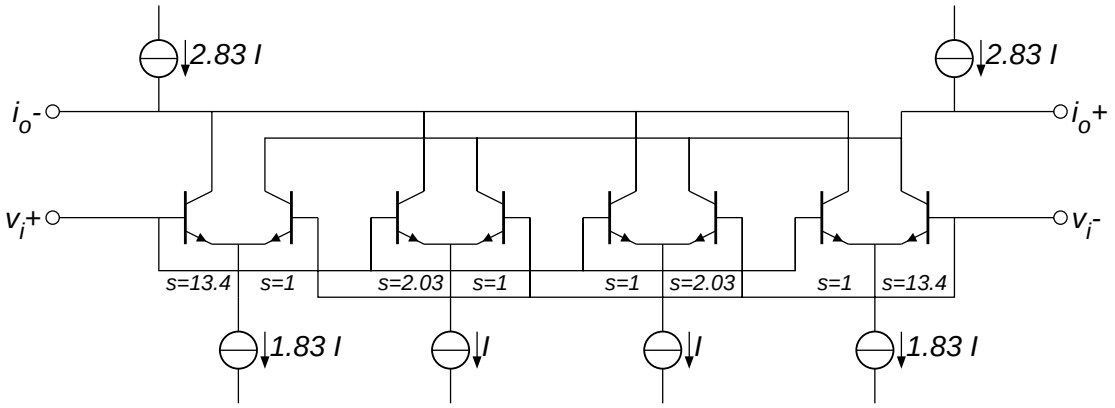

Figure 6.7: A transconductor with a 100 mV input swing using four emitter-coupled pairs

6.4 A capacitance-transconductance amplifier

An integrator operating in the current domain using a transconductance amplifier with an indirect output is shown in Figure 6.8. The capacitance C transforms the input current i_i into a voltage $v_i = i_i/j2\pi fC$. This voltage, in turn, is transformed by resistor R, the op amp and Q_1 into a current $i'_o = v_i/R = i_i/j2\pi fRC$. Q_2 provides the indirect output. When the bias current through Q_2 equals n times the bias current through Q_1 (and when the Early effect is negligible) we find for the transfer function H_I of the integrator

$$H_I = \frac{n}{j2\pi fRC} \tag{6.1}$$

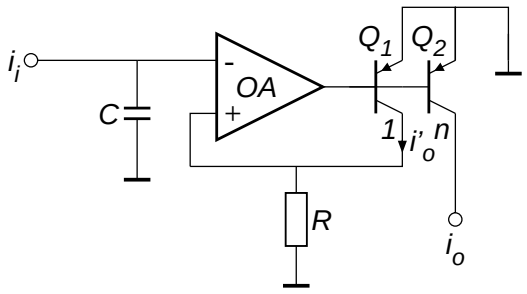

Figure 6.8: An integrator using a transconductance amplifier with an indirect output

A realization of this integrator is obtained when the op amp is replaced by a single CE stage. This is shown in Figure 6.9.

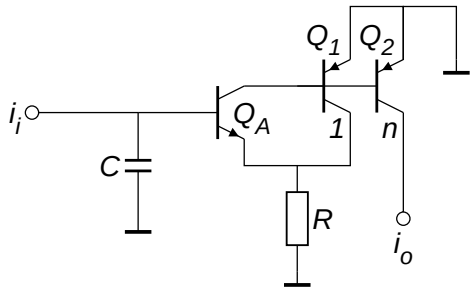

Figure 6.9: A possible integrator implementation

To calculate the amount of noise the capacitance-transconductance amplifier contributes to its output current, we shift the dominating noise sources (i.e., the noise sources of Q_A, v_n and i_n (Chapter 3), and the noise source of resistor R, i_R) to the output, and we find an expression for the equivalent noise current power density spectrum at the output, $S(i_{n,\mathrm{eq}})$:

$$S(i_{n,\mathrm{eq}}) = S(v_n)\frac{n^2}{R^2} + S(i_n)n^2\left(1+\frac{1}{j2\pi fRC}\right)^2 + S(i_R)n^2 \tag{6.2}$$

With $S(v_n) = 2kT/g_m$, $S(i_n) = 2kTg_m/B_F$ and $S(i_R) = 4kT/R$ this can be rewritten as

$$S(i_{n,\mathrm{eq}}) = \frac{2kTn^2}{g_m R^2} + \frac{2kTg_m n^2}{B_F}\left(1+\frac{1}{j2\pi fRC}\right)^2 + \frac{4kTn^2}{R} \tag{6.3}$$

When the maximal voltage swing across the capacitor is $v_{C,\max}$ and when we integrate the above expression over the total frequency range (from f_1 to f_2) we can find an expression for the dynamic range ($D.R.$) of the integrator for sinusoidal input signals

$$D.R. = \frac{v_{C,\max}^2}{16kT(f_2-f_1)\left(\frac{1}{g_m}+\frac{g_m}{B_F}\left(R^2+\frac{1}{4\pi^2 f_1 f_2 C^2}\right)+2R\right)} \tag{6.4}$$

Obviously, C has to be chosen to be as large as possible. In addition, this expression can be maximized by varying g_m. Because g_m is proportional to the collector current of Q_A, I_{C,Q_A}, it is possible to maximize the dynamic range by varying I_{C,Q_A}. For this optimum value, $I_{C,Q_A,\mathrm{opt}}$, we find

$$I_{C,Q_A,\mathrm{opt}} = \frac{V_T}{\sqrt{R^2/B_F + 1/4\pi^2 B_F C^2 f_1 f_2}} \tag{6.5}$$

and the dynamic range becomes with this optimum

$$D.R._{\text{opt}} = \frac{v_{C,\max}^2}{32kT(f_2 - f_1)\left(\frac{V_T}{I_{C,Q_A,\text{opt}}} + R\right)} \tag{6.6}$$

In line with the design procedure laid out in Chapter 4, the value of resistor R is to be chosen in such a way that the dynamic range is larger than the minimum acceptable dynamic range of the integrator [7], the scaling factor n is larger than one (efficiency!), if possible, and resistor R is integratable.

Another conclusion that can be drawn from (6.4), is that to obtain a large dynamic range, also the voltage swing across the capacitor should be as large as possible. This cannot be achieved with the circuit shown in Figure 6.9. Here, the voltage swing is limited mainly by the base-emitter voltage of Q_A. For example, if the supply voltage is as low as 1 V, the base-emitter voltage amounts to 650 mV and 150 mV is reserved to avoid saturation of the driving circuit, there is only 200 mV of swing possible. One way to enlarge the voltage swing is to make use of another op amp implementation, with rail-to-rail input capability [17]. However, a major disadvantage of this option is that the circuit complexity is enlarged considerably — in fact two complementary input stages and various level shifts are needed —, which entails a larger noise contribution and a larger power consumption.

6.5 A capacitance-transconductance amplifier with enlarged voltage swing

Another possibility of obtaining a wider voltage swing across the capacitor, is sensing the voltage at the input of the integrator, amplifying this voltage and feeding the result to the other capacitor terminal. See Figure 6.10.

The voltage at the input, v_i, is amplified by the voltage amplifier by a factor A_V and fed to the other terminal of the capacitor C. This results in a voltage across C that equals $(1 - A_V)v_i$. The current through C thus is a factor $1 - A_V$ larger than in the integrator shown in Figure 6.9. This effect corresponds to the situation where C is replaced by a capacitor that is $1 - A_V$ times as large. See Figure 6.11. Both circuits perform the same (integrating) transfer function H_I

$$H_I = \frac{n}{j2\pi fR(1 - A_V)C} \tag{6.7}$$

6.5.1 Dynamic range

If the noise contributed by the voltage-amplifier part is negligible, we can rewrite (6.4) for the circuit depicted in Figure 6.10 and obtain for the dynamic range of this integrator

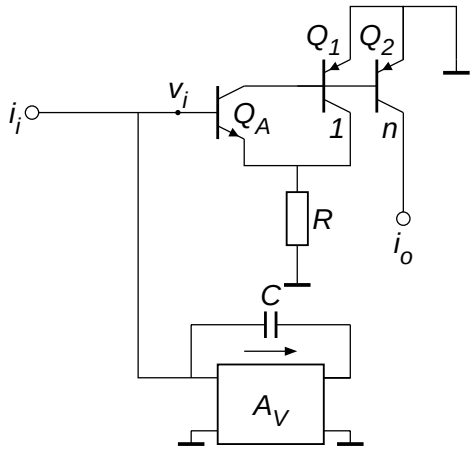

Figure 6.10: Enlarging the voltage swing across C

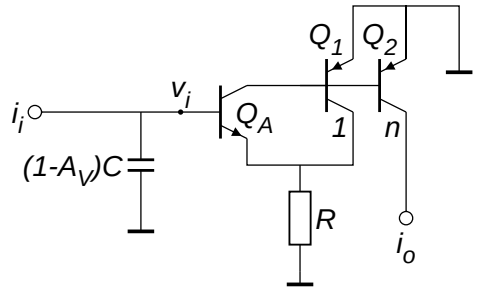

Figure 6.11: Modeling the capacitor and the voltage amplifier by means of an enlarged capacitor at the input

$$D.R. = \frac{v_{i,\max}^2}{16kT(f_2 - f_1)\left(\frac{1}{g_m} + \frac{g_m}{B_F}\left(R^2 + \frac{1}{4\pi^2 f_1 f_2 (1-A_V)^2 C^2}\right) + 2R\right)} \tag{6.8}$$

Following the same optimization procedure, we obtain a value for the optimized dynamic range that (if the influence of R on the noise contribution can be neglected) exceeds (6.6) by a factor $1 - A_V$. Because the supply voltage is limited, A_V cannot be chosen arbitrarily. A practical value is -5. The dynamic range thus improves a factor 6, or 7.8 dB.

6.5.2 Influence of the output impedance of the voltage amplifier on the transfer function

In the foregoing, it has tacitly been assumed that the voltage amplifier has an ideal (i.e., zero) output impedance. We now investigate the influence of a non-zero output impedance on the transfer function of the integrator. Suppose the voltage

amplifier can be modeled as an ideal voltage amplifier and an impedance Z_o in series with the output. The input impedance Z_i of the integrator then becomes

$$Z_i = \frac{Z_o + 1/j2\pi fC}{1 - A_V} \tag{6.9}$$

If Z_o is real, i.e., a resistance R_o, an additional zero is introduced in the transfer function of the integrator at the frequency $1/2\pi R_o C$, which causes the filter transfer function to be inaccurate at higher frequencies. The design of the voltage amplifier must thus be done in such a way that this inaccuracy is tolerable.

6.5.3 The voltage amplifier

An elegant way of realizing the voltage amplifier is providing the transconductance amplifier with an additional (scaled) output and transform the outcoming current into a voltage by means of a transimpedance amplifier. This is depicted in Figure 6.12. The input voltage v_i is transformed into a current mv_i/R_1 , available from the collector of the additional transistor Q_3, which in turn is transformed into a voltage $-mv_iR_2/R_1$ by the op amp and resistor R_2. Thus

$$v_C = (1 - A_V)v_i = \left(1 + \frac{mR_2}{R_1}\right) v_i \tag{6.10}$$

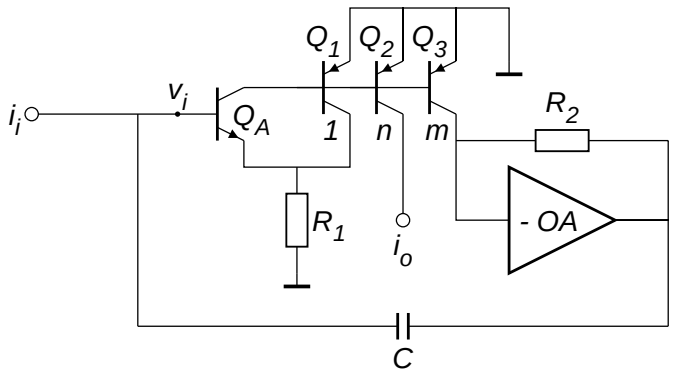

Figure 6.12: Realizing the voltage gain by an additional integrator output and a transimpedance amplifier

A possible embodiment of the transimpedance amplifier might be a single shunt stage. This is depicted in Figure 6.13. This often produces satisfying results.

An example of a filter using an integrator with enlarged voltage swing across the capacitor is discussed in Chapter 7.

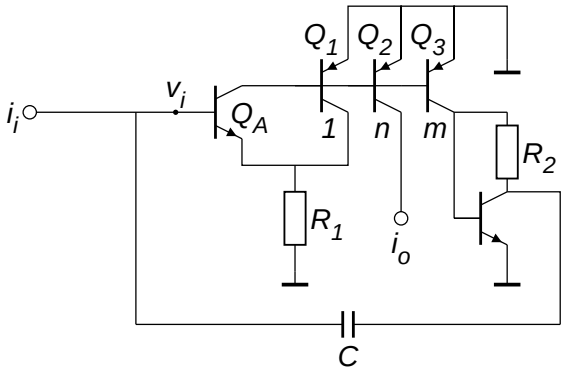

Figure 6.13: Possible implementation of the integrator using a shunt stage for the transimpedance amplifier

6.6 An example: a low-voltage low-power current-mode highpass leapfrog filter

6.6.1 Introduction

As the size and power consumption of electronic circuits are becoming increasingly important, the demand for circuits that use one single battery and consume little current is increasing. Examples of such application areas are hand-carried radiotelephones, pagers and hearing instruments (see e.g. [18, 19, 20, 21]). To improve the speech intelligibility in these systems, especially of consonants, often a highpass filter is used [22, 23, 24]. Apart from operating at 'low-voltage level' (i.e. 1–1.3 V) and consuming as little current as possible to ensure long battery life, the filter bandwidth must be programmable to ensure a wide application area. Moreover, insofar as possible, external components should be avoided.

This section deals with the design and measurement of a fully integrated second-order highpass Butterworth filter that meets all former specifications and whose cutoff frequency can be varied from 100 Hz to 1 kHz. In subsections 2 and 3, the filter design is followed from a suitable filter architecture, via the elementary building blocks, up to their signal path. Together with a proper biasing circuit, these blocks form the complete filter, as described in subsection 4. Subsection 5 deals with a semicustom realization of which, in subsection 6, measurement results are given.

6.6.2 A first approach

Our starting point is a second-order highpass Butterworth leapfrog filter as depicted in Figure 6.14. The filter consists of integrators (because of their frequency stability) and current mirrors with multiple outputs and operates in the current

domain. The right-hand current mirror provides three output signals: one equals the (inverted) input signal, the other two equal half the input signal. The input-output relation $H(f)$ is given by

$$H(f) = \frac{i_o}{i_i} = \frac{1}{j^2 + j\sqrt{2}f_c/f + f_c^2/f^2} \tag{6.11}$$

in which f_c denotes the cutoff frequency of the filter. Note that for every f_c the filter response is maximally flat (i.e., a Butterworth characteristic).

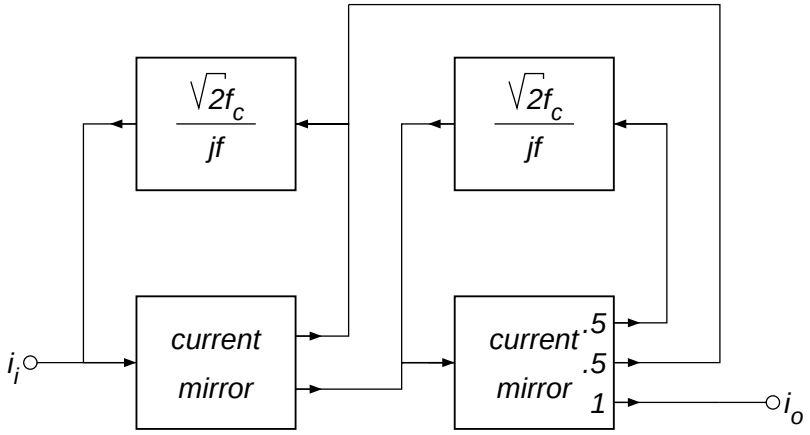

Figure 6.14: Implementation of a second-order highpass Butterworth leapfrog filter operating in the current domain

6.6.3 The integrator blocks

For the integrator we have taken the circuit shown in Figure 6.9. See Figure 6.15.

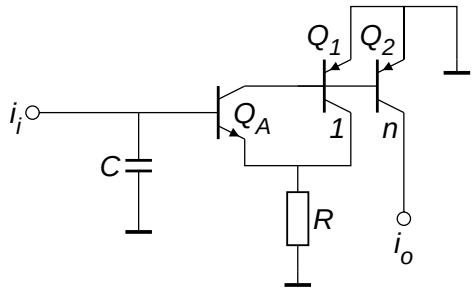

Figure 6.15: Circuit diagram of the integrator

This integrator realizes the transfer function

$$H_I = \frac{n}{j2\pi fRC} \tag{6.12}$$

The scaling factor n sets the cutoff frequency f_c of the filter. Combining (6.11) and (6.12) we find that n must satisfy

$$n = 2\pi\sqrt{2}\ f_c RC \tag{6.13}$$

The noise performance of the integrator can be optimized using (6.6) resulting in an optimal collector current I_{C,Q_A} of the first stage

$$I_{C,Q_A,\text{opt}} = \frac{V_T}{\sqrt{R^2/B_F + 1/4\pi^2 B_F C^2 f_1 f_2}} \tag{6.14}$$

The maximum output current $i_{o,\max}$ of the integrator can be determined from the maximum input voltage, $V_{C,\max}$. With (6.13) it follows that

$$i_{o,\max} = v_{C,\max} n/R = v_{C,\max} 2\pi\sqrt{2}\ f_{c,\min} C \tag{6.15}$$

$f_{c,\min}$ being the minimum cutoff frequency of the filter. As $i_{o,\max}$ is delivered by Q_2, the collector current of Q_2, I_{C,Q_2}, is best chosen to be at least $i_{o,\max}/2$. A practical value of 0.6 times $i_{o,\max}$ will do. As the filter has to operate at voltages down to 1 V, $V_{C,\max}$ has been chosen equal to 200 mV.

The tuning of the filter is done by varying the factor n, which equals the collector current of Q_2, I_{C,Q_2} divided by the collector current of Q_1, I_{C,Q_1}. With (6.13) it follows:

$$I_{C,Q_1} = I_{C,Q_2}/n = I_{C,Q_2}/2\pi\sqrt{2}\ f_c RC \tag{6.16}$$

Only a proper choice of the resistance R remains. Therefore we look at the efficiency η of the integrator, defined as follows:

$$\eta = \frac{\text{maximum signal current at the output}}{\text{total supply current of the integrator}} \tag{6.17}$$

or:

$$\eta = \frac{nI_{C,Q_1}}{I_{C,Q_A} + (n+1)I_{C,Q_1}} \tag{6.18}$$

In order to obtain good efficiency we see that it is appropriate to choose n larger than one for all cutoff frequencies possible. With (6.13) it follows that

$$n = 2\pi\sqrt{2}\ f_c RC > 1\ \forall\ f_c \tag{6.19}$$

and thus

$$R > \frac{1}{2\pi\sqrt{2}\, f_{c,\min} C} \tag{6.20}$$

In practice, this frequently yields values of R that cannot be integrated. For example, if $f_{c,\min}$ equals 100 Hz and C equals 400 pF this results in: $R > 2.8$ MΩ. In most standard bipolar IC processes, the value of a diffused resistor is limited to several hundreds of kilo ohms. Apart from this, the noise behavior is seriously degraded by such a large value. See (6.4). Hence, a compromise must be found.

6.6.4 The complete filter

When we combine two integrators with two current mirrors with multiple outputs according to the block diagram shown in Figure 6.14, we have completed the signal path of the complete filter (Figure 6.16). The (adjustable) scale factor n, which determines the cutoff frequency of the filter, is obtained by means of an adjustable voltage source V_F:

$$n = e^{-V_F/V_T} \tag{6.21}$$

With (6.13) it follows:

$$f_c = \frac{n}{2\pi\sqrt{2}\, RC} = \frac{e^{-V_F/V_T}}{2\pi\sqrt{2}\, RC} \tag{6.22}$$

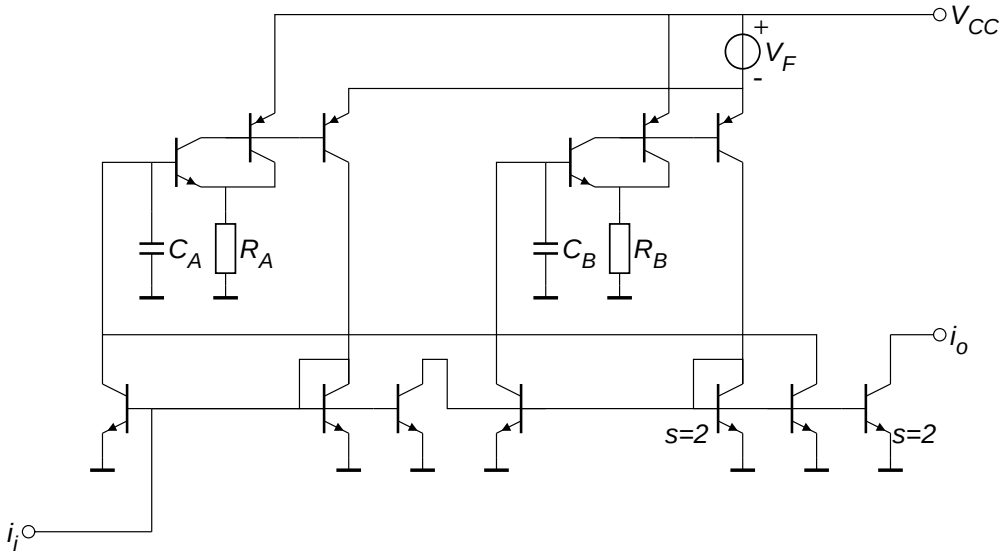

Figure 6.16: Signal path of the complete filter, $s = 2$ means a doubled emitter area ratio

This exponential relation between V_F and the cutoff frequency enables us to adjust the cutoff frequency over a wide range. If V_F is made proportional to the absolute temperature (PTAT), the cutoff frequency is independent of the temperature.

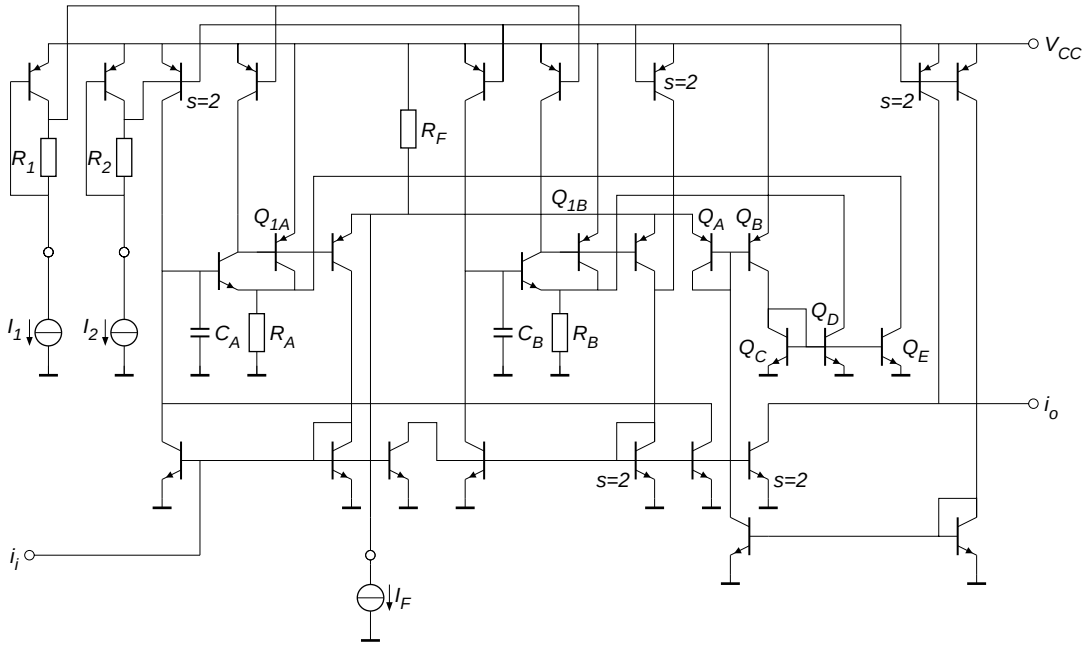

Figure 6.17: The filter including its biasing scheme. $s = 2$ means a doubled emitter area ratio

The complete filter, including its biasing scheme, is depicted in Figure 6.17. Gm-compensated mirrors [25] with multiple outputs provide the bias currents of every stage. When the voltage across R_1 and R_2 equals the thermal voltage V_T ($= kT/q$), the output of the mirror is insensitive to its input (I_1 and I_2). At this point I_1 and I_2 equal e times the output currents $I_{C,Q_A,\mathrm{opt}}$ and I_{C,Q_2}, respectively. With (6.14) and (6.15) it follows that

$$I_1 = e\, I_{C,Q_A,\mathrm{opt}} = e\, \frac{V_T}{\sqrt{R^2/B_F + 1/4\pi^2 B_F C^2 f_1 f_2}} \tag{6.23}$$

$$I_2 = e\, I_{C,Q_2} = 1.2\ \pi e \sqrt{2}\ v_{C,\max}\ f_{c,\min} C \tag{6.24}$$

$$R_1 = \frac{V_T}{I_1} \tag{6.25}$$

$$R_2 = \frac{V_T}{I_2} \tag{6.26}$$

The currents I_1 and I_2 originate from an external circuit which controls whether the filter is on or off (standby position). Transistors Q_A through Q_E provide the

collector currents of Q_{1A} and Q_{1B}. The voltage source V_F is realized by a single resistor R_F through which flows a current I_F that is derived from an external circuit (e.g., a potentiometer or a programmable current source):

$$I_F = \frac{V_F}{R_F} = -\frac{V_T}{R_F} \ln\left(2\pi\sqrt{2}\ f_c RC\right) \tag{6.27}$$

Besides this current I_F, two emitter currents also contribute to the voltage over R_F. Because they contain an AC component as well, there is distortion of the output signal at higher input signal levels. The distortion can be made sufficiently small by choosing R_F to be smaller and I_F larger. Unfortunately, this degrades the efficiency of the filter. An acceptable compromise is therefore to be found with the aid of computer simulations. In critical situations, the distortion can be reduced by means of a buffered voltage source [26].

6.6.5 Semicustom realization

The active circuitry shown in Figure 6.17 has been integrated in a semicustom chip in the LA251 process [27]. Figure 6.18 shows a microphotograph of the chip. The two integrating capacitors C_A and C_B were chosen to be 400 pF. The two (diffused) resistors R_A and R_B were chosen to be 200 kΩ. These values can be integrated easily in an ordinary full-custom process. With T, B_F, f_1, f_2 and $f_{c,\min}$ assumed 300 K, 100, 100 Hz, 10 kHz and 100 Hz, respectively, (6.23)–(6.26) result in

$$\begin{aligned} I_1 &= 1.6\ \mu\text{A} \\ I_2 &= 120\ \text{nA} \\ R_1 &= 16\ \text{k}\Omega \\ R_2 &= 220\ \text{k}\Omega \end{aligned}$$

For R_F a 6-kΩ resistor has been chosen. I_F therefore varies between 1.5 and 11 μA.

6.6.6 Measurements

The communication between the filter and the measuring instruments was done as follows. In order to perform the voltage-to-current conversion, a 100-MΩ resistor was chosen. The output signal was made measurable by an op amp and a 1-MΩ resistor in transimpedance configuration, to perform the current-to-voltage conversion. For three different values of the control current I_F, corresponding with cutoff frequencies of 100, 320 and 1000 Hz, respectively, the gain and phase

Figure 6.18: Micro-photograph of the semicustom chip.

of the transfer were measured. The result is shown in Figure 6.19. We observe a second-order Butterworth characteristic between 10 Hz and 10 kHz. The loss in the pass-band is less than 1 dB. The bandwidth equals 10 kHz. The filter linearity was evaluated by measuring the total harmonic distortion for various input signals. The maximum current (at both the input and output) corresponding to a 5 % total harmonic distortion amounts to 25 nA (peak value). Combining this figure with the measured output noise of 57 pA_{rms} yields a dynamic range of 50 dB. The filter operates well at voltages down to 1.0 V and consumes less than 16 μA. No instability occurs.

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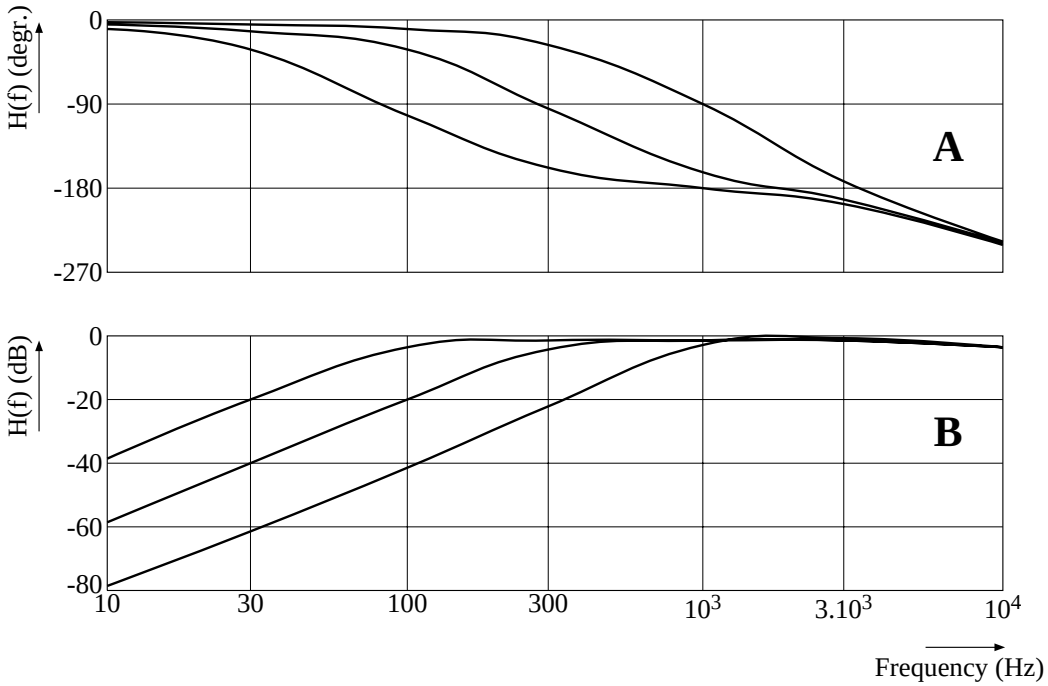

Figure 6.19: Phase (A) and gain (B) transfer of the filter

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Chapter 7

A universally applicable analog integrated circuit for hearing instruments

Walk
In silence
Don't walk away
In silence
See the danger
Always danger
Endless talking
Life rebuilding
Don't walk away

Joy Division: Atmosphere

7.1 Introduction

More and more people have great difficulty in understanding speech in surroundings with background noise and/or reverberation. This especially is a problem for an increasing number of elderly people. It is estimated that in the Netherlands of all the people older than 65 more than 30 % suffer from hearing impairment. Apart from these people, also about half a million people on the work floor run the risk of becoming subject to severe hearing damage. Every year another 20,000 young people become hard of hearing, as a direct result of listening to their favorite music or playing in their own band. And as if all that is not enough, also the ears of babies and little children are in danger from noisy toys.

All these people may become easily isolated by the lack of communication

with other people in their immediate surroundings. This is particularly true in situations such as informal get-togethers, parties, meetings, cafés and playgrounds.

Hearing impairment may be due to various causes, either external or pathological, but is frequently the result of the aging of the auditory organ itself [1]. This often entails both the attenuation and the distortion of sounds [2]. It is the distortion of sounds especially that results in a worse speech intelligibility in noisy surroundings.

In the past, various devices have been invented to assist those with impaired hearing. Until 1900 they were often shaped as a tapered horn. In the horn, the sound energy at the large opening is concentrated towards a small opening on the side of the ear. After the turn of the century, the first commercially available electrical hearing aids were introduced [3]. Initially they only consisted of a microphone, a telephone and a bulky battery. Amplification was achieved in the transduction process from acoustic to electrical signals in the carbon-microphone. These early hearing aids were of poor quality and provided limited gain. A major turning point came with the invention of electron tubes, the first active components, and the development of practical electronic amplifiers [4].

When the transistor was invented, smaller apparatus could be developed. At the end of the fifties, the first hearing instruments of the behind-the-ear type appeared. These had an enormous advantage over all the earlier types: they could be worn almost invisibly. Some types were also supplied with a pick-up coil for listening via an induction-loop system, as used in, e.g., churches, theaters and other public buildings.

In the eighties, hearing instruments that could be worn inside the ear appeared. Apart from the cosmetic effect, their main advantages are the small size, and the natural placement of the microphone, which enables directional hearing. With the progress in IC technology other features became possible. Today there are remote-controlled, digitally programmable, and self-adapting apparatus.

It must be noted that amplification alone is often insufficient, because not only the desired sound but also the noise is amplified. In this case, some improvement of the speech intelligibility can be obtained by applying signal processing in the frequency or time domain [5]. For this reason, many types of today's hearing instruments are equipped with filters, gain controls (whether automatic or not), limiters or a compression/expansion circuitry [6].

7.2 A universally applicable analog integrated circuit for hearing instruments

Since 1990, our project group 'Low-Voltage Low-Power Electronics' of the Electronics Research Laboratory has been engaged in the research and development

of universally applicable analog integrated circuits for hearing instruments. This project is being carried out in close cooperation with an industrial partner. The functions to be incorporated are:

- a microphone preamplifier
- a pickup-coil preamplifier
- a highpass filter with adjustable cutoff frequency
- a lowpass filter with adjustable cutoff frequency
- an input-controlled automatic gain control (AGC-I) with adjustable knee level
- an output-controlled automatic gain control (AGC-O) with adjustable knee level
- a volume control
- a maximum-gain control
- a gain-tolerance control
- a power amplifier
- a -30-dB output, used for driving external power amplifiers in so-called super-power hearing aids
- a microphone supply

In the following sections, the design and measurement of the preamplifiers, the filters and the input-controlled automatic gain control (together denoted as the front-end of the total hearing instrument) are described. For this purpose we use the results as discussed in the preceding three chapters. The other parts (forming the the rear-end of a hearing instrument) are being designed by my colleague Albert van der Woerd and are not discussed here.

7.3 Specifications

The integrated circuitry of the front-end had to fulfill the following requirements:

7.3.1 General parameters

- chip area: as small as possible, preferably less than 5 mm^2
- supply voltage: 1.1 – 1.6 V
- supply impedance: 0 – 100 Ω
- current consumption: as small as possible, preferably less than 300 μA
- temperature range: 10 – 45 ^{0}C
- preferably no external components

7.3.2 Audio parameters

Output signal

The interface between the front-end and the rear-end of the hearing instrument is a signal current of maximally 5 μA (peak value).

Bandwidth and distortion

- bandwidth: at least from 150 Hz to 8 kHz. (-3 dB)
- distortion: $< 7\%$ when input signal is between 14 and 28 mV_{rms} and $< 2\%$ when input signal is less than 14 mV_{rms}

Microphone preamplifier

- source impedance: 4.4 kΩ in series with 33 nF
- input impedance: 50 kΩ
- input referred noise of total hearing instrument:
  - max. 2 μV_{rms} A-weighted when gain is between max. gain and 26 dB below max. gain
  - 10 μV_{rms} A-weighted when gain is 40 dB below max. gain is tolerable
- max. input signal:
  - 28 mV_{rms} unweighted for frequencies higher than 50 Hz.
  - 56 mV_{rms} unweighted for frequencies lower than 50 Hz.

Pickup-coil preamplifier

- transimpedance amplifier[1], gain adjustable from 6 to 60 kΩ with an external resistor
- load is the input impedance of the microphone preamplifier
- max. output voltage: 24 mV_{rms}
- source impedance: L in series with R, L between 500 and 900 mH, R = 2 kΩ
- output impedance: about 4 kΩ, in correspondance with the microphone impedance
- output noise: $< 5\mu V_{rms}$ flat between 100 Hz and 10 kHz
- max. current consumption: $< 30\mu A$

Highpass filter

- order: 2
- cutoff frequency: 100 – 1600 Hz (linearly adjustable in octaves)
- stop-band attenuation: $>$ 40 dB

Lowpass filter

- order: 2
- cutoff frequency: 1.6 – 8 kHz (linearly adjustable in octaves)
- stop-band attenuation: $>$ 30 dB

AGC-I

- attack time: $<$ 5 ms
- release time: 80 ms
- knee level: 60 μV_{rms} – 28 mV_{rms} (linearly adjustable in dBs)
- compression ratio above knee level: 2

[1] Although the output *voltage* of the pickup coil is proportional to the magnetic flux, the linearity of the transfer is not essentially different when using either *voltage* or *current* sensing. In the latter case, however, the transfer also depends on the coil impedance. Together with a coupling capacitor this leads to a second-order low-frequency roll-off, which can improve the speech intelligibility. For this reason *current* sensing is used here.

7.4 A compression/expansion system

From the input-referred noise and the maximum input signal, it follows that the dynamic range of the total hearing instrument must be at least $28\text{mV}/2\mu\text{V} = 83$ dB. This requires of all the circuits in the signal path that their dynamic range is at least more than this 83 dB. Due to the limited supply voltage, this is a problem especially in circuits that have a voltage as the information-carrying quantity somewhere inside, such as integrators. The filters described in Chapter 6 use integrators and we thus can expect that the design of filters with more than 83 dB dynamic range is the hardest part of the total design.

In the example given in Chapter 6, a second-order highpass filter has been presented that, with some minor modifications, could be applicable in this design. However, for a 83-dB dynamic range, instead of 50 dB, this would require a total capacitance of 36 nF, which is unacceptable in a fully-integrated realization. Even with the aid of a transconductance amplifier with enlarged voltage swing across the integrating capacitor, 15 nF would still be necessary. This also is unacceptable.

For the above reasons, a compression/expansion solution has been chosen. The key idea is that, in order to fulfill the dynamic range requirements of the total circuit, the signal must be compressed before it is passed to the 'noisy' filters. Afterwards, the signal is expanded again to restore the original input-output relation. Thus, the noise is always masked by the signal, leading to a virtually higher dynamic range. As the total circuit already contains a compressor (AGC-I) only one additional expander is needed. The operation of the total compression/expansion system is as follows. The compressor compresses the input signal when it becomes larger than a fixed reference level. This reference level corresponds with the lowest knee level of the AGC-I ($60\ \mu\text{V}_{\text{rms}}$). In the compressor also a control signal is generated that contains information about the magnitude of the input signal. This signal controls the gain of the controlled amplifier in the compressor but can also be used to control the gain of the expander. In the expander the control signal is compared with the knee level. If the input signal is smaller than the knee level the expander will expand; the input-output relation becomes linear again. If the input signal is larger than the knee level the expander must no longer be controlled by the control signal; the input-output relation remains compressed. Note that in this system the knee level thus is set by the expander and not by the compressor.

Another point of concern is offset. In bipolar integrated circuits offset occurs as a product of base currents and mismatch between the various components. For this reason the second-order highpass-filter function is realized by means of two first-order highpass filters in cascade. These two filters can be inserted at places where the offset may become critical and thus they act as offset filters. Of course, when used in this way, the poles of the highpass filter function cannot be complex. However, this is no problem in this application.

As discussed in Chapter 5, a compressor consists of three parts: a controlled amplifier, a comparator and an integrator. Instead of using a microphone preamplifier with a fixed transfer followed by a controlled amplifier, it is also possible to provide the microphone preamplifier with a controlled output. This reduces the complexity of the total circuit. The remaining circuitry of the compressor, viz. the comparator and the integrator, are called from now on the *envelope processor*.

During the design process, it also appeared that too much offset could be expected to originate from the microphone preamplifier. For the highpass filter this does not pose a problem as it acts as an offset filter itself. However, for the envelope processor, the offset leads to uncertainty in the value of the knee level. Therefore an additional offset filter has been placed between the microphone preamplifier and the envelope processor.

The resulting block diagram is depicted in Figure 7.1

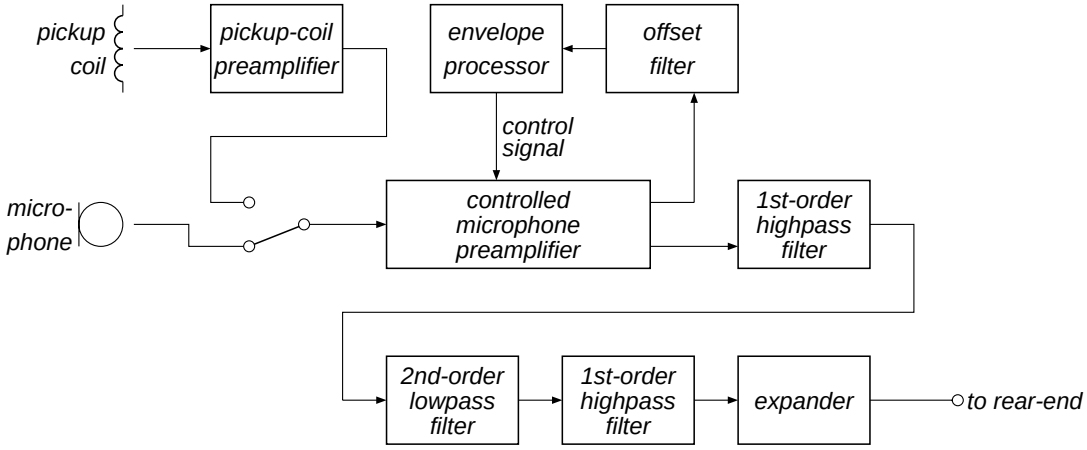

Figure 7.1: Block diagram of the front-end

Needless to say that, as this is a typical low-voltage low-power analog integrated circuit, current has been chosen as the information-carrying quantity wherever possible. The interface between the various circuits is thus performed by currents.

7.5 The filters

As has been mentioned earlier in this chapter, it is to be expected that the filters set an upper limit to the dynamic range of the total hearing instrument. We therefore discuss them first.

7.5.1 The two first-order highpass filters

The starting point of our discussion is a first-order highpass leapfrog filter operating in the current domain (Chapter 6), as depicted in Figure 7.2. The filter consists of an integrator (because of its frequency stability) and a current mirror with multiple outputs. The input-output relation $H(f)$ is given by

$$H(f) = \frac{i_o}{i_i} = \frac{-1}{1 + f_c/jf} \tag{7.1}$$

in which f_c equals the cutoff frequency of the filter.

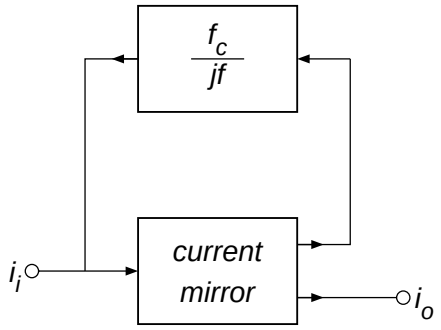

Figure 7.2: A first-order highpass leapfrog filter operating in the current domain

For the integrator we have taken a capacitance-transconductance amplifier with enlarged voltage swing (Chapter 6). See Figure 7.3.

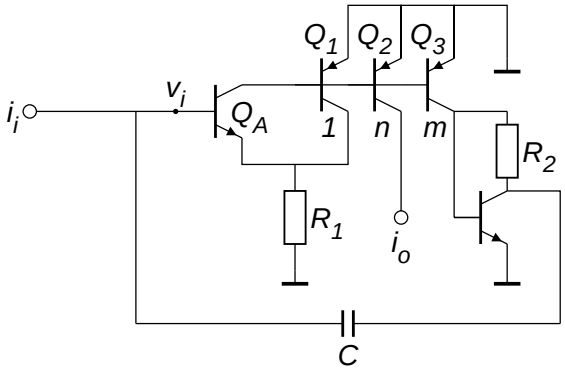

Figure 7.3: Signal path of the integrator

This integrator realizes the transfer function

$$H_I = \frac{n}{j2\pi f R_1(1 - A_V)C} \tag{7.2}$$

with $A_V = -R_2/R_1$.

The scaling factor n sets the cutoff frequency f_c of the filter. Combining (7.1) and (7.2) we find that n must satisfy

$$n = 2\pi f_c R_1 (1 - A_V) C \tag{7.3}$$

The noise performance of the integrator can be optimized by varying the collector current of the first stage, Q_A, resulting in an optimal collector current

$$I_{C,Q_A,\text{opt}} = \frac{V_T}{\sqrt{R_1^2/B_F + 1/4\pi^2 B_F (1 - A_V)^2 C^2 f_1 f_2}} \tag{7.4}$$

f_1 and f_2 being the lowest and highest frequency of the audio bandwidth respectively.

The maximum output current $i_{o,\max}$ of the integrator can be determined from the maximum input voltage, $V_{C,\max}$. With (7.3) it follows that

$$i_{o,\max} = V_{C,\max} n / R_1 = V_{C,\max} 2\pi f_{c,\min} (1 - A_V) C \tag{7.5}$$

$f_{c,\min}$ being the minimal cutoff frequency of the filter.

The tuning of the filter is done by varying the factor n, which equals the collector current of Q_2, I_{C,Q_2} divided by the collector current of Q_1, I_{C,Q_1}. With (7.3) it follows:

$$I_{C,Q_1} = I_{C,Q_2}/n = I_{C,Q_2}/2\pi f_c R_1 (1 - A_V) C \tag{7.6}$$

Only a proper choice for the resistors R_1 and R_2 remains. Therefore we look at the efficiency of the integrator. In Chapter 6 we concluded that n is best chosen larger than one for all cutoff frequencies possible. With (7.3) it follows that

$$n = 2\pi f_c R_1 (1 - A_V) C > 1 \;\forall\; f_c \tag{7.7}$$

and thus

$$R_1 > \frac{1}{2\pi f_{c,\min} (1 - A_V) C} \tag{7.8}$$

With $f_{c,\min} = 100$ Hz, $C = 400$ pF and $A_V = -5$ this results in: $R_1 > 660$ kΩ and $R_2 = -A_V R_1 > 3.3$ MΩ. These are very large values for an IC. Apart from this the noise behavior is seriously degraded by such a large R_1. A compromise therefore has been adopted: $R_1 = 40$ kΩ and $R_2 = 200$ kΩ.

When we combine the integrator with a current mirror according to the block diagram shown in Figure 7.2, we have completed the signal path of the filter. See Figure 7.4. The adjustable scaling factor n, which determines the cutoff frequency of the filter, is obtained by means of an adjustable voltage source V_{FH}:

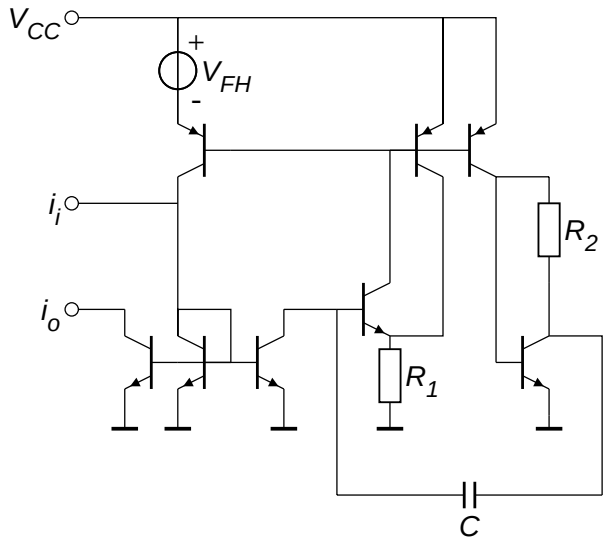

Figure 7.4: Circuit diagram of the highpass filter

$$n = e^{-V_{FH}/V_T} \tag{7.9}$$

With (7.3) it follows:

$$f_c = \frac{n}{2\pi R_1(1 - A_V)C} = \frac{e^{-V_{FH}/V_T}}{2\pi R_1(1 - A_V)C} \tag{7.10}$$

This exponential relation between V_{FH} and the cutoff frequency means that when V_{FH} varies linearly the cutoff frequency varies in octaves. If V_{FH} is made proportional to the absolute temperature (PTAT) the cutoff frequency also becomes independent of the temperature.

The complete filter, including its biasing scheme, is depicted in Figure 7.5.

All the necessary bias currents are delivered by one PTAT current source with multiple outputs. The voltage V_{FH} originates from another circuit. This circuit is not discussed here. Transistors Q_B though Q_H provide the collector current of Q_3. The terminals V_P, V_N and V_T all are connected with the PTAT current source and are used for the biasing of the other circuits. Capacitor C_X increases the phase margin of the shunt stage, to avoid instability.

7.5.2 The second-order lowpass filter

The starting point is the second-order lowpass leapfrog filter as depicted in Figure 7.6. This filter operates in the current domain, consists of two integrators, two current mirrors with multiple outputs and an ordinary current mirror. The third

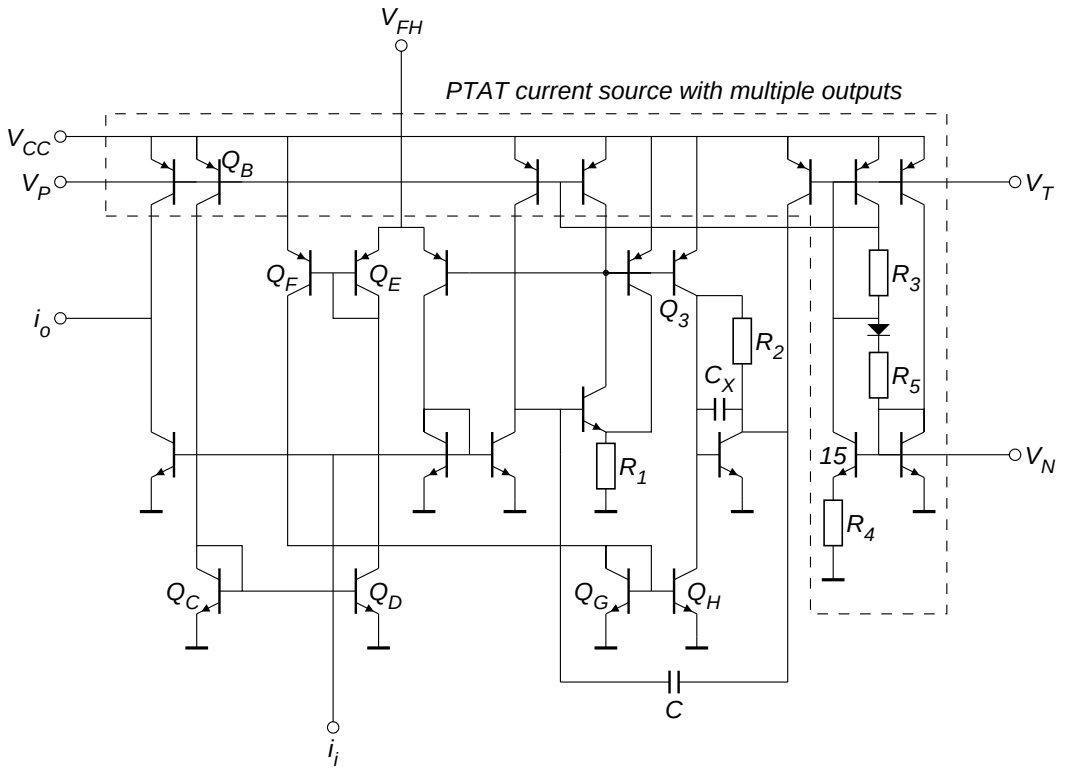

Figure 7.5: The highpass filter including its biasing scheme

output of the right mirror equals twice the (inverted) input, to obtain a zero-loss passband transfer. The input-output relation H_f of the filter is given by

$$H_f = \frac{i_o}{i_i} = \frac{-1}{j^2 f^2 / f_c^2 + j\sqrt{2} f / f_c + 1} \tag{7.11}$$

in which f_c equals the cutoff frequency of the filter. Note that for every f_c the filter response is maximally flat (i.e., a Butterworth characteristic).

For the integrator we have taken a capacitance-transconductance amplifier (Chapter 6). See Figure 7.7
This integrator realizes the transfer function

$$H_I = \frac{n}{j2\pi f RC} \tag{7.12}$$

The scaling factor n sets the cutoff frequency f_c of the filter. Combining (7.11) and (7.12) we find that n must satisfy

$$n = \pi\sqrt{2}\ f_c RC \tag{7.13}$$

The noise performance of the integrator can be optimized by varying the collector current of the first stage, Q_A, yielding an optimal collector current

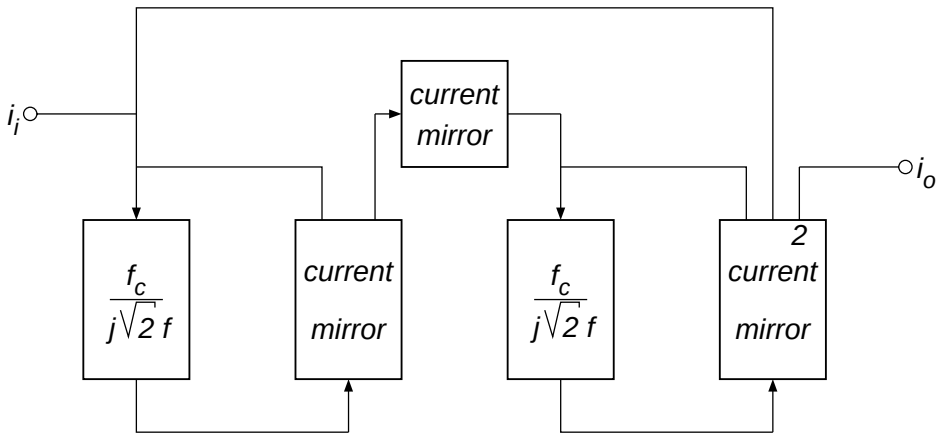

Figure 7.6: A second-order lowpass Butterworth leapfrog filter operating in the current domain

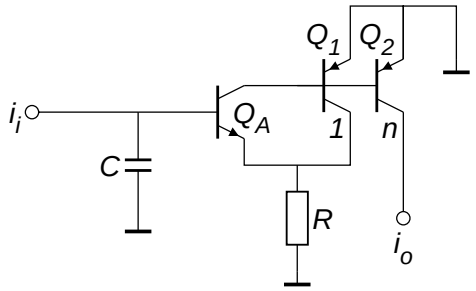

Figure 7.7: Circuit diagram of the integrator

$$I_{C,Q_A,\mathrm{opt}} = \frac{V_T}{\sqrt{R^2/B_F + 1/4\pi^2 B_F C^2 f_1 f_2}} \tag{7.14}$$

The maximum output current $i_{o,\max}$ of the integrator can be determined from the maximum input voltage, $V_{C,\max}$. With (7.13) it follows that

$$i_{o,\max} = v_{C,\max} n/R = v_{C,\max} \pi\sqrt{2}\; f_{c,\min} C \tag{7.15}$$

$f_{c,\min}$ being the minimal cutoff frequency of the filter.

The tuning of the filter is done by varying the factor n. With (7.13) it follows:

$$I_{C,Q_1} = I_{C,Q_2}/n = I_{C,Q_2}/\pi\sqrt{2}\; f_c RC \tag{7.16}$$

Only a proper choice for the resistor R remains. For that we look at the efficiency of the integrator. In Chapter 6 we concluded that n is best chosen to be larger than one for all possible cutoff frequencies. With (7.13) it follows that

$$n = \pi\sqrt{2}\ f_c RC > 1 \ \forall\ f_c \tag{7.17}$$

and thus

$$R > \frac{1}{\pi\sqrt{2}\ f_{c,\min} C} \tag{7.18}$$

With $f_{c,\min} = 100$ Hz and $C = 100$ pF this results in: $R > 1.4$ MΩ. This is a very large value for an IC. Apart from this, the noise behavior is seriously degraded by such a large value. A compromise therefore has been adopted: $R = 140$ kΩ.

When we combine the two integrators with three current mirrors according to the block diagram shown in Figure 7.6, we have completed the signal path of the filter. See Figure 7.8. The adjustable scaling factor n, which determines the cutoff frequency of the filter, is obtained by means of an adjustable voltage source V_{FL}:

$$n = e^{-V_{FL}/V_T} \tag{7.19}$$

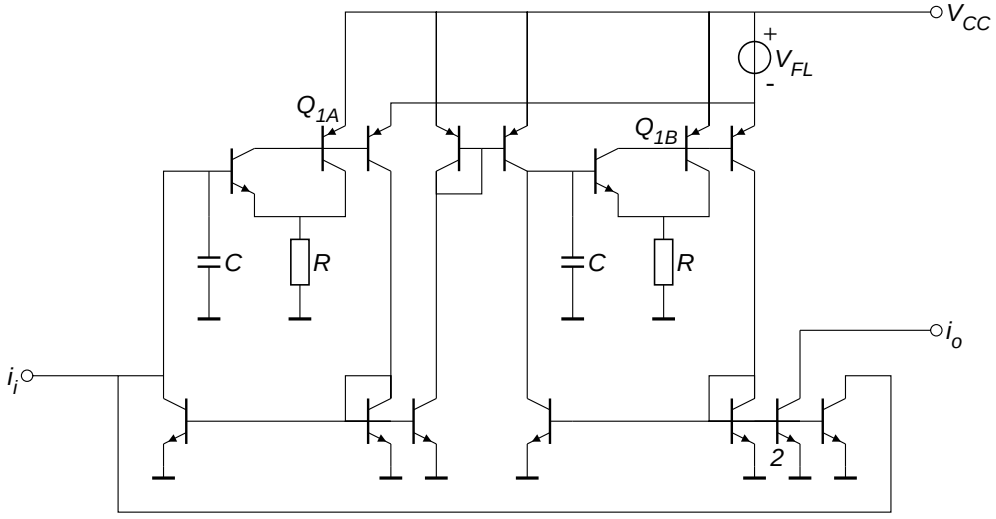

Figure 7.8: Signal path of the lowpass filter

With (7.13) it follows:

$$f_c = \frac{n}{\pi\sqrt{2}\ RC} = \frac{e^{-V_{FL}/V_T}}{\pi\sqrt{2}\ RC} \tag{7.20}$$

This exponential relation between V_{FL} and the cutoff frequency means that when V_{FL} varies linearly the cutoff frequency varies in octaves. If V_{FL} is made proportional to the absolute temperature (PTAT) the cutoff frequency also becomes independent of the temperature.

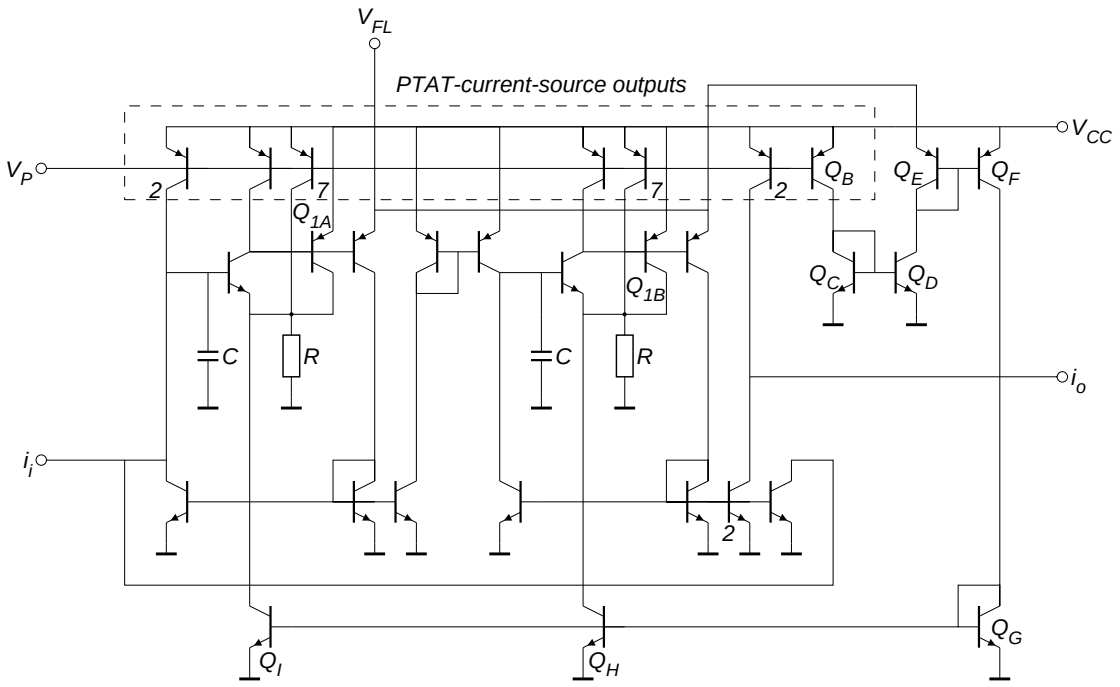

Figure 7.9: The lowpass filter including its biasing scheme

The complete filter, including its biasing scheme, is depicted in Figure 7.9.

All the necessary currents are delivered by the PTAT current source with multiple outputs in the highpass filter (terminal V_P). The voltage V_{FL} originates from another circuit. This circuit is not discussed here. Transistors Q_B though Q_I provide the collector currents of Q_{1A} and Q_{1B}.

7.5.3 The offset filter

The starting point for the design of the offset filter is the first-order highpass leapfrog filter operating in the current domain according to Figure 7.2. See Figure 7.10. The filter consists of an integrator (because of its frequency stability) and a current mirror with multiple outputs. The input-output relation $H(f)$ is given by

$$H(f) = \frac{i_o}{i_i} = \frac{-1}{1 + f_c/jf} \tag{7.21}$$

in which f_c equals the cutoff frequency of the filter.

In order to keep the voltage across the (small) integrating capacitor in the integrator within bounds the filter is scaled with a scaling factor α (Chapter 6). This gives the filter shown in Figure 7.11. The current mirror provides two different outputs. One output equals the inverted input. The other equals $1/\alpha$ times the

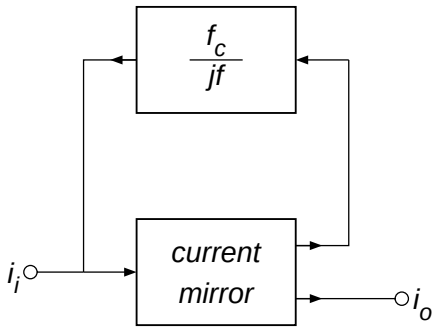

Figure 7.10: A first-order highpass leapfrog filter operating in the current domain

inverted input. This output is fed back to the integrator. Note that the transfer functions of both filters are the same.

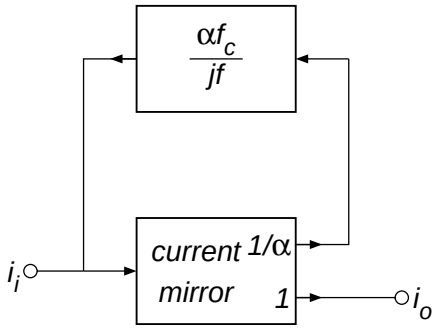

Figure 7.11: A scaled first-order highpass leapfrog filter operating in the current domain

For the integrator we have taken the circuit depicted in Figure 7.12.

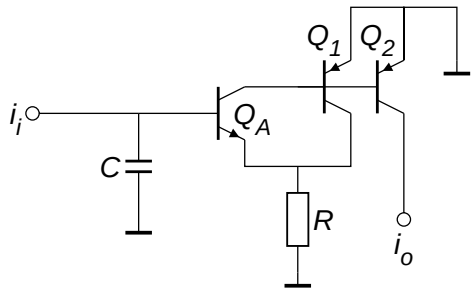

Figure 7.12: Circuit diagram of the integrator

This integrator realizes the transfer function

$$H_I = \frac{1}{j2\pi fRC} \tag{7.22}$$

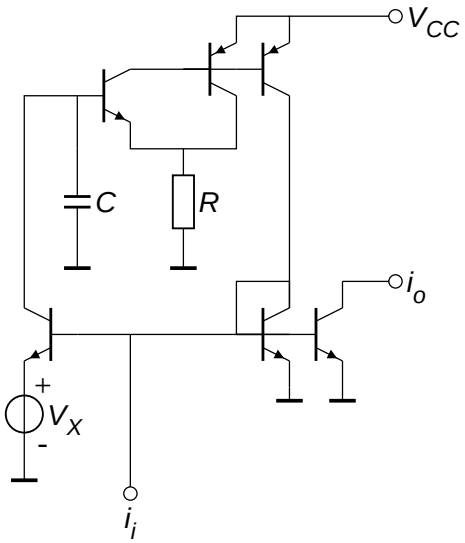

Figure 7.13: Signal path of the offset filter

Combining (7.21) and (7.22) we find that α must satisfy

$$\alpha = \frac{1}{2\pi f_c RC} \tag{7.23}$$

As the offset filter is not part of the signal path its noise performance is of minor importance. For this reason, the collector current of the first stage of the integrator is not optimized with respect to the noise contribution of the integrator, but with respect to its influence on the offset current at the output of the total filter. I_{C,Q_A} therefore simply equals the sum of the base currents of Q_1 and Q_2.

The maximum output current $i_{o,\max}$ of the integrator can be determined from the maximum input voltage, $V_{C,\max}$. With (7.22) it follows that

$$i_{o,\max} = V_{C,\max}/R \tag{7.24}$$

This determines the value of R.

When we combine the integrator with a current mirror according to the block diagram shown in Figure 7.11, we have completed the signal path of the filter. See Figure 7.13. The scaling factor $1/\alpha$ is obtained by means of a fixed voltage source V_X in series with the emitter of the scaled transistor:

$$\alpha = e^{V_X/V_T} \tag{7.25}$$

With (7.23) it follows:

$$f_c = \frac{1}{2\pi\alpha RC} = \frac{e^{-V_X/V_T}}{2\pi RC} \tag{7.26}$$

If V_X is proportional to the absolute temperature (PTAT) the cutoff frequency also is independent of the temperature.

The complete filter, including its biasing scheme, is depicted in Figure 7.14.

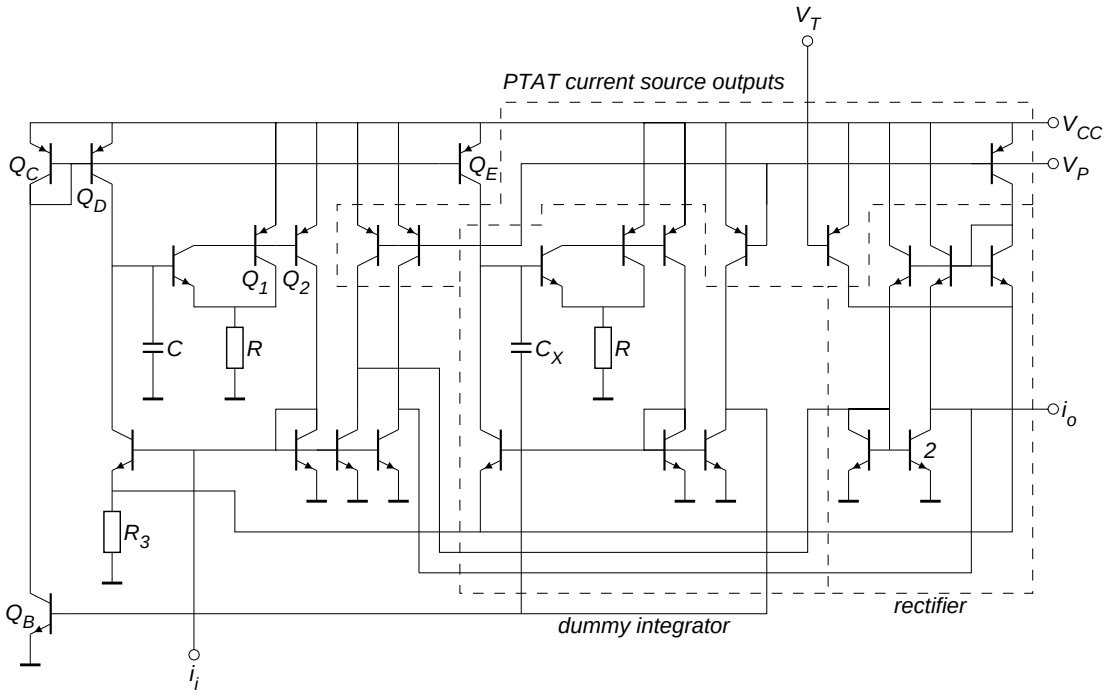

Figure 7.14: The offset filter including its biasing scheme

To reduce the offset current at the output of the filter, the correct values of the collector currents of Q_1 and Q_2 are provided by a dummy version of the integrator and transistors Q_B through Q_E. The operation is as follows. The output current of the dummy integrator is compared with a bias current coming from the PTAT current source with multiple outputs (terminal V_P). The error signal is amplified by Q_B through Q_E and fed back to the input of the dummy integrator. As the absolute value of the loop gain is much larger than one, the error signal is nullified; the dummy integrator is biased correctly. As the collector current of Q_D equals the collector current of Q_E and the integrators are identical (for DC), the integrator also is biased correctly.

The voltage source V_X is realized by means of a resistor R_3 through which flows a current. This current also originates from the PTAT current source (terminal V_T). The capacitor C_X prevents instability of the dummy integrator.

As the absolute value of the offset-filter output signal is to be compared with a reference level — this is done in the envelope processor — the output signal is fed through a rectifier before it is fed to the envelope processor.

7.6 The controlled microphone preamplifier

The next step in the design of the hearing-instrument front-end is the design of the controlled microphone preamplifier. As this circuit is the first in the total signal path, its noise performance is of major importance. It deserves, therefore, special attention.

There are three possibilities of realizing an amplifier with a 50-kΩ input impedance. We can choose a current amplifier with a 50-kΩ resistor in series with its input terminals. Although this is an easy solution, it is not applicable here, because the noise contributed by this resistor would be too large. Another solution might be a transconductance amplifier with a 50-kΩ resistor in parallel with its input terminals. However, this would turn out to be in conflict with a low current consumption. Probably the best solution is realizing the input impedance by means of a two-loop negative feedback amplifier [7, 8]. We have chosen for this solution. As the input of the first highpass filter and of the offset filter is a current, we thus need an amplifier with a fixed input resistance and a current output. The basic configuration of this amplifier is depicted in Figure 7.15.

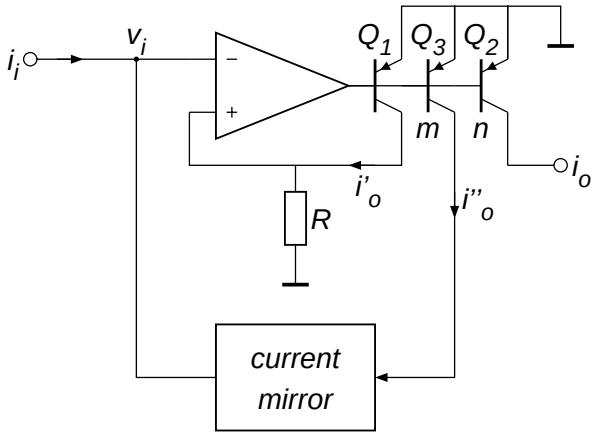

Figure 7.15: Basic configuration of an amplifier with a fixed input resistance and a current output

This type of amplifier has not been discussed in the preceding chapters. It can be considered as consisting of a combination of a transconductance amplifier and a current amplifier. The operation is as follows. The input voltage v_i is transformed by resistor R, the op amp and transistor Q_1 into a current $i'_o = v_i/R$. Q_2 provides the output current $i_o = nv_i/R$. Q_3 provides another indirect output current $i''_o = mv_i/R$, which is inverted by the current mirror and fed back to the input. As $i''_o = i_i$ we find for the input impedance R_i of the power-to-current convertor

$$R_i = v_i/i_i = R/m \tag{7.27}$$

For the transfer function H_t of the preamplifier we can write

$$H_t = i_o/v_i = n/R \tag{7.28}$$

From (7.27) and (7.28) we see that R_i and H_t can be chosen independently by means of the scaling factors m and n.

Even if the op amp is noise-free the amplifier adds some noise to the signal. This noise contribution originates from the resistor R and transistors Q_1, Q_2 and Q_3. Their noise sources can be shifted towards the input and summed in one noise voltage source $v_{n,\mathrm{eq}}$, with a power density spectrum $S(v_{n,\mathrm{eq}})$, in series with the signal source. We obtain:

$$S(v_{n,\mathrm{eq}}) = 4kTR + R^2\left(2qI_{C,Q_1} + \frac{2qI_{C,Q_2}}{n^2} + \frac{2qI_{C,Q_3}}{m^2}\right) \tag{7.29}$$

and thus

$$v_{n,\mathrm{eq}} = \sqrt{(f_2 - f_1)\left(4kTR + R^2\left(2qI_{C,Q_1} + \frac{2qI_{C,Q_2}}{n^2} + \frac{2qI_{C,Q_3}}{m^2}\right)\right)} \tag{7.30}$$

With $I_{C,Q_1} = I_{C,Q_2}/n = I_{C,Q_3}/m$ this can be rewritten as

$$v_{n,\mathrm{eq}} = \sqrt{(f_2 - f_1)\left(4kTR + 2qR^2 I_{C,Q_1}(1 + 1/n + 1/m)\right)} \tag{7.31}$$

From this expression we see that R is best chosen to be as small as possible. However, if $R < 1/H_t$, I_{C,Q_2} becomes too large. This degrades the power efficiency. A compromise therefore has been adopted: $R = 5$ kΩ. For a 50-kΩ input impedance the scaling factor m thus must equal 0.1. Unfortunately, this increases the noise again. The problem has been overcome by realizing the scaling factor m not in the power-to-current amplifier but in the current mirror. The resulting scaling current mirror is realized in class-B. When there is little signal at the input its noise production is also small. A simple class-B scaling current mirror is depicted in Figure 7.16.

This class-B mirror consists of two ordinary current mirrors (Q_{1A} and Q_{1B}, Q_{2A} and Q_{2B}) and a CB stage (Q_3). If the incoming current i_i is negative, all the current flows into the upper mirror; the CB stage and the lower mirror are off. If i_i is positive, the current flows via the CB stage to the lower mirror; the upper mirror is off. At the output, both the positive and negative half of the input signal are added and the original signal is restored.

We now return to the design of the total preamplifier.

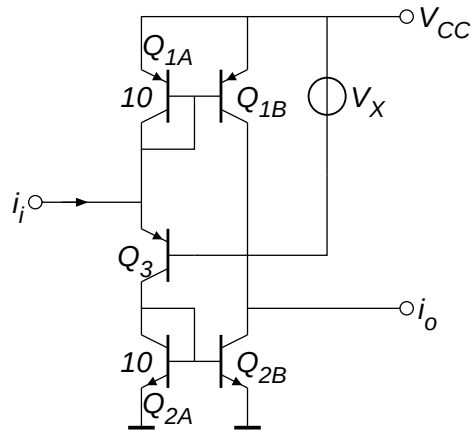

Figure 7.16: A simple class-B scaling current mirror

To here, the op amp has been considered to be noise-free. In practice, an op amp always contributes some noise. A possible implementation of the op amp is a single CE stage. The circuit diagram of the preamplifier becomes with this CE stage as depicted in Figure 7.17.

We can shift the two noise sources of the CE stage (Chapter 3) towards the input of the amplifier and transform them into one equivalent noise voltage source $v_{n,\text{eq}}$ in series with the input terminals. In Chapter 4, it was found that the power density spectrum of this noise source equals

$$S(v_{n,\text{eq}}) = S(v_n) + S(i_n)|Z_S + R|^2 \tag{7.32}$$

Z_S being the source impedance (in this situation the 4.4-kΩ microphone resistance and the 33-nF coupling capacitor).

Following the same procedure as that discussed in Chapter 4, an optimal collector current for the CE stage, $I_{C,\text{CE,opt}}$, can be found:

$$I_{C,\text{CE,opt}} = \frac{V_T}{\sqrt{(R+R_S)^2/B_F + 1/4\pi^2 B_F C_S^2 f_1 f_2}} \tag{7.33}$$

R_S and C_S being the microphone resistance and the coupling capacitor value, respectively. With $R_S = 4.4$ kΩ, $C_S = 33$ nF, $B_F = 100$ and $R = 5$ kΩ this optimal current equals 28 μA. However, 5 μA is also acceptable in this design. This only slightly deteriorates the noise behavior of the preamplifier. In view of the power efficiency 5 μA is even better.

The transfer of the preamplifier is made controllable by the scaling factor n. This scaling factor is realized by means of a controllable voltage source V_C:

$$n = e^{-V_C/V_T} \tag{7.34}$$

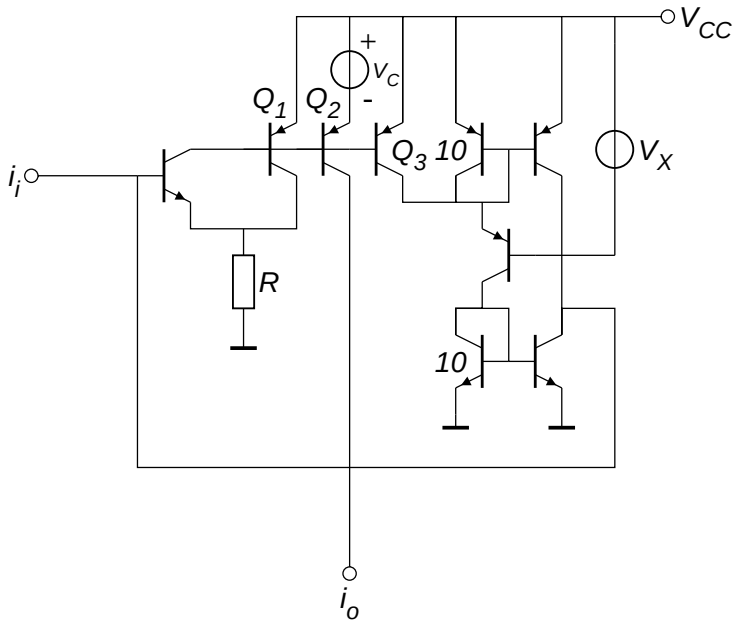

Figure 7.17: Circuit diagram of the preamplifier

With (7.28) it follows:

$$H_t = i_o/v_i = n/R = \frac{e^{-V_C/V_T}}{R} \tag{7.35}$$

The complete preamplifier, including its biasing circuitry, is depicted in Figure 7.18.

As the preamplifier must have two controlled outputs — one to be connected with the first highpass filter, the other with the offset filter — an extra output has been added. To reduce offset at both outputs, the amplifier is made almost symmetrical by means of a dummy amplifier. The collector bias currents are delivered either by the current mirror with two outputs (above) or by the gm-compensated current mirror (below). The emitter resistors R_E are used to improve the noise behavior of the total preamplifier.

The resistor R_X in the class-B current mirror reduces the current consumption at high input levels. When the input signal is large, there is a large voltage drop over R_X and the scaling factor of the npn part of the class-B current mirror decreases — the npn mirror is, in fact, a gm-compensated mirror. Therefore, the input current, and thus the current consumption, decreases.

The capacitor C_{comp} prevents the microphone preamplifier from becoming instable.

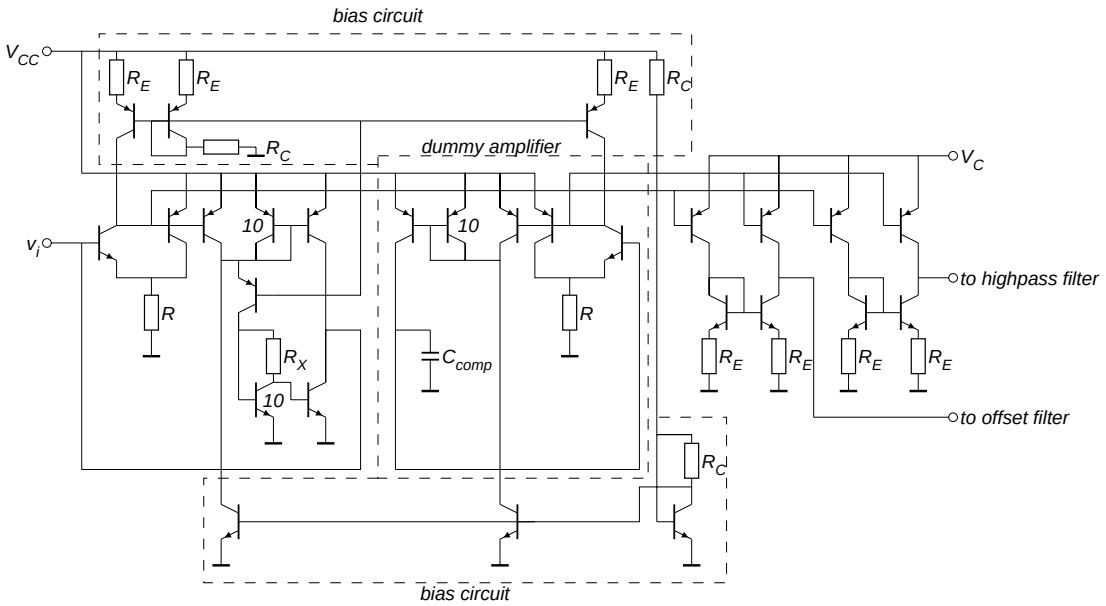

Figure 7.18: The controllable microphone preamplifier including its biasing scheme

7.7 The envelope processor

Together, the controlled microphone preamplifier and the envelope processor perform the AGC-I function. In Chapter 5, it was shown that we have three possibilities of realizing an automatic gain control with a finite compression ratio. All three contain two controlled amplifiers. However, in the agc variant with a controlled knee level — the third one — the demands that are made upon the controlled amplifier that controls the knee level can be much fewer. This reduces the circuit complexity and for this reason we have chosen this variant. See Figure 7.19.

The operation is as follows. The output signal E_o is compared with a reference level E'_K. If $E_o < E'_K$ the integrator is charged by quantity $E_{\rm rel}$; $E_{\rm int}$ increases, resulting in a larger output signal. If $E_o > E'_K$ the integrator is discharged by $E_{\rm att} - E_{\rm rel}$ ($E_{\rm att} > E_{\rm rel}$!); $E_{\rm int}$ decreases, resulting in a smaller output signal. If $m < 0$, variations of the input signal thus always result in smaller variations of the output signal. In Chapter 5, we found that the compression ratio — the ratio of the variation of the input signal and the variation of the output signal, both in dBs — must equal $1 - m$. For a compression ratio of two, m equals -1; the divider becomes an inverter. With (7.35) we find for the transfer function H_m of the controlled amplifier

$$H_m = \frac{I'_K}{I_K} = e^{-E_{\rm int}} = e^{V_C/V_T} \tag{7.36}$$

The current-domain implementation of the envelope processor is depicted in

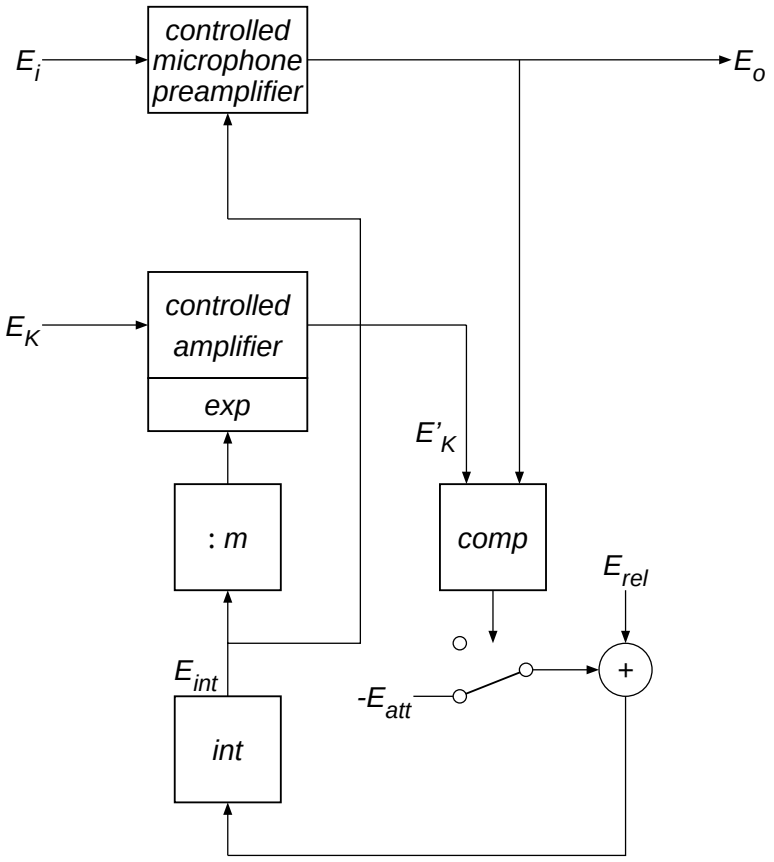

Figure 7.19: AGC with $C.R. = 1 - m$ using a controlled knee level

Figure 7.20. Apart from $E_{\rm int}$ all the quantities are represented by currents. The voltage follower generates a low-impedance version of the voltage across the capacitor C, to avoid interaction.

For the release time $t_{\rm rel}$ and the attack time $t_{\rm att}$ it is found that

$$t_{\rm rel} = \frac{2.6\ V_T C}{I_{\rm rel}} \tag{7.37}$$

and

$$t_{\rm att} = \frac{2.6\ V_T C}{I_{\rm att} - I_{\rm rel}} \tag{7.38}$$

Figure 7.21 shows the circuit diagram of the envelope processor with ideal bias sources.

The controlled current amplifier has been realized by means of a scaling current mirror. The output current of the controlled microphone preamplifier is subtracted

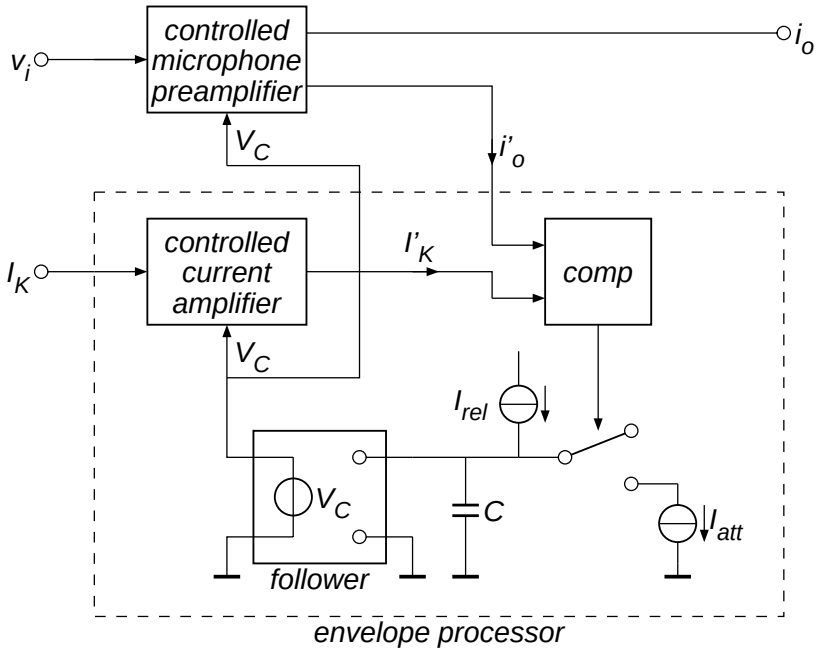

Figure 7.20: Current domain implementation of the envelope processor

from I'_K. If the remainder is negative, Q_S becomes non-conducting and the capacitor C is discharged by the current $I_{\text{att}} - I_{\text{rel}}$. If the remainder is positive, Q_S saturates and C is charged by I_{rel}. The voltage follower is realized by means of transistors Q_A through Q_D. I_1, I_2 and I_3 provide the collector currents of these transistors.

The reference current I_K corresponds with the lowest knee level of the AGC-I (60 μV). The actual knee level is set by the expander.

Figure 7.22 shows the circuit diagram of the total envelope processor including its bias circuitry. R_C realizes the current I_3. All the other currents are derived

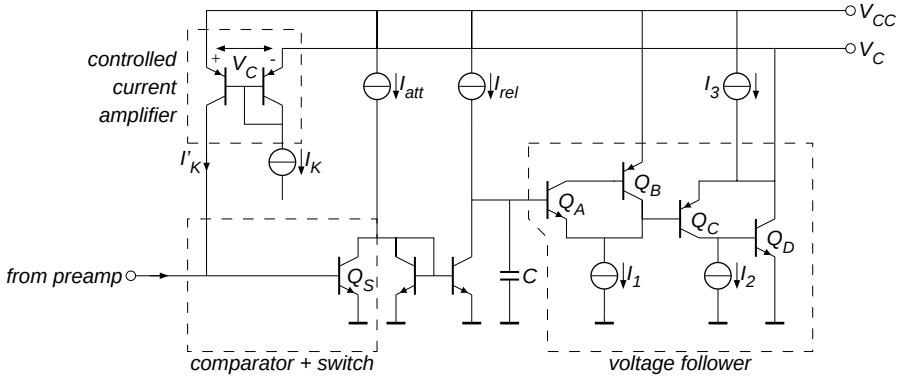

Figure 7.21: The envelope processor with ideal bias sources

from a gm-compensated current mirror with multiple outputs. The input current of this mirror originates from the PTAT current source (terminal V_N).

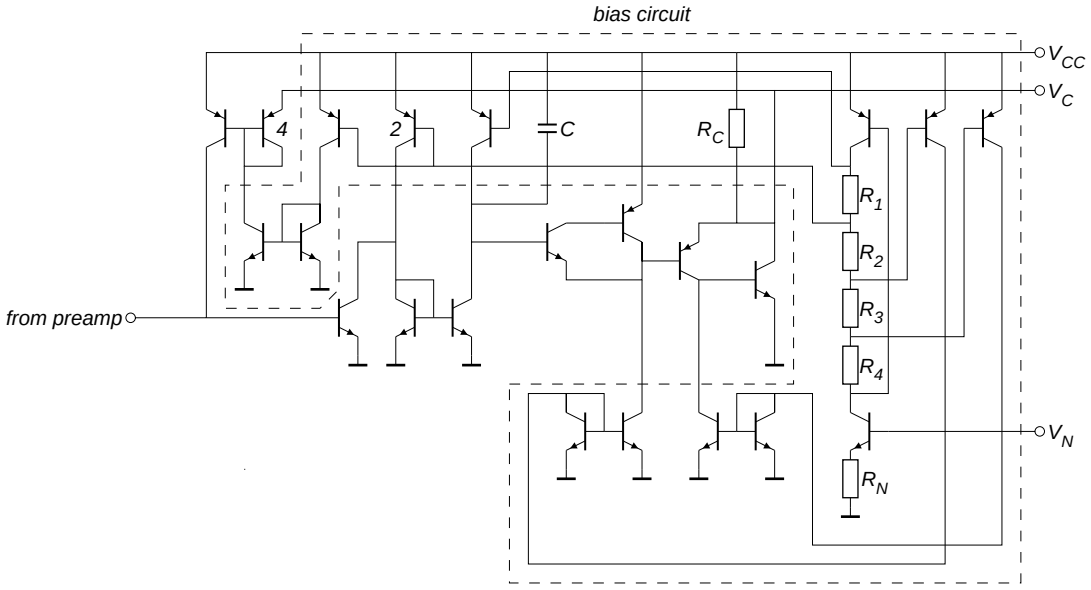

Figure 7.22: Circuit diagram of the envelope processor including its bias circuitry

7.8 The expander

In section 7.4, we discussed the function of the expander, which is to expand the signal as long as the input signal of the microphone preamplifier is beneath the knee level of the AGC-I function; if the transfer function of the expander is proportional to the inverse function of the controlled microphone preamplifier, then the total input-output relation becomes linear again. However, if the input signal is above the knee level the transfer of the expander is linear and the total system functions as a compressor with a compression factor of 2.

This can be accomplished by a simple circuit, which is depicted in Figure 7.23.

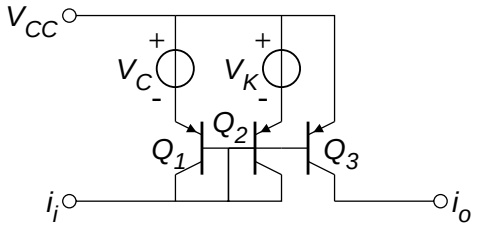

Figure 7.23: Circuit diagram of the expander

Its operation is as follows. If $V_C < V_K$ the base-emitter voltage of Q_2 is smaller than the base-emitter voltage of Q_1, and the transfer is determined by Q_1, Q_3 and V_C only. In formula

$$H_e = e^{V_C}, \; V_C < V_K \tag{7.39}$$

If $V_C > V_K$ the base-emitter voltage of Q_2 is larger than the base-emitter voltage of Q_1, the transfer is determined by Q_2, Q_3 and V_K only, or

$$H_e = e^{V_K}, \; V_C > V_K \tag{7.40}$$

If V_C is the same control voltage that is generated in the envelope processor and that is used to control the microphone preamplifier, the input-output relation $H_{\mathrm{front-end}}$ of the total front-end satisfies

$$H_{\mathrm{front-end}} = H_t H_e = \begin{cases} 1/R, & V_C < V_K \quad (7.41) \\ e^{V_K - V_C}/R, & V_C > V_K \quad (7.42) \end{cases}$$

It must be noted that the filters need not to be taken into account since they all possess a 0-dB transfer in the passband. The exponential relation between V_K and the knee level means that when V_K varies linearly, the knee level varies in dBs. If V_K is made proportional to the absolute temperature (PTAT), the knee level also becomes independent of the temperature.

The circuit diagram of the expander including its bias circuitry is depicted in Figure 7.24. In order to reduce the offset current at the output, a dummy version of the collector current of Q_3 is generated and subtracted from this collector current. The other collector currents are derived from the PTAT current source (terminal V_P). The voltage source V_K originates from another circuit. This circuit is not discussed here.

7.9 The pickup-coil preamplifier

Finally the design of the pickup-coil preamplifier: a transimpedance amplifier with a gain which is to be adjustable from 6 to 60 kΩ by an external resistor. Its output is connected to a switch which passes either this signal — in the T position — or the microphone signal — in the M position — to the input of the microphone preamplifier. For this reason, the output impedance of the pickup-coil preamplifier must approximately equal the microphone impedance (4 kΩ).

The basic configuration of a transimpedance amplifier (Chapter 4) is depicted in Figure 7.25. The additional resistor R_O has been inserted to obtain the desired output impedance.

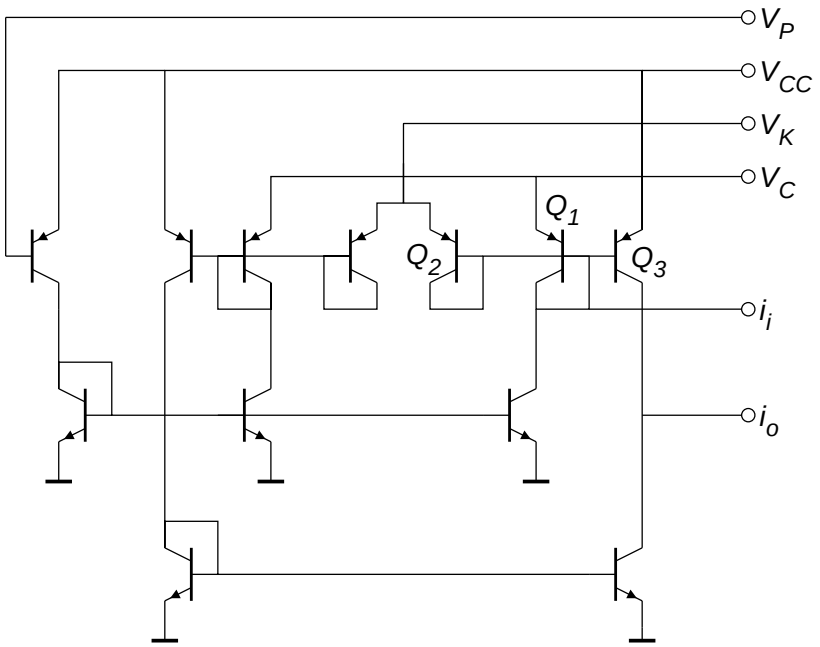

Figure 7.24: The expander including its bias circuitry

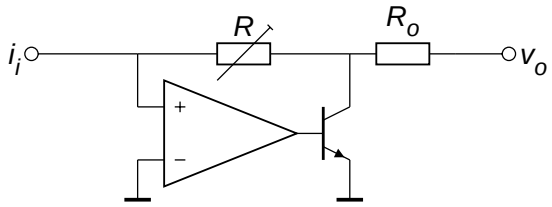

Figure 7.25: Basic configuration of the transimpedance amplifier

For the ideal transfer $A_{f,\infty}$ we can write

$$A_{f,\infty} = -R \tag{7.43}$$

A possible implementation of the op amp might be a short circuit. This results in a shunt stage. However, the loop gain of this one-transistor transimpedance amplifier is too small, which causes inaccuracy, distortion or a poor power efficiency (Chapter 4). We thus need more amplifying stages in the signal path. A practical solution is given in Figure 7.26. The circuit consists of two CE stages in cascade and a current mirror, the low-voltage counterpart of a CB stage. The noise behavior of this amplifier is determined mainly by the noise coming from the first stage Q_A and the resistor R. With regard to the noise contribution of the first stage, an optimal collector current can be found, which, unfortunately, becomes too large with regard to the power efficiency. A compromise therefore has been adopted:

10 μA.

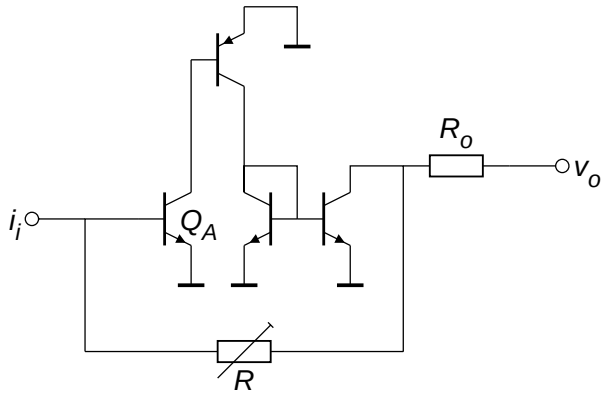

Figure 7.26: A four-transistor transimpedance amplifier

The collector current of the three other transistors depends on the output capability of the amplifier. 10 μA is a very convenient value.

Analyzing the high-frequency behavior of this amplifier we find that the closed loop contains three dominant poles, which cause the circuit to oscillate. However, this problem can easily be overcome by adding one additional transistor connected between input and output. See Figure 7.27. We now obtain a *multi-path structure* [9]. Its operation is as follows. At low frequencies the loop gain is delivered by the parallel connection of the four-transistor amplifier and the multipath transistor and, as the gain of the four-transistor amplifier is much larger, thus mainly determined by this one. At higher frequencies the multi-path transistor takes over, because its dominant pole lies at a much higher frequency than the dominant poles of the four-transistor amplifier. Therefore, the phase margin can be as high as 90 degrees. The capacitor C_X has been inserted to ensure that the dominant poles of the four-transistor amplifier indeed lie at a much lower frequency than the dominant pole of the single CE stage.

The pickup-coil preamplifier including its bias circuitry is depicted in Figure 7.28.

All collector currents are derived from a current mirror with two outputs. The emitter resistors R_E reduce the noise contribution of this mirror.

7.10 Semicustom realization of the front-end

All the circuits presented in the foregoing sections have been integrated in two semicustom chips fabricated at the Delft Institute of Microelectronics and Submicrontechnology (DIMES). Experiment results proved the correct operation of the two highpass filters, the lowpass filter, the microphone preamplifier, the envelope

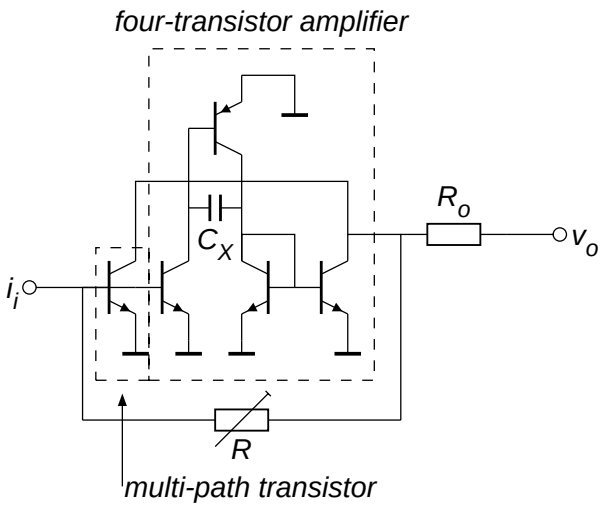

Figure 7.27: Circuit diagram of the pickup-coil preamplifier

processor, the expander and the pickup-coil preamplifier. Only the offset filter did not function properly, for a still unknown reason. In order to test the total front-end, a breadboard version of the offset filter was realized, according to the same circuit diagram and using transistor arrays fabricated in the same process. This offset filter operated correctly. The measurement results are discussed in the following subsections .

7.10.1 General parameters

- supply voltage (35 ^{0}C): 1.05 – 1.9 V
- current consumption (35 ^{0}C): 120 – 175 μA
- temperature range (1.3 V): -40 – +100 ^{0}C

7.10.2 Audio parameters

Input-output transfer

- i_L/v_S = 100 μA/V

Bandwidth and distortion

- bandwidth: from 70 Hz to 100 kHz (-3 dB)
- distortion: $< 2.1\%$ when input signal is between 14 and 28 $\mathrm{mV_{rms}}$ and $< 1.8\%$ when input signal is less than 14 $\mathrm{mV_{rms}}$

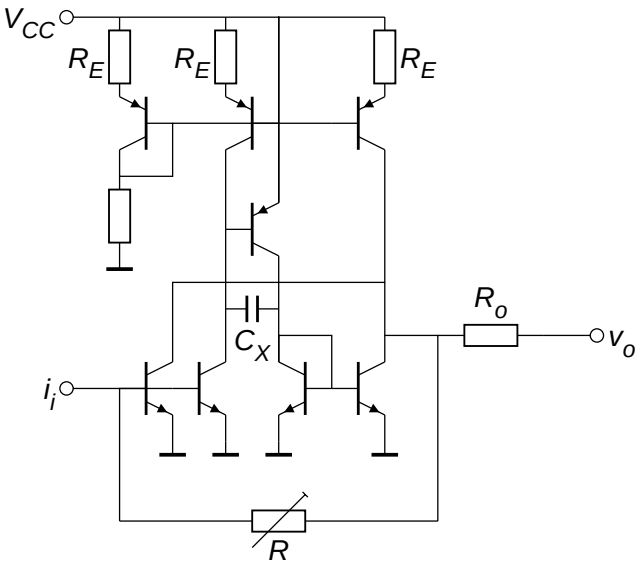

Figure 7.28: The pickup-coil preamplifier including its bias circuitry

Microphone preamplifier

- **input impedance**. The measured input impedance amounts to 63 kΩ. The difference between this value and our design aim of 50 kΩ is due to the relatively low value of the current gain factor β_F of the vertical PNP transistors in the semicustom process, which is about 40. This is also confirmed by simulations. Simulation of the input impedance of the microphone preamplifier using the model of the lateral PNP transistors that will be used in the fullcustom version ($\beta_F \approx 200$) of the front-end yields an input impedance of 52 kΩ, which is in good accordance with our design aim.

- **noise**. The input referred noise was calculated by measuring the spectral density of the noise current at the output of the front-end, dividing this spectrum by the measured transfer function of the front-end and multiplying the result by a polynome to obtain an A-weighted result. The input referred noise of the front-end amounts to 2.4 μV_{rms}. This is in accordance with simulations. When the input referred noise is simulated with lateral PNP transistors the result is 2.2 μV_{rms}, which is in good accordance with our design aim. As the rear-end of the hearing instrument operates in class-B, it is to be expected that its influence on the noise behavior of the total hearing instrument will not be noticeable.

- max. input signal:

  - 35 mV_{rms} unweighted for frequencies higher than 70 Hz

– 50 mV_{rms} unweighted for frequencies lower than 50 Hz

Pickup-coil preamplifier

- transfer: 5.4 – 55 kΩ
- input impedance (1 kHz): $< 400\ \Omega$
- output impedance (1 kHz): 4.0 – 4.7 kΩ
- bandwidth: > 100 kHz
- output noise (8 kHz): $< 2.7\ \mu V_{rms}$
- current consumption: $< 21\ \mu A$

Highpass filter

- order: 2 (real poles)
- cutoff frequency: 100 Hz – 1.5 kHz (linearly adjustable in octaves)
- stop-band attenuation: > 43 dB

Lowpass filter

- order: 2 (Butterworth characteristic)
- cutoff frequency: 1.5 kHz – 7.8 kHz (linearly adjustable in octaves)
- stop-band attenuation: > 27 dB

AGC-I

- attack time: 3.5 ms
- **release time: 55 ms**. The difference between this value and our design aim of 80 ms is again due to the relatively low value of the current gain factor β_F of the vertical PNP transistors. This causes a large error in the input-output relation of the gm-compensated current mirror in the envelope processor, which, in turn, has a dominant effect on the release time. However, simulations of the front-end with lateral PNP transistors yields a release time of 81 ms. Hence it is expected that the release time of the fullcustom version of the front-end will be in accordance with our design aim.
- knee level: 60 μV_{rms} – 35 mV_{rms} (linearly adjustable in dBs)
- compression ratio above knee level: 2

7.11 Fullcustom realization of the front-end

All the circuits, of both the front-end and the rear-end, have been realized on a single chip in a 2.5-μm BiCMOS process that contains vertical NPNs and PNPs as well as lateral PNPs. Unfortunately, at the time this thesis was about to be printed the test chip still had to be processed. For this reason no measurement results can be given here. The estimated chip area of the front-end amounts to 2.4 mm^2. For the total IC, including its bond pads, the chip area is about 5.1 mm^2.

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Chapter 8

Summary and conclusions

Nicht jedes Ende ist das Ziel.
Das Ende der Melodie ist nicht deren Ziel;
aber trotzdem: hat die Melodie ihr Ende nicht erreicht,
so hat sie auch ihr Ziel nicht erreicht.
Ein Gleichniss.

Friedrich Nietzsche: Menschliches, Allzumenschliches

This thesis deals with the design of low-voltage low-power analog integrated circuits and their applications in hearing instruments. Its purpose is twofold: to offer a design procedure for low-voltage low-power analog integrated circuits in general and to give a new concept of design for a hearing instrument.

Chapter 1 introduces the subject and in Chapter 2 it is shown that low-voltage low-power integrated circuits operate best in the current domain. Thus, the influence of the node capacitances, which are the main parasitics in low-power integrated circuits, can be reduced and indirect feedback, which is advantageous in a low-voltage environment, can be applied.

In Chapter 3, the derivation is given of three mathematical models that describe the terminal behavior of bipolar transistors in low-voltage low-power circuits with regard to their large-signal, small-signal and noise behavior.

Chapter 4 deals with the design of low-voltage low-power negative-feedback amplifiers. Two amplifier configurations, that have been considered to be especially suitable for low-voltage integrated circuits, have been examined: current amplifiers and transconductance amplifiers, both having an indirect output. For each amplifier type various quality aspects have been considered: noise, distortion, accuracy, bandwidth, output capability, power efficiency and integratability. It has been shown that a special variant of the current amplifiers, the scaling current amplifier, often is the best choice for realizing a real transfer function. As an

example, the final section discusses a microphone preamplifier for use in hearing instruments.

Chapter 5 deals with the design of low-voltage low-power automatic gain controls. Four different setups for realizing AGCs have been presented. All consisted of three elementary building blocks: a controlled current amplifier, a comparator and a voltage follower. Their design has been treated separately. As an example, the final section describes an automatic gain control for hearing instruments.

Chapter 6 is about the design of low-voltage low-power filters. It had appeared that, using conventional design methods, it was difficult, if not impossible, to control the cutoff frequency over a large range. To overcome this problem, two new integrators are introduced, both using a transconductance amplifier with an indirect output. As an example, the final section deals with a second-order highpass leapfrog filter.

The results of the foregoing three chapters have been combined in Chapter 7 in order to give the realization of a universally applicable analog integrated circuit for hearing instruments. This IC comprises the following functions: a microphone preamplifier, a pickup-coil preamplifier, a highpass filter and a lowpass filter, both with a controllable cutoff frequency, and an input-controlled automatic gain control with an adjustable knee level.

Acknowledgements

In working on a subject of both scientific and social importance, I have found myself in a luxurious position for a period of four years. However, it would not have been possible to bring this investigative expedition to a satisfying close without the help of many people in my technical and personal environment. There are a few people I would like to thank in particular.

First of all there are my 'promotor' Prof.dr.ir. Jan Davidse and my colleague Dr.ir. Albert van der Woerd, who spent great amounts of their time on proofreading the early versions of this thesis and on valuable discussions. I also thank Ir. Jeroen Kuenen and Rob van Beijnhem, the people of Philips Hearing Instruments, Ir. Bertus Geerdink, Ir. Han Hallie and Ir. Jos Leenen, and Ir. Jos Göbbels of Philips Semiconductors, Solid-State Special Products Group, who have always been willing to be of help. Rob van Beijnhem also made many breadboard and semicustom versions of the designs, thus paving the way to early detection of errors. Rob Janse prepared many of the drawings in this thesis, using his self-developed drawing program 'tekplot'. Wil Straver did the wire-bonding of the ICs and made several chip photos. Jacco Spaargaren printed the photographs of the AGC and the filter in Chapters 5 and 6, respectively. Cees Ruigrok designed the front cover. Ms. Jane Zaat-Jones corrected my numerous linguistic errors. Finally, there are my beloved wife Marjo and my son Jeroen. Without their support, not only in the technical field, this thesis would not have become what it is. To all I am greatly indebted.

Delft
February 1994
Wouter Serdijn

The Author

Wouter Serdijn was born in Zoetermeer, the Netherlands, on the 19$^{\text{th}}$ of March, 1966. He started his study at the Faculty of Electrical Engineering at the Delft University of Technology in 1984, and received his 'ingenieurs' (M.Sc.) degree in 1989. Subsequently, he did his Ph.D. research at the Electronics Research Laboratory of the same faculty.

Samenvatting

Dit proefschrift handelt over het ontwerpen van laagspannings-, laagvermogens-analoge geïntegreerde schakelingen en hun toepassingen in hoorapparaten. De doelstelling is tweeledig:

- het geven van een ontwerp-procedure voor laagspannings-, laagvermogens-analoge geïntegreerde schakelingen in het algemeen, en
- het geven van een nieuwe opzet voor een hoorapparaat.

Na de inleiding in hoofdstuk 1 wordt in hoofdstuk 2 aangetoond dat laagspannings-, laagvermogens-, geïntegreerde schakelingen het beste functioneren in het stroom-domein. Op deze manier kan de invloed van de knooppunts-capaciteiten, welke de belangrijkste parasieten vormen in laagvermogens- geïntegreerde schakelingen, worden verminderd en kan indirekte tegenkoppeling, wat voordelig is in een laagspannings-omgeving, worden toegepast.

In hoofdstuk 3 worden drie wiskundige modellen afgeleid, die het klem-gedrag van bipolaire transistoren in laagspannings-, laagvermogens-schakelingen beschrijven met betrekking tot, achtereenvolgens, hun groot-signaal, klein-signaal en ruis-gedrag.

Hoofdstuk 4 behandelt het ontwerpen van laagspannings-, laagvermogens- tegengekoppelde versterkers. Twee versterker-configuraties, welke zeer geschikt worden geacht voor laagspannings-, laagvermogens- geïntegreerde schakelingen, worden onderzocht: stroomversterkers en transconductantie-versterkers. Voor elk versterkertype worden diverse kwaliteitsaspecten beschouwd: ruis, vervorming, nauwkeurigheid, bandbreedte, uitstuurbaarheid, vermogens-rendement en integreerbaarheid. Het blijkt dat een speciale variant van de stroomversterkers, de schalende stroomversterker, in veel gevallen de beste keuze vormt voor het realiseren van een reële overdrachtsfunctie. In de laatste paragraaf wordt een praktisch voorbeeld beschreven: een microfoon-voorversterker voor toepassing in hoorapparaten.

Hoofdstuk 5 gaat over het ontwerpen van laagspannings-, laagvermogens- automatische versterkingsregelingen. Vier verschillende configuraties voor het realiseren van AVR's worden gepresenteerd. Alle bestaan uit drie elementaire bouwstenen: een geregelde stroomversterker, een comparator en een spanningsvolger. Hun ontwerp wordt afzonderlijk behandeld. Als praktisch voorbeeld beschrijft de laatste paragraaf een automatische versterkingsregeling voor hoorapparaten.

Hoofdstuk 6 beschrijft het ontwerpen van laagspannings-, laagvermogens-filters. Het blijkt dat, gebruik makend van conventionele ontwerp-methoden, het moeilijk is, zo niet onmogelijk, om de kantelfrequentie over een groot bereik te regelen. Om dit probleem te overwinnen worden twee nieuwe integratoren geïntroduceerd,

beide gebruik makend van een transconductantie-versterker met een indirekte uitgang. Als praktisch voorbeeld behandelt de laatste paragraaf een tweede-orde hoogdoorlaat leapfrog-filter.

In hoofdstuk 7 worden de resultaten van de voorgaande drie hoofdstukken gecombineerd teneinde een universeel toepasbaar analoge geïntegreerde schakeling voor hoorapparaten te realiseren. Dit IC bevat de volgende funkties: een microfoon-voorversterker, een luisterspoel-voorversterker, een hoogdoorlaat-filter en een laagdoorlaat-filter, beide met een regelbare kantelfrequentie, en een ingangsgeregelde automatische versterkingsregeling met een instelbaar kniepunt.

Abstract

Low-voltage low-power analog integrated circuits are applied in the area of battery-operated systems. They are of crucial importance for implantable and injectable devices, such as pacemakers, blood-flow meters and auditory stimulators, but they can also be found in portable radios, hand-carried radiotelephones, pagers and hearing instruments.

This book discusses the design of analog integrated circuits in a low-voltage low-power environment, following a systematic approach. Subsequently attention is paid to low-voltage low-power electronics from a network-theoretical point of view, modeling of the devices in a low-voltage low-power environment and the design of various functional blocks: amplifiers, automatic gain controls and filters. These three functions are the main functions that can be found in a hearing instrument. Their application in a universally applicable IC for hearing instruments and its realization in silicon is treated separately.