800MHz Voltage-Controlled Oscillator with 6dB Phase-Noise Tuning Range

Aleksandar Tasić, Wouter A. Serdijn and John R. Long

Abstract - **An 800MHz adaptive voltage-controlled oscillator is designed for a maximal phase-noise tuning range of 6dB with a factor three saving in power consumption. Operating from a 3V supply, it achieves better than –136dBc/Hz phase noise at 10MHz offset from the 800MHz oscillating frequency at a current consumption level of 5mA, and phase noise of –130dBc/Hz at 10MHz offset from the 800MHz oscillating frequency at a current consumption level of 1.7mA. For a 3V tuning voltage, a frequency tuning range of 120MHz, from 715MHz and 835MHz, is achieved.**

Keywords – **voltage-controlled oscillators, adaptive circuits, RF circuits, analog circuits, low power IC design.**

I. INTRODUCTION

Single-mode, single-standard oscillators are conventionally designed to satisfy the most stringent conditions, having all the performance and circuit parameters fixed. As in portable devices the oscillators are exposed to such conditions only for a short period of time during operation, this (over)design for worst case condition turns out to be rather expensive in terms of power.

Therefore an adaptive voltage-controlled oscillator (VCO) has been designed that can trade performance, i.e., phase noise, for power consumption and thereby allows for adaptation to a varying radio-channel conditions. The presented 800MHz adaptive VCO is designed for a maximal phase-noise tuning range of *PNTR*=6dB, with up to three times saving in power consumption. Operating from a 3V supply, a frequency tuning range of 120MHz, from 715MHz and 835MHz, is measured.

The organization of the paper is as follows. The design procedure of an adaptive voltage-controlled oscillator is outlined in Section II. Measurement results are discussed in Section III, and conclusions are summarized in Section IV.

II. VCO DESIGN

The quasi-tapped voltage-controlled oscillator [1], shown in Fig. 1, consists of a resonating LC tank, two capacitive voltage dividers and a cross-coupled transconductance amplifier as the active part. Here, L stands for the tank inductance, C_V for the varactor capacitance, C_A and C_B for the quasi-tapping capacitances and R_D for the tail-current source degenerative resistance.

The relation between the parameters of the oscillator can be summarized as:

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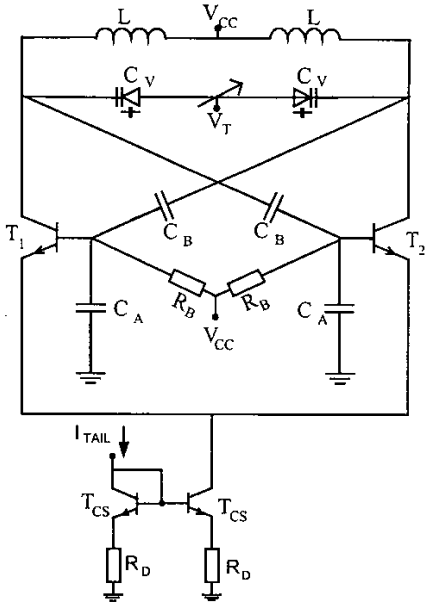

Fig. 1 Quasi-tapped LC-oscillator.

$$G_{TK} = \frac{R_L}{(\omega_0 L)^2} + R_C(\omega_0 C)^2 \quad (1)$$

$$n = 1 + \frac{C_A}{C_B}, \quad G_M = g_m/2, \quad G_{M,TK} = G_M/n \quad (2)$$

$$L_{TOT} = L, \quad C_{TOT} = C + \frac{C_A C_B}{C_A + C_B}, \quad \omega_0 = \frac{1}{\sqrt{L_{TOT} C_{TOT}}} \quad (3)$$

R_L and R_C stand for the inductor L and the varactor C series loss resistances, G_{TK} the effective tank conductance, n is the quasi-tapping factor, $-G_M$ the transconductance of the active part of the oscillator, $-G_{M,TK}$ the conductance seen by the LC-tank and g_m the transconductance of the bipolar transistors.

A. Phase-Noise Tuning

By trading phase noise for power consumption, oscillators and oscillating systems allow for adaptation by, e.g., physical layer resource manager (PLRM), to varying channel conditions, still complying with the requirements of the complete RF front-end system. Referred to as a *phase-noise tuning* [2], this concept explicitly shows how phase-noise and power consumption trade between each other in an adaptive way.

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Selection of the design parameters of an adaptive oscillator is quite different from a design procedure of a fixed oscillator. Therefore, the design procedure of an adaptive voltage-controlled oscillator is outlined in the remainder of this section.

Let us first determine the range of phase-noise tunability for the oscillator under consideration.

Relating phase noise to loop gain (k) as [2]:

$$\mathcal{L}_{QT}(k) \propto \frac{1+n\cdot(k/2+r_B g_{ms-up,QT})}{k^2 n^2} \quad (4)$$

the *phase-noise tuning range* $PNTR(k_1,k_2)$ for a k_2/k_1-times change in power consumption can be defined as [2]:

$$PNTR(k_1,k_2)=\frac{\mathcal{L}_{QT}(k_1)}{\mathcal{L}_{QT}(k_2)}=\frac{k_2^2}{k_1^2}\frac{1+n(k_1/2+c')}{1+n(k_2/2+c')} \quad (5)$$

where c' is a positive constant equal to $c'=r_B\, g_{ms-up}$, with r_B and g_{ms-up} being the base resistance and start-up (k=1) transconductance of the active part transistors and $\mathcal{L}$ phase noise of the oscillator.

If the safety start-up condition corresponds to k_{MIN}=2, in order to calculate the achievable phase noise tuning range, for the oscillator under consideration, the loop gain k_{MAX}, corresponding to the best phase noise, will be determined first. Both phase noise and loop gain are controlled by means of tail current I_{TAIL}, indicated in Fig. 1.

For a maximum voltage swing across the LC tank [3]

$$V_{S,MAX} \le \frac{2n}{n+1}(V_{BE}-V_{CE,SAT}) \quad (6)$$

the detrimental effects of both hard saturation of the transistors in the active part of the oscillator and additional current noise of their forward biased base-collector junctions can be circumvented [4]. Here, V_{BE}=0.75V is the base-emitter voltage of the transistors in the active part and $V_{CE,SAT}$ their collector-emitter saturation voltage. As the bases of the transistors are at the maximum supply voltage, the maximum voltage swing across the LC tank ($V_{CE,SAT}$=0V) equals $V_{S,MAX1}=1.5n/(n+1)$. On the other hand, the maximum voltage swing corresponding to the non-saturation condition ($V_{CE,SAT}$=0.3V) is $V_{S,MAX2}=0.9n/(n+1)$. Compromising between larger voltage swing, on one hand, and weaker saturation, on the other hand, we opt for a maximum voltage swing across the tank of $V_{S,MAX}=(V_{S,MAX1}+V_{S,MAX2})/2$.

Now, relating the voltage swing across the LC-tank as:

$$V_S=\frac{8}{\pi}nkV_T \quad (4)$$

the maximal loop-gain value, derived from the condition $V_S=V_{S,MAX}$ and n=2, is found to be k_{MAX}=6. V_T is thermal voltage, approximately equal to 26mV at room temperature.

For example, if k_{MIN}=2 (the safety start-up condition), and k_{MAX}=6 (expected best phase noise), r_B=40Ω and g_{ms-up}=8.2mS, the control ranges of the power consumption and the phase noise, both for a quasi-tapping factor n=2, are respectively:

$$P_{MAX}/P_{MIN}=k_{MAX}/k_{MIN}=3$$

$$PNTR(2,6)=\mathcal{L}_{MIN}/\mathcal{L}_{MAX}=6.3dB$$

where P_{MAX} and P_{MIN} stand for maximum and minimum power consumption, and $\mathcal{L}_{MAX}$ and $\mathcal{L}_{MIN}$ represent the maximum and minimum phase noise corresponding to the values of k_{MAX} and k_{MIN}, respectively.

The phase-noise tuning range of 6dB is the maximum achievable tuning range for the bipolar voltage-controlled oscillator, shown in Fig. 1.

B. VCO Design Parameters

For a quasi-tapping ratio of n=2, the quasi-tapping capacitances C_A=1pF and $C_\Pi+C_B$=1pF have been chosen, C_Π being the base-emitter junction capacitance of the devices T_1 and T_2 in Fig 1. The transistors achieve a maximum transit frequency of f_T=8GHz in this technology.

For the variable capacitor (varactor), a reverse biased base-collector junction of the transistors has been employed. The quality factor (Q) of the varactor is estimated at 15 from simulations.

Optimised for low-power operation, a rather large inductance value of 12nH is chosen, laid-out in 1um thick second metal layer, resulting in the quality factor of 2 at the operating frequency of 800MHz. Such a low Q is a result of the very low, 6 Ωcm substrate resistivity, low frequency and thin, top (second) metal close to the substrate. The 6.25-turn inductor's outer diameter is d_{OUT}=360um, its metal width w=18.5um and its metal spacing s=1um.

The equivalent lumped element model of the on-chip spiral inductor is shown in Fig. 2. The coil is modelled with an ideal inductance L, a series resistance R_L, representing the losses in the coil, and an inter-winding capacitance C_L. The oxide capacitance between the spiral and the silicon substrate is modelled by C_{OX}. Representing the RF signal flow through the silicon substrate, the substrate resistance and capacitance R_{SUB} and C_{SUB} are added as well.

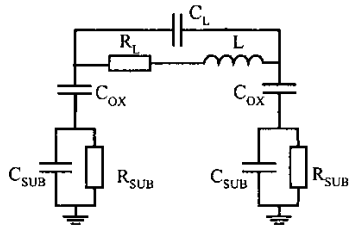

Fig. 2 Lumped-element model of spiral inductor on silicon.

The model parameters are estimated with the aid of the *phase-noise-inductance (PNL)* simulator [5], and shown in Table I.

Parameter	Value
L	12nH
R_L	18 Ω
C_L	80fF
C_{OX}	0.8pF
C_{SUB}	40fF
R_{SUB}	150 Ω

Table I. Integrated inductor model parameters.

As an interfacing stage between the VCO and measurement equipment, a two-stage common collector buffer has been designed. Its current consumption is 2mA.

Even though no commercially available field-solvers were used for the estimation of the on chip inductors, a rather good match is obtained between results predicted by calculations and the simulations on one hand and the measurement results on the other hand, emphasizing the merit of the undertaken design procedure. The sizing of the oscillator parameters and determining its performance has also been done with the aid of the *PNL* simulator.

III. Measurement Results

The chip micrograph is shown in Figure 3. It occupies an area of 1mm^2, including bondpads. Wire-bonded on a 20-lead package, it is placed in a metal test fixture, shown in Fig. 4. All measurements have been performed with an Agilent E4446A spectrum analyser.

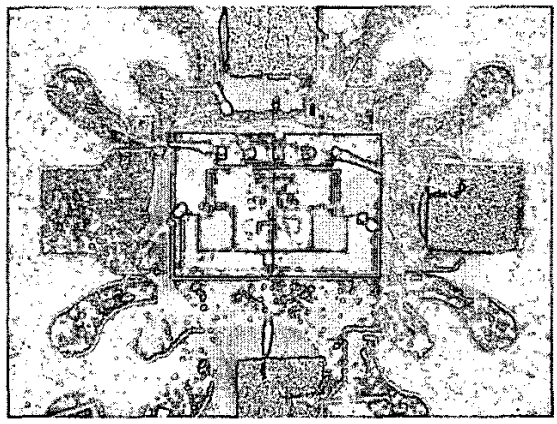

Fig. 3 The 800MHz VCO chip micrograph.

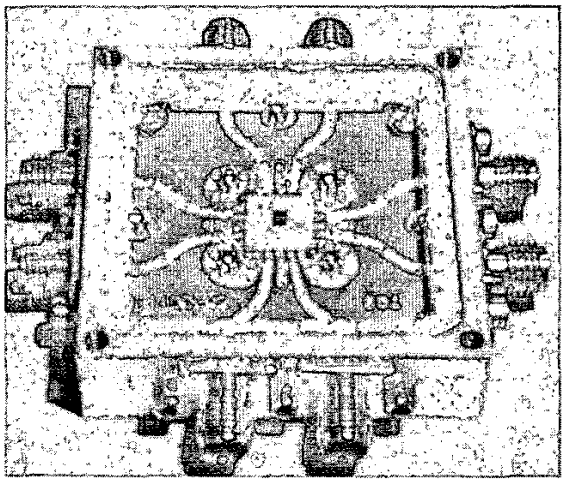

Fig. 4 Packaged VCO in test fixture.

For a 3V tuning voltage, the frequency tuning range of 120MHz, between 715MHz and 835MHz, is achieved. The measured frequency tuning range is shown in Fig. 5.

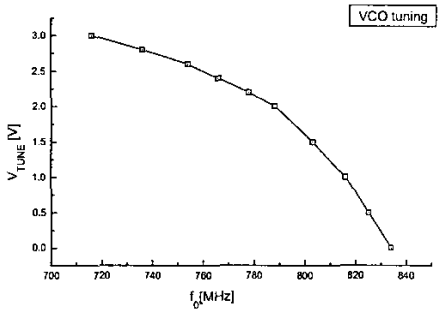

Fig. 5 Frequency tuning of the VCO.

Using 8GHz technology device parameters, the VCO achieves a phase noise of –135.8dBc/Hz at 10MHz offset frequency from the 800MHz oscillating frequency at a current consumption level of 5mA, and a phase noise of –128.6dBc/Hz at 10MHz offset from the 800MHz oscillating frequency at a current consumption level of 1.5mA. The plots of the maximal and the minimal phase noise are shown in Fig. 6. The achieved phase-noise tuning range of 7dB is for a factor 3.3 change in power consumption.

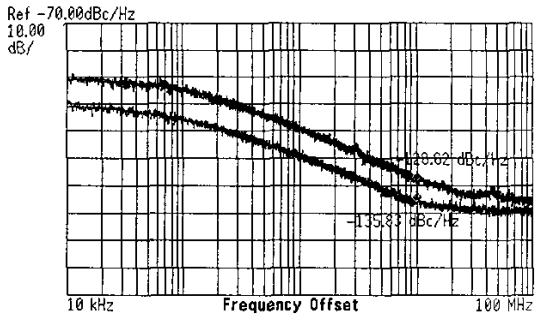

Fig. 6 Maximum and minimum phase noise at 10MHz offset from 800MHz oscillating frequency at 5mA and 1.5mA tail current, respectively.

The need for frequency-transconductance tuning [6] can be observed by measuring the spectrum of the oscillator's output signal, as depicted in Fig. 7. Here, the oscillator is tuned to the resonant frequency f_1=800MHz at a tail-current level I_{TAIL}=2.5mA. The measured signal power is –19dBm, corresponding to a loop gain of around k=3. By tuning the resonant frequency to f_2=740MHz the oscillating signal output power changes to –26dBm, and the oscillator's loop gain to k=1. Any further reduction in frequency, at the same power consumption level, results in a disappearance of the oscillations as the oscillating condition is violated, i.e., loop gain k<1. This is shown in Fig. 7 at left.

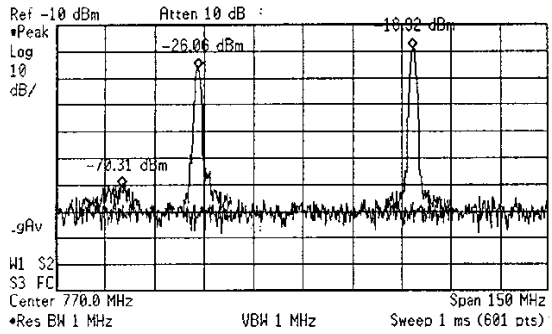

Fig. 7 Frequency-transconductance tuning from 800MHz to 715MHz oscillating frequency at 2.5mA tail current.

The oscillator performance parameters accompanying Fig. 7 are given in Table II.

frequency	*signal power*	*loop gain*
800MHz	-19dBm	3
740MHz	-26dBm	1
715MHz	-70dBm	<1

Table II. VCO Performance at I_{TAIL}=2.5mA.

IV. Conclusions

In single-standard applications, the adaptivity can be utilized as *power saving mechanism*, thereby enhancing the overall RF system performance.

Accordingly, an 800MHz adaptive voltage controlled oscillator has been designed for phase-noise tuning range of 6dB and a factor three saving in power consumption.

Acknowledgements

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