



A 0.5-V, 2-nW, 55-dB DR, fourth-order bandpass filter using single branch biquads: An efficient design for FoM enhancement

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ARTICLE INFO

Article history:

Received 18 February 2013

Received in revised form

22 December 2013

Accepted 2 January 2014

Available online 23 January 2014

Keywords:

Analog filter

Bandpass filter

Bionic ear processor

Biomedical circuit

CMOS circuit

G_m -C filter

Low voltage

Ultra low-power

ABSTRACT

A compact nano-power fourth-order bandpass filter operating from a 0.5 V supply, with an adjustable center frequency ranging from 125 Hz to 16 kHz, is presented. The filter is constituted from cascaded second-order circuit cells that are realized by a network of three transistors and two capacitors comprising only one branch of bias current. The measurement results of the filter fabricated in a 0.18- μm CMOS IC process indicate that, for a 1 kHz center frequency, a dynamic range of 55 dB is obtained from 2 nW power consumption. These results lead to best figure of merit achieved when compared to other existing designs to date.

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1. Introduction

Analog filters are indispensable circuit building blocks in electronic systems. They separate desired signals from other signals and noise by making use of differences in their energy frequency spectra. In order to be able to compare various filters a 'figure of merit (FoM)' that combines several circuits or signal parameters in a certain formula is helpful. Adapting the concept of minimum possible energy per cycle and per pole [1] to the design of a bandpass filter (BPF) circuit, the BPF's FoM can be defined by

$$\text{FoM} = \frac{P}{Nf_c \text{DR}} \quad (1)$$

where P , N , f_c , and DR are the power consumption, filter order, center frequency and dynamic range of the filter, respectively. It is quite straightforward that the cost (numerator) over the performance (denominator) should be as low as possible. This suggests that to enhance the FoM, the following conditions need to be met.

- 1) The filter topology should contain a minimum number of active (noisy) elements per time-constant.

- 2) The filter circuit should contain the least amount of current branches and operate from a very low supply voltage (V_{DD}) for a given N , f_c and DR.

For the FoM of biomedical BPF designs that have a low center frequency (audio range and below) and a power consumption less than 1 μW [2–6], V_{DD} has been added into the numerator of Eq. (1) [3]. As a consequence, V_{DD} is accounted for twice and becomes the most important factor in this modified definition. Although it has been commonly used in recently reported BPFs [4–6], as reducing V_{DD} is considered a virtue, the fundamental basis of this modified FoM is questionable. In this work, we thus consider the definition of Eq. (1) [1] instead of the FoM introduced in [3].

Fig. 1 shows a FoM plot versus V_{DD} using Eq. (1) of various biomedical BPFs collected from 2003 to 2012 [2–6]. The second best BPF is the design presented in [2]. Its topology satisfies the first condition for enhancing FoM (more details on the filter topology are given in Section 3). The worst FoM belongs to the BPF introduced in [4]. This is because the design of [4] uses a state-space filter topology that requires many G_m cells to realize both feed-forward and feedback filter coefficients and integrators. Obviously, this violates Condition no. 1. The BPFs introduced in [3,6] use very similar filter topologies (based on element substitution of a passive LC ladder prototype) and provide almost the same FoMs (0.89×10^{-13} and 1×10^{-13} , respectively). These numbers show a considerable FoM improvement with respect to the design

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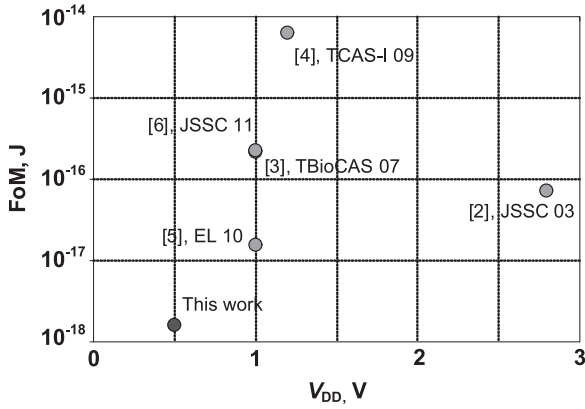


Fig. 1. Figure of merit comparison of G_m -C bandpass filters collected over 2003–2012 and this work.

of [4], but are still worse than that of [2]. The reason for this is that substituting one floating inductor in G_m -C filters requires $4G_m$ cells and a grounded capacitor. Although the number of active elements is less than that required in the state-space filter of [4], this is not in line with Condition 1, either. A significant improvement can be seen for the filter presented in [5], for which almost an order of magnitude improvement with respect to the filter of [2] is achieved. This design uses the same filter topology as used in [2] and, at transistor level, adopts a compact power efficient G_m -C biquad structure that requires only two branches of current consumption from [7]. It can be said that, in this design, the conditions for FoM enhancement have almost been fulfilled. However, since the filter topologies used in [2,5] require a voltage follower circuit to prevent any loading effect and the transistor circuit of the biquad section used in [5,7] cannot be operated at a very low V_{DD} , there is still a possibility for the FoM to be enhanced further.

In this paper, within the context of low-frequency integrated filters for biomedical applications, for which very large resistors would occupy a too large chip area and would be severely limited in bandwidth, we develop further the G_m -C BPF topology to achieve a significant FoM improvement by proposing the following:

- **Macro-model:** a low-voltage second-order filter topology that has a minimum number of active (noisy) elements and can be cascaded without the expense of a voltage buffer.
- **Transistor-level circuit:** a low-voltage power-efficient single branch circuit structure using a single transistor as a G_m cell that can be fitted into the filter topology mentioned above.

By doing so, a fourth-order BPF with FoM improvement can be successfully realized. The measurement results of the proposed BPF fabricated in AMS' 0.18- μ m CMOS technology confirm our concept.

It should be noted also that, as a consequence of the approach taken, there are two possible disadvantages of this method: 1) the filter's linearity is limited, resulting in a maximum signal swing of a few milli-volts; 2) the BPF's quality factor is limited to a maximum value of 0.5. However, these limitations do not prevent this filter from being applied in various biomedical applications, such as a filter for cochlear implant speech processing [2,10,11]. Parts of this work's (i.e., the basic concept and some circuit simulations) results have been reported previously in [8]. A more detailed performance analysis and measurement results are presented here.

In the next section, Section 2, the proposed idea of realizing filtering functions from a single branch circuit structure and their performance is discussed. The proposed BPF design, including

details on the filter topology selection, transistor level architectures, and common-mode behavior, is presented in Section 3. Section 4 presents measurement results and a detailed comparison with previously published designs. Conclusions are given in the last section.

2. Single branch filters

To achieve a compact power efficient circuit structure, this section explores the feasibility to realize continuous-time filters from circuit structures capable of operating from a supply voltage of less than two gate-source voltages (V_{GS}) plus one saturation voltage (V_{DSsat}) and employing only one branch of bias current.

2.1. Filter topologies using feedback transconductors

For a MOSFET that is properly biased in weak inversion saturation, a differential g_m cell connected in a negative feedback fashion as shown in Fig. 2 can be obtained from the small signal operation of the transistor. To get rid of the body effect, a pMOS device is preferred in an n-well CMOS process. Biased by a DC current I_B , the transconductance of the transistor with zero V_{BS} (bulk and source terminals are connected) and neglecting channel length modulation is given by

$$g_m = \frac{I_B}{nU_T}, \quad (2)$$

where n and U_T represent the sub-threshold slope factor and the thermal voltage, respectively [9]. Using this macro-model, several filter topologies can be found from circuit structures with a single branch bias current.

Fig. 3 shows possible realizations of single-branch G_m -C filters. An LP filter can be obtained from the circuits in Fig. 3(a) and (b): an HP filter (from the former) and a bandpass (BP) filter (from the latter). The circuits in Fig. 3 are all formed by a cascade connection of transistors M_1 and M_2 and capacitors between source and AC ground terminals. Both transistors share the same bias current I_B . Replacing M_1 and M_2 by the macro-model of Fig. 2 results in the small signal macro-model shown in Fig. 4. Using this model we can straightforwardly analyze that

$$H_{LP}(s) = \frac{V_{LP}(s)}{V_{in}(s)} = \frac{1}{1 + s(C_1/g_{m1})}. \quad (3)$$

Without capacitor C_2 , we obtain the following HP transfer function:

$$H_{HP}(s) = \frac{V_{HP}(s)}{V_{in}(s)} = \frac{-s(C_1/g_{m2})}{1 + s(C_1/g_{m1})}. \quad (4)$$

By adding C_2 to the former HP output node, the following BP transfer function can be achieved:

$$H_{BP}(s) = \frac{V_{BP}(s)}{V_{in}(s)} = \frac{-s(C_1/g_{m2})}{(1 + s(C_1/g_{m1}))(1 + s(C_2/g_{m2}))}. \quad (5)$$

It can be seen that there are three filter topologies obtained from this single branch structure. Apart from the low current consumption, another advantage of these filters is that they feature a high impedance input node (being the gate of M_1). As a

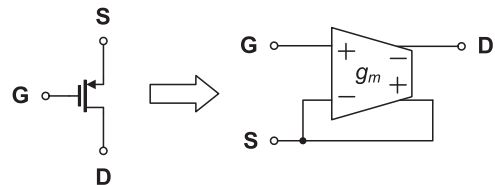


Fig. 2. Single transistor and its macro-model.

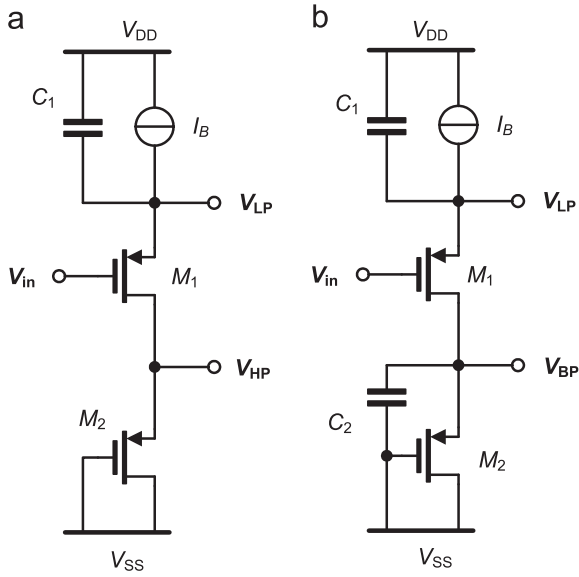


Fig. 3. Single branch filter circuits. (a) First-order LP and HP filters. (b) First-order LP and second-order BP filters.

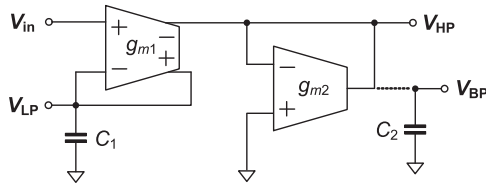


Fig. 4. Single branch filter small signal models.

result, there is no severe loading effect for cascade connections of these filters assuming that the gate–source parasitic capacitance of \$M_1\$ (\$C_{GS1}\$) is sufficiently small.

Since the filters are operating in weak inversion saturation and the cutoff frequency can be adjusted by the value of \$g_m\$, which is proportional to \$I_B\$ in weak inversion saturation, a wide tuning range of the filter's cutoff frequency via controlling \$I_B\$ can be expected.

2.2. Supply voltage requirement and current consumption

Considering the circuits in Fig. 3(b) in conjunction with its transfer function obtained in Eq. (5), a current consumption of \$0.5I_B\$ per filter order is obtained. To create proper bias points in weak inversion saturation, supply voltage \$V_{DD}\$ and common mode level \$V_{CM}\$ should be considered. For the stacked circuit shown in Fig. 3 and setting \$V_{SS}=0\$ V, the supply voltage required must be at least \$V_{DD} = V_{inpp} + V_{SG} + 2V_{SDsat}\$ (assuming that \$I_B\$ requires one \$V_{SDsat}\$). This can be re-arranged to

$$V_{DD} \cong V_{inpp} + U_T \left(8 + n \ln \left(\frac{I_B}{I_{D0}} \right) \right), \quad (6)$$

where \$I_{D0}\$ and \$V_{inpp}\$ are the zero bias current of the transistors and input (peak to peak) voltage swing, respectively.

It can be seen from Eq. (6) that there are a fixed term of \$8U_T \cong 200\$ mV and a bias current related term. The latter term is directly related to the cutoff frequency of the filter. In the case of cascading HP and BP filters, to maintain the same signal swing range for all cascaded stages, \$V_{CM}\$ of each stage should be equal to

$$V_{CM} = V_{SS} + V_{SG2}. \quad (7)$$

This condition of \$V_{CM}\$ creates a new requirement for \$V_{DD}\$ to be at least \$2V_{SG} + V_{SDsat}\$ or in a form similar to Eq. (6)

$$V_{DD} \cong V_{inpp} + U_T \left(2 + n \ln \left(\frac{I_B}{I_{D0}} \right) \right). \quad (8)$$

In this extremely low-power design context, \$I_B\$ in the range of 0.1–10 nA is used to accommodate cutoff frequencies ranging from 100 Hz to 10 kHz. Therefore, either Eq. (6) or (8) can be higher and the highest one is the minimally required \$V_{DD}\$ for the cascaded stage. For the 0.18-μm CMOS technology used in this work, \$I_{D0} \cong 230\$ pA and \$n \cong 1.6\$ is obtained for \$W/L=10\$. Fig. 5 shows a detail of the required \$V_{DD}\$ for \$V_{inpp}=25\$ mV and different values of \$I_B\$ according to Eq. (6) and (8). The gray line indicates the level of \$V_{DD}\$ required. For \$I_B\$ less than 3 nA, Eq. (6) defines \$V_{DD}\$, which can be set as low as 0.2 V at \$I_B=0.1\$ nA. For \$I_B\$ greater than 3 nA, \$V_{DD}\$ is defined by Eq. (8). From this plot, \$V_{DD}=0.5\$ V is confirmed to be sufficient for the whole range of \$I_B\$.

On the other hand, any cascade connection that uses the LP filter increases the required \$V_{DD}\$ as the output is taken from the source terminal and the input is applied at the gate terminal, unless a complementary (nMOS) version of the single branch LP filter is applied [6]. This will make either the required \$V_{DD}\$ eventually exceed the available supply voltage or the filter suffer from the body effect. Another way to solve this problem is using a level shifter as an interface block to shift down the source voltage of \$M_1\$ before cascading the next stage of LPF, thereby maintaining the same required \$V_{DD}\$. This, however, leads to more power consumption and more noise contribution. For this reason, the LP filter will be, from now on, no longer considered.

2.3. Noise

Fig. 6(a) shows a single branch BPF biquad circuit and its noise sources. In practice, \$I_B\$ can be formed by a single transistor with its biased gate terminal \$M_B\$. Assuming here that, for simplicity, \$V_B\$ is noiseless, each transistor is sized large enough and its drain current is low enough to keep the \$1/f\$ noise corner frequency lower than the frequency of interest, the transistor's weak inversion noise behavior will be dominated by its shot noise. Equivalent current noises \$i_{nB}\$, \$i_{n1}\$ and \$i_{n2}\$ will have the same power spectral density of \$S_{ini}=2qI_B\$ [9].

Fig. 6(b) illustrates a simplified equivalent model for the noise calculation that realistically assumes the drain–source conductance of each transistor is negligible when compared to its \$g_m\$. First noise currents \$i_{nB}\$ and \$i_{n1}\$ are combined and flow through the LP network comprising \$C_1\$ and \$R_1 (=g_{m1}^{-1})\$. The resulting noise voltage will be converted into output current noise by \$g_{m1}\$ and will

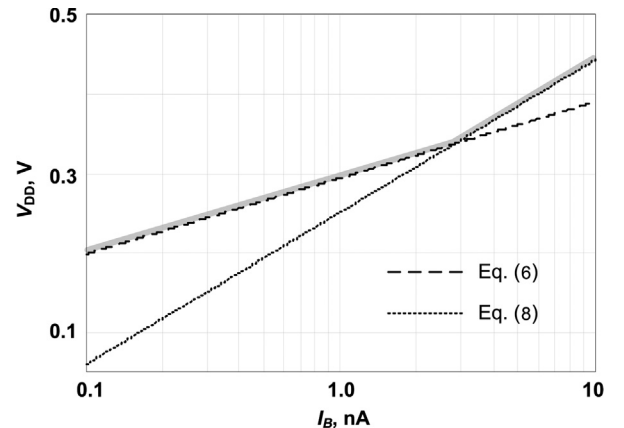


Fig. 5. Supply voltage requirement for different bias currents.

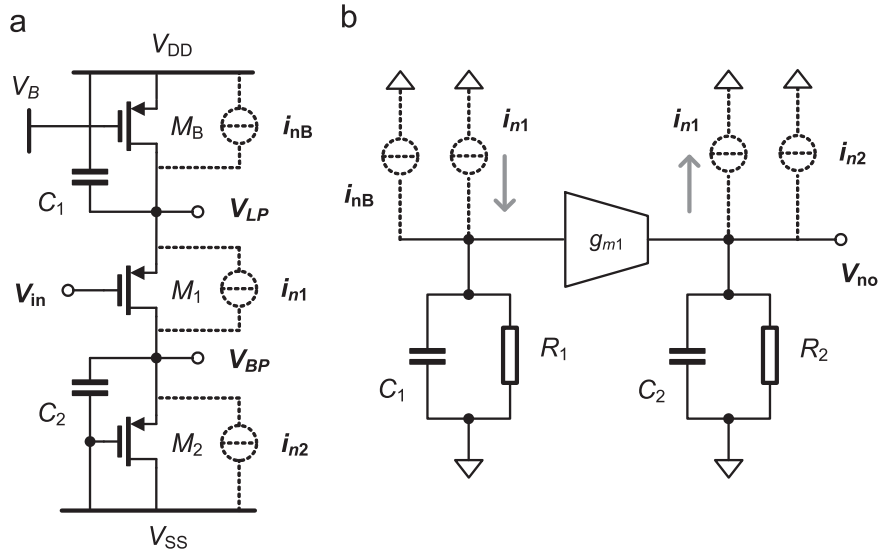


Fig. 6. BPF with noise sources. (a) Transistor circuit. (b) Equivalent model.

combine with $-i_{n1}$ and i_{n2} and together flow through another LP network, C_2 and R_2 ($=g_{m2}^{-1}$). Subsequently, output noise voltage v_{no} appears at the output port. Note that the current noise of M_1 appears at both the input and the output ports of g_{m1} (i_{n1} and $-i_{n1}$, respectively), leading to two current sources that are fully correlated.

Following the aforementioned mechanism, for $g_{m1}=g_{m2}$, an average output noise power can be found from

$$\overline{v_{no}^2} = \int_0^\infty (S_{inB}|H_B(s)|^2 + S_{in2}|H_2(s)|^2 + S_{in1}|H_1(s)|^2) df, \quad (9.1)$$

where

$$H_B(s) = \frac{g_{m2}^{-1}}{D(s)} = \frac{g_{m2}^{-1}}{1 + s((C_1/g_{m1}) + (C_2/g_{m2})) + s^2(C_1C_2/g_{m1}g_{m2})}, \quad (9.2)$$

$$H_2(s) = \frac{g_{m2}^{-1}}{1 + s(C_2/g_{m2})}, \quad (9.3)$$

and

$$H_1(s) = H_B(s) - H_2(s) = \frac{-s(C_1/g_{m1}g_{m2})}{D(s)}, \quad (9.4)$$

After some mathematical rearrangement this results in $\overline{v_{no}^2} = nkT/C_2$.

Note that Eq. (9) can be applied to the HP filter of Fig. 3(a) by replacing C_2 with the gate-source parasitic capacitance of M_2 (C_{GS2}) since C_{GS2} will bypass the output voltage to ground at very high frequencies eventually forming a BP response.

3. Proposed BPF design

3.1. Filter topology considerations

Fig. 7(a) shows the fourth-order BPF topology used in [2,5]. It is composed of two identical second-order sections connected in cascade. Capacitor C_1 with transconductor G_{m1} and capacitor C_2 with G_{m2} form the HP and LP cutoff frequencies of each second-order section, respectively. To prevent any loading effect induced by the input impedance of the subsequent stage, a voltage follower is inserted. This leads to more chip area and power consumption. In this work, we develop further from this structure instead of the structures used in [3,4,6] because this

topology has a small number of active and noisy elements (G_{ms}) per noiseless elements (Cs). Therefore, minimum noise contribution and minimum power consumption can be expected from this topology. In order to further enhance the filter's FoM, we need to get rid of the voltage buffer by looking for a cascable filter topology and implement the filter using a very low-power compact circuit.

The proposed BPF biquad section in Fig. 4 is well compatible with the above requirement. Fig. 7(b) shows the single-ended fourth-order BPF constituted by the two identical G_m -C biquad sections proposed. More detail on the transfer function of each proposed biquad section can be found by rearranging Eq. (5) to

$$H_{BP}(s) = \frac{-s(G_{m1}/C_2)}{s^2 + s((G_{m2}/C_2) + (G_{m1}/C_1)) + s^2(G_{m1}G_{m2}/C_1C_2)}. \quad (10)$$

For $G_{m1} = G_{m2} = G_m$ we have

$$\omega_0 = \frac{G_m}{\sqrt{C_1C_2}}, \quad Q = \frac{\sqrt{C_1C_2}}{C_1 + C_2}, \quad K = \frac{C_1}{(C_2 + C_1)}, \quad (11)$$

where parameters ω_0 , Q and K stand for the center frequency, the quality factor and the mid-band gain, respectively. As this structure has a high-impedance input port, the cascade connection for higher order realization does not need an additional buffer circuit.

Unfortunately, this topology can only realize real poles and, as a consequence, its maximum value of Q is limited to 0.5. To achieve higher quality factors, additional circuit elements and power consumption are thus required. However, for a plethora of biomedical applications, e.g., in cochlear implant channels that require very low power consumption and electronic adjustability, this low value of Q is acceptable [2,10].

3.2. Transistor level realization

At transistor level, the filter topology in Fig. 7(b) can be directly formed by using the single branch BPF of Fig. 3(b) to implement the second-order sections. The filter's center frequency can be linearly adjusted by adjusting bias current I_B . Transistors M_1 and M_2 are acting as G_{m1} and G_{m2} , respectively. Note that, according to the exponential characteristic of a MOSFET operating in weak inversion saturation, the equivalent operation of the proposed filter topology and the circuit is valid only for the small signal condition. As a consequence, a

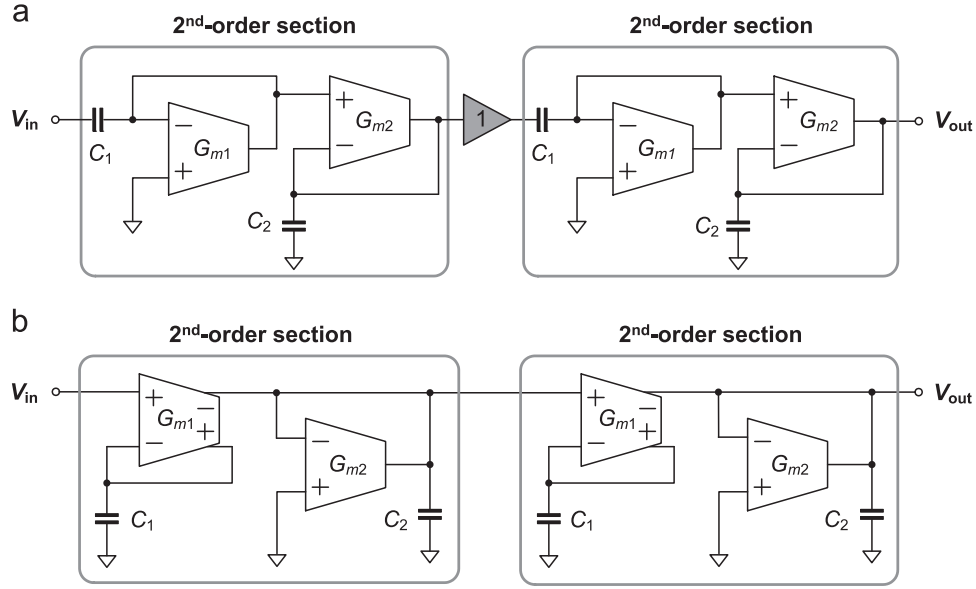


Fig. 7. Cascaded fourth-order BPFs. (a) Topology of [1]. (b) Topology used in this work.

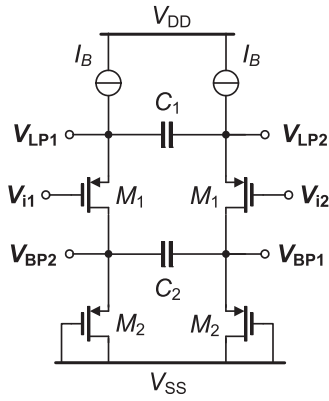


Fig. 8. Differential version of the single branch BPF.

differential structure as shown in Fig. 8 is required to reduce the filter's nonlinearity and thereby maximize its dynamic range. The output average noise power defined in Section 2.3 will double here as well as the differential signal voltage swing. In this case bias current I_B defines the transconductance

$$g_{m1} = \frac{G_{m1}}{2} = g_{m2} = \frac{G_{m2}}{2} = \frac{I_B}{nU_T}. \quad (12)$$

In line with Eq. (11), ω_o is linearly adjustable by I_B .

3.3. Common-mode behavior

It is interesting to analyze the common-mode behavior of the differential circuit in Fig. 8 that provides two filtering functions. For the LPF, the output voltages are taken from the source terminals of the circuit configured as source followers. In the pass-band the output voltages will follow the input voltages regardless whether differential mode or common mode signals are applied. There is no common rejection at all here.

On the other hand, the output voltages of the BPF are taken from the drain terminals of M_1 and as a result, high common-mode rejection capability can be expected. Theoretically, under the condition that each current source I_B has infinite output

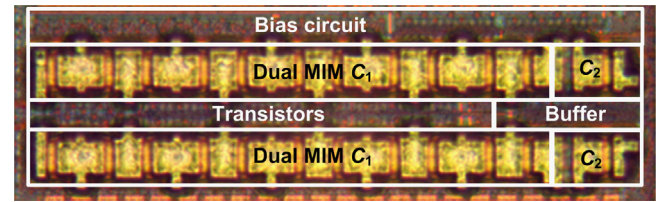


Fig. 9. Chip photo.

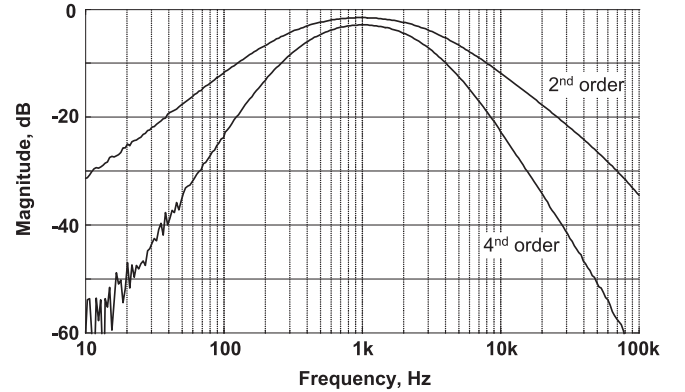


Fig. 10. Magnitude responses of the proposed BPFs.

impedance and neglecting the channel length modulation effect of M_1 , the output common-mode and differential mode signal will be completely isolated, thus featuring an infinite common-mode rejection ratio.

In practice, a low-frequency common-mode gain of this circuit can be found for the case that M_1 and M_2 are perfectly matched, which equals $A_{CM} \cong -g_{oc}g_{m2}^{-1}$, where g_{oc} represents the output conductance of current source I_B . Enhancement of the common-mode rejection ratio (CMRR) can be done by improving the output impedance of I_B . Besides, taking into account mismatches between transistor pairs M_1 and M_2 , common-mode to differential-mode conversion will occur and the CMRR will be attenuated further.

4. Measurement results

The proposed fourth-order BPF shown in Fig. 7(b) has been fabricated in 0.18- μm AMS CMOS technology with a nominal threshold voltage of $V_{\text{tp}} \cong -0.42$ V. The filter chip photo is shown in Fig. 9. Including the filter core (pMOS transistors and dual MIM capacitors $C_1=10C_2=6$ pF), the bias circuit (formed by simple current mirror circuits) and source follower buffers to drive the off-chip capacitive load (formed by the bondpads, chip package, PCB and instrument probes), the chip occupies $64\text{ }\mu\text{m} \times 225\text{ }\mu\text{m}$ area. The following results were measured using a dynamic signal analyzer (SR785) under the condition of $V_{\text{DD}}=0.5$ V for the BPF and bias circuits, $V_{\text{DD}}=1.8$ V for the buffers and V_{CM} set to 0.15 V. An external bias current is supplied from a precision current source (Keithley 6430).

The measured magnitude responses of the second-order and the fourth-order BPFs are shown in Fig. 10. Bias current I_B was set to 1 nA to obtain a 1 kHz f_c . Mid-band gains K of -1.54 dB and -2.63 dB are observed for the second-order and fourth-order filters, respectively. These values include the gain loss of the source follower buffers, estimated to be around -0.45 dB.

Fig. 11 shows the measured magnitude responses of the fourth-order BPF for I_B ranging from 0.125 nA to 16 nA. f_c moves almost linearly for 7 octaves, starting from 124 Hz to 15.8 kHz. We can observe that, for I_B lower than 0.5 nA, K starts decreasing. At these values of bias current, diode connected M_2 is forced to leave weak inversion saturation as its drain-source voltage is being reduced by I_B . It affects the magnitude response and gives a lower limit to the filter's adjustability. The upper limit is defined by V_{DD} . When I_B goes high, the gate-source voltages of all transistors will go up and after they reach a certain value, the source voltage of M_1 and V_{DD}

will start forcing M_B out of its saturation region. This implies that the tuning range for higher frequencies can be widened by supplying more V_{DD} . Also noise from the measurement setup can be noticed at a magnitude of around -60 dB at frequencies lower than 200 Hz. This is because the signal amplitude was set very small (10 mV) within the linear range of the BPF. Low frequency noise with peak values around $10\text{ }\mu\text{V}$ affects the measured results in this range.

To see the tunability of the fourth-order BPF in more detail, cutoff frequencies obtained from different values of I_B have been collected and plotted in Fig. 12. Linear tunability of the proposed filter is obtained for 7 octaves (more than 2 decades). As has been discussed in the previous paragraph, although linear adjustability is confirmed for f_c , mid-band gain K cannot be maintained constant over the whole tuning range. This phenomenon can be

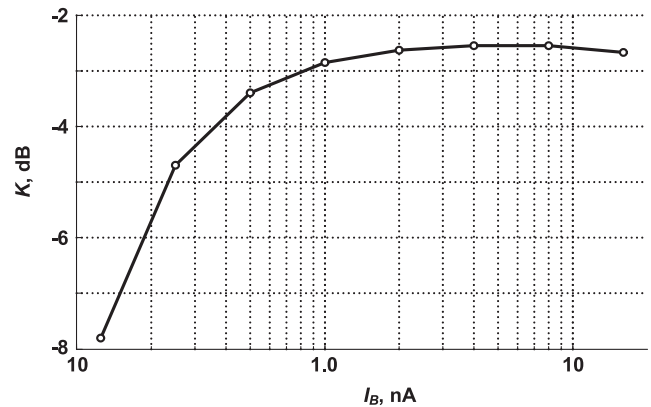


Fig. 13. Midband gain versus bias current.

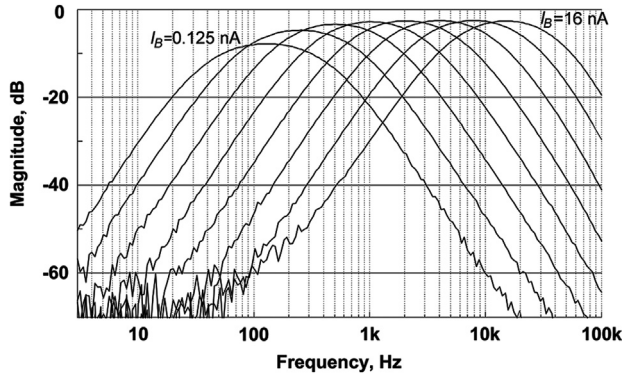


Fig. 11. Magnitude responses of the fourth-order BPF for different bias currents ranging from 0.125 nA to 16 nA.

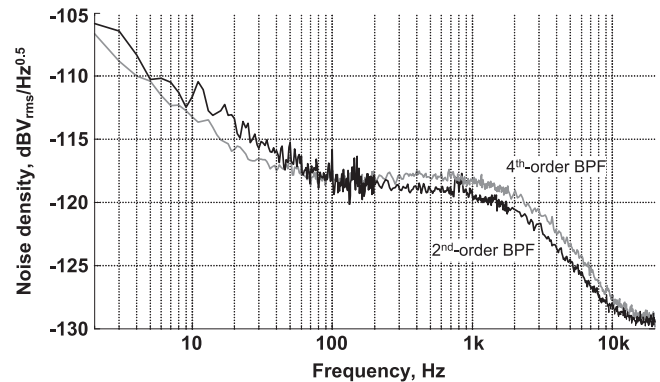


Fig. 14. Output noise voltage spectral density.

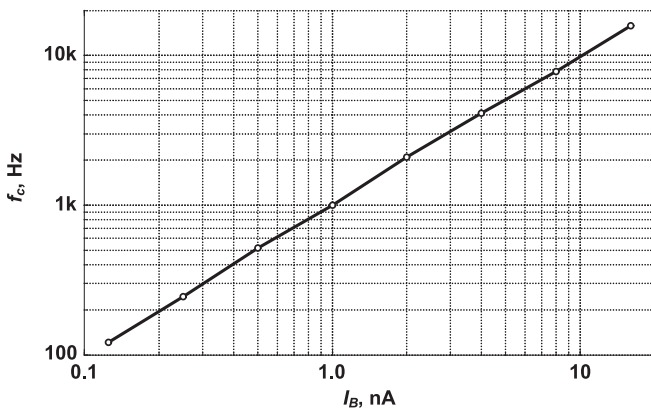


Fig. 12. Center frequency versus bias current.

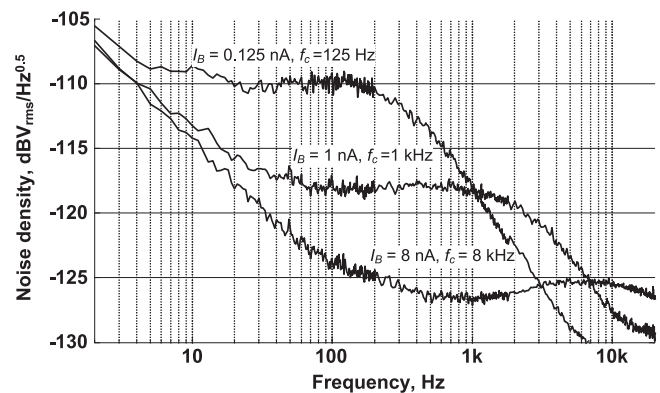


Fig. 15. Output noise voltage spectral density for different center frequencies.

seen more clearly from Fig. 13, in which, for the same conditions as for the results obtained in Fig. 12, values of K have been collected and plotted. For I_B less than 1 nA, K drops below -3 dB. On the other hand, for higher I_B , a K higher than -3 dB can be maintained.

Fig. 14 shows the measured output noise voltage spectral densities of both BPFs. At frequencies lower than f_c , both shot noise and flicker noise contribute noise to the output. Within this frequency range the noise density was suppressed more for the case of a fourth-order BPF due to the steeper roll-off in its transition band. For frequencies higher than 1 kHz, only shot noise plays a role and it is suppressed by the filter's transfer function. Integrated over the entire bandwidth, output noise voltages of $54 \mu\text{V}_{\text{rms}}$ and $57.4 \mu\text{V}_{\text{rms}}$ are obtained for the second-order and fourth-order BPFs, respectively.

Output noise voltage spectral densities of the fourth-order BPF for different f_c s (adjusted by different I_B s) are presented in Fig. 15. The filter's noise power spectral density goes lower for higher I_B (higher f_c and bandwidth). This mechanism maintains the same integrated shot noise power for different values of I_B .

The linearity of the filter has been tested by applying a sinusoidal input voltage to the filter with input frequency $f_{\text{in}}=f_c$ and observing its output spectrum. For the case of $I_B=1$ nA (1 kHz f_c), the measured results for input amplitudes V_{inps} of 25 mV and 58 mV are illustrated in Fig. 16. Since the proposed filter operates in a differential fashion, the third-harmonic component was found to be the main harmonic component. The third harmonic distortions (HD_3) were found at -40.7 dB and -26.1 dB for 25 mV and 58 mV V_{inps} , respectively. These values are associated with a total harmonic distortion (THD) of 1% and 5%, respectively.

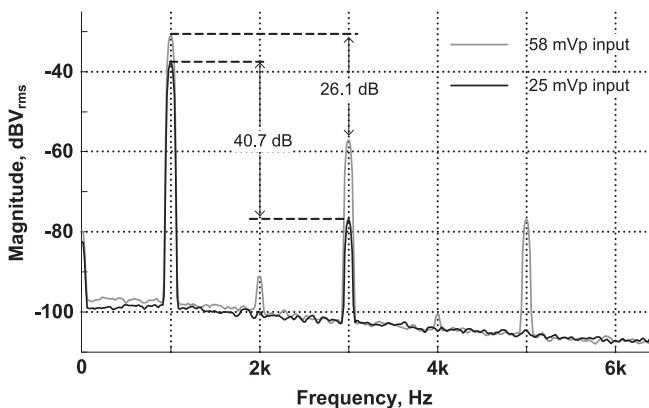


Fig. 16. Output voltage spectra of the fourth-order BPF for $f_{\text{in}}=f_c=1$ kHz.

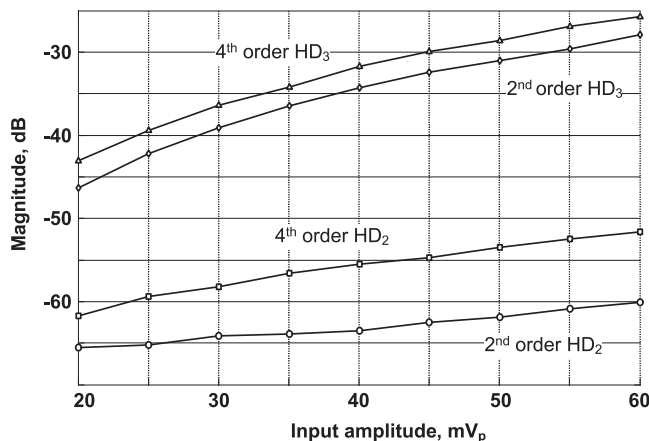


Fig. 17. Harmonic components versus input amplitude.

Fig. 17 provides the values of second harmonic distortion HD_2 and HD_3 of both the second-order and the fourth-order filters for different V_{inps} at $f_{\text{in}}=f_c=1$ kHz. For the range of $20 \text{ mV} < V_{\text{inps}} < 60 \text{ mV}$, HD_2 appeared more than 20 dB below HD_3 for both cases. For this reason HD_3 can be considered to be responsible for the THD. The HD_3 for the fourth-order BPF was found 3 dB worse than that of the second-order BPF for the entire range of V_{inps} . As the filter's pass band is quite flat and the transition band roll-off is not sharp, the third order intermodulation distortion (IMD_3) can be estimated by calculating it from the exponential behavior of transistor pair M_1 . For $V_{\text{inps}}=25$ mV and $U_T=26$ mV, it is found that $\text{IMD}_3 \approx -28.5$ dBc.

Other relevant filter parameters at $I_B=1$ nA were also tested and are summarized for the second and fourth-order BPFs in Table 1. It can be seen that all the filter characteristics of the second-order BPFs are better than those of the fourth-order one except the filter selectivity. More detail on the fourth-order BPF characteristics is summarized in Table 2 for three different cutoff frequencies.

Table 1

Filter performance for 1 kHz center frequency.

Filter	Second-order	Fourth-order
Total current (nA)	2 ($2I_B$)	4 ($4I_B$)
V_{DD} (V); P (nW)	0.5; 1	0.5; 2
K (dB)	-1.54	-2.63
BW (f_i-f_h) (Hz)	290–3.49k	420–2.55k
$V_{\text{inps}}@1\%$; 5% THD (mV)	29; 68	25; 58
^a $\text{IMD}_3@V_{\text{inps}}=25$ mV	-28.5 dBc	-28.5 dBc
^b Output noise (μV_{rms})	54	57
Inp. referred noise (μV_{rms})	65	78
DR@1%; 5% THD (dB)	50; 57.5	47; 55

^a Calculated.

^b Integrated over BW.

Table 2

Performance summary of the proposed filter.

I_B (nA)	0.125	1	8
f_c (Hz)	124	1k	7.84k
BW (f_i-f_h) (Hz)	48–345	420–2.5k	3.2k–19.7k
K (dB)	-7.85	-2.63	-2.55
^a Output noise (μV_{rms})	51	57.4	67
Inp. referred noise (μV_{rms})	126	78	90
$V_{\text{inps}}@1\%$; 5% THD (mV)	27; 67	25; 58	25; 59
DR@1%; 5% THD (dB)	44; 52	47; 55	46; 53
FoM@1%; 5% THD (10^{-18} J)	20; 3.2	10; 1.6	12.8; 2.6

^a Integrated over BW.

Table 3

Performance summary and comparison.

Reference	[2], 2003	[3], 2007	[4], 2009	[5], 2010	[6], 2011	This work
CMOS tech. (μm)	1.5	0.35	0.18	0.18	0.35	0.18
Order	4	6	8	4	7	4
Chip area (mm^2)	NA	0.234	0.11	0.132	0.216	0.0144
f_c (Hz)	141	671	3.5k	732	2	1k
P (nW)	230	68	875	14.4	0.06	2
V_{DD} (V)	2.8	1	1.2	1	1	0.5
Inp. referred noise (μV_{rms})	776	50	NA	50	51	78
THD (%)	5	NA	NA	1	0.3	1
DR (dB)	67.5	49	37	55	43	47
FoM (10^{-18} J)	72.5	213	6240	15.6	215	9.98

Table 3 shows a performance comparison among existing biomedical BPFs collected from journal articles with measurement results. The main distinct features of this design are the 0.5 V V_{DD} , smallest chip area and the FoM of 9.98×10^{-18} J and 1.58×10^{-18} J measured at 1% THD and 5% THD, respectively. The latter value is approximately an order of magnitude better than that of [5], the lowest number reported until recently. Also our BPF occupies approximately 10 times smaller chip area compared with that of [5]. The BPF of [5] and ours are comparable in circuit complexity and process technology but the pMOS second-order circuit cell of [5] cannot be connected in cascade without considerable loading effect and the circuit itself requires a higher V_{DD} of $2V_{SG} + V_{SDsat}$. It is also interesting to see that the seventh-order BPF of [6] consumes extremely little power of 60 pW, which is almost 45 times smaller than that of our design, but it does not provide the best FoM since its f_c is only 2 Hz.

5. Conclusion and discussion

A smart choice of the filter topology and a very compact circuit that operates from a very low supply voltage are the keys to the design of a BPF to achieve a good FoM. Measurement results of the proposed BPF filter, designed according to the keys mentioned above, show a considerable FoM improvement with respect to other existing designs. The proposed BPF filter can find its application in multi-channel cochlear implant speech processors that require very low power consumption and more than 6 octaves tuning ability ranging from 100 Hz to 10 kHz [2]. Although the DR of this proposed BPF is not as high as that of the BPF in [2], in

combination with a logarithmic compressor as recently suggested by Suzuki et al. [11], a sufficient overall DR can be obtained.

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