Microelectronics Journal ∎ (∎∎∎∎) ∎∎∎–∎∎∎

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Hybrid cascode feedforward compensation for nano-scale low-power ultra-area-efficient three-stage amplifiers

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ARTICLE INFO

Article history:
Received 29 March 2013
Received in revised form
2 August 2013
Accepted 6 August 2013

Keywords:
Cross-feedforward cascode compensation
Frequency compensation
Hybrid cascode feedforward compensation
Low power
Nested-Miller compensation
Operational amplifier (opamp)
Single-Miller feedforward compensation
and stability

ABSTRACT

A modified frequency compensation technique is proposed for low-power area-efficient three-stage amplifiers driving medium to large capacitive loads. Coined hybrid cascode feedforward compensation (HCFC), the total compensation capacitor is divided and shared between two internal high-speed feedback loops instead of only one loop as is common in prior art. Detailed analysis of this technique shows significant improvement in terms of bandwidth and stability. This is verified for a 1.2-V amplifier driving a 500-pF capacitive load in 90-nm CMOS technology, where HCFC reduces the total capacitor size and improves the gain-bandwidth by at least 30% and 40% respectively, compared to the prevailing schemes.

1. Introduction

Frequency compensation is a conventional design step in the design procedure for negative-feedback amplifiers used in drivers, filters, data converters and low-dropout regulators [1–17]. Depending on the load capacitor (C_L), a minimum compensation capacitor (C_C) is required to maintain stability, by which the gain-bandwidth (GBW) and slew-rate (SR) are affected depending on their value. With two large compensation capacitors proportional to C_L, the well-known nested Miller compensation (NMC) [1–3] fails to achieve sufficient GBW and SR under low power constraints. Various frequency compensation strategies have therefore been proposed to reduce the size of the compensation capacitors with limited power budget. Multipath nested Miller compensation (MNMC) [6] compensation is among these solutions which aims to further push away the power/area envelope. It uses a feedforward stage to implant an additional left-half-plane (LHP) zero to the NMC transfer function. The undesired right-half plane (RHP) zero in basic NMC architecture imposes excessive power for sufficient stability. Nested *Gm-C* compensation is another compensation solution dedicated for three-stage amplifiers to remove this RHP zero [7]. Looking for ways to remove the bulky capacitance used within the internal ac feedback loop of the NMC has also been the idea of some improved architectures. This capacitance is used to control the location of the complex poles for adequate gain margin (GM). The damping-factor-control frequency compensation (DFCFC) [8] replaces this capacitor with an active damping-factor-control unit. As a step further, the main compensation capacitor is substituted with an active capacitance in active feedback frequency compensation (AFFC) [9], resulting in improved stability with lower compensation capacitance. The remaining passive capacitance in AFFC is replaced by a damping-factor-control unit in dual-loop parallel compensation (DLPC) [10]. Two high-speed paths are also included to extend the bandwidth and to reduce the capacitor [10]. A serial RC network is added at the output of the amplifier intermediate stage to create a LHP zero in impedance adapting compensation (IAC) [11]. A standard Miller capacitance is also used for pole-splitting. Combining the concepts of signal feedforwarding and pole-splitting, single Miller capacitor feedforward frequency compensation (SMFFC) successfully removes the second compensation capacitance in NMC topology [12]. As proposed, the sizing of the remaining capacitance can also be decreased when increasing the gain of the intermediate stage [12].

To stabilize the amplifiers driving ultra-large capacitive loads, a few compensation techniques have been reported so far. Among these solutions are single capacitor with current amplifier compensation (SCCAC) [13], and current-buffer Miller compensation (CBMC) plus parasitic-pole cancellation [14,15].

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http://dx.doi.org/10.1016/j.mejo.2013.08.004

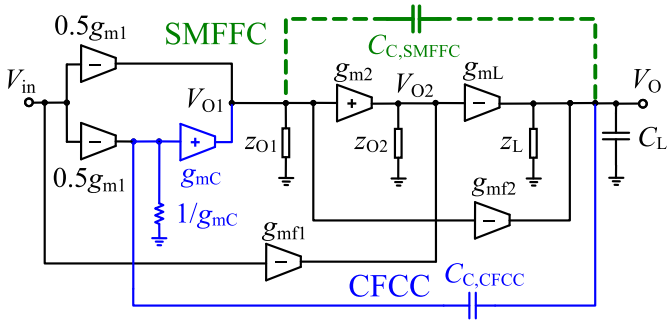

Fig. 1. Block diagram of a three-stage amplifier with SMFFC and CFCC.

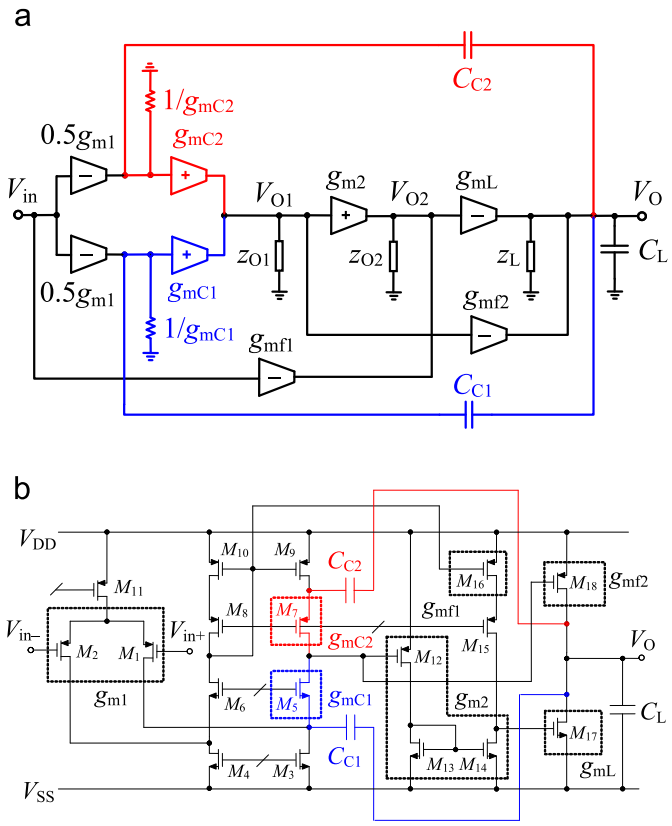

Fig. 2. Structure of a three-stage HCFC amplifier: (a) block diagram; and (b) circuit-level implementation.

The available compensation solutions some of which reported above considerably reduce the size of the compensation network, yet, unless consuming significant power, this block still remains as one of the largest parts of the integrated negative-feedback amplifiers [5–15].

Cross feedforward cascode compensation (CFCC) [16] is one of the recently-proposed effective solutions to decrease the size of the compensation capacitance in a three-stage operational amplifier. In comparison with other topologies based on the required capacitance value, power consumption, and design complexity, it shows better performance metrics for capacitive loads up to a few nano-farads [5–16]. Fig. 1 depicts a three-stage amplifier with one compensation capacitance either in SMFFC or CFCC configurations. Compared to advanced variations of NMC, SMFFC needs less area for implementation as the required C_C is divided by the gain of the intermediate stage [12]. A transconductance (g_m)-stage (g_{mC}) in series with the compensation capacitance further decreases the required area in accordance with the results from CFCC [16]. This makes C_C a function of $\sqrt{C_L}$ rather than C_L in SMFFC that is considerably effective especially for larger capacitive loads.

Coined hybrid cascode feedforward compensation (HCFC), Fig. 2a shows the proposed compensation scheme with two compensation capacitors, i.e., C_{C1} and C_{C2}. A similar compensation scheme proves useful for low-dropout regulators and two-stage operational amplifiers [4,17]. One important observation from this topology is that instead of a single loop to stabilize the amplifier as occurs in Fig. 1, HCFC shares the total capacitance between two high-speed feedback loops each with a corresponding g_m-stage (g_{mC1} and g_{mC2}) [4]. The output current is thus sensed and buffered via g_{mC1} and g_{mC2} simultaneously. For equal g_{mC1} and g_{mC2}, the amount of ac current fedback by the compensation network to the first gain stage is now twice that of CFCC. This decreases the total loading of the compensation network on the output node and, for the same capacitance as CFCC, extends the bandwidth. Hence, identical stability margins are resulted with smaller compensation network and, accordingly, smaller operational amplifier. A circuit-level implementation of a three-stage HCFC amplifier is illustrated Fig. 2b. The additional g_m-stage (g_{mC2}) required in this topology is properly embedded to the input stage without any increase in die size and power.

A few key parameters should be taken into consideration in order to quantify and fairly compare the efficiency of various frequency compensation topologies. Among these variables, the supply current of the amplifier (I_{DD}), the load capacitance it can drive (C_L), and the achieved GBW and SR are especially important. Based on these metrics, the two widely-used figures of merit, IFOMS$=$GBWC_L/I_{DD} and IFOML$=$SRC_L/I_{DD}, can be used to characterize the small-signal and large-signal capabilities. Comparing the results for HCFC with CFCC, the proposed technique improves the small-signal IFOMS and the large-signal IFOML by at least 40%.

The rest of this paper is organized as follows. The proposed HCFC is analyzed based on the transfer function, stability, noise, and slew-rate in Section 2. In Section 3, the HCFC is compared with SMFFC and CFCC from different perspectives from small-signal to large-signal behaviors. As an important result, it is shown that the HCFC can achieve similar stability margins with compensation capacitor values considerably smaller than in SMFFC and CFCC. A proposed HCFC amplifier is detailed and carefully simulated in Section 4. The conclusions are drawn in Section 5 along with a few comments for future works.

2. Hybrid cascode feedforward compensation

2.1. Transfer function

The amplifier diagram in Fig. 2a contains three main gain stages each with an equivalent transconductance (g_{m1}, g_{m2}, g_{mL}), and an output impedance (z_{o1}, z_{o2}, z_{oL}). Each output impedance is composed of a capacitance element (C_{P1}, C_{P2}, C_L) along with a conductance (g_{O1}, g_{O2}, g_L), where $z_{Oi}=1/(g_{Oi}+sC_{Pi})$. The amplifier also contains two feedforward stages (g_{mf1} and g_{mf2}) to improve the large-signal settling response as well as the small-signal settling behavior [8,10,12,16]. Analysis of this topology is simplified (and, as will be shown later, improved) by defining an equivalent transconductance g_{mC} and a total compensation capacitor C_C such that:

$$g_{mC}=g_{mC1}=g_{mC2} \quad \text{and} \quad C_C=2\times C_{C1}=2\times C_{C2}. \tag{1}$$

To obtain a simplified transfer function for this topology, the following assumptions are considered to hold:

(1) The DC gains of all the stages are much greater than unity.
(2) The parasitic output capacitors C_{P1}, and C_{P2} are much smaller than C_C and C_L.

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Under these circumstances, the gain of the amplifier is calculated as follows:

$$A_V(s) = V_O/V_{in} \approx \frac{A_0\left(1+s\frac{C_C}{2g_{mC}}\right)\left(1+s\frac{g_{mf1}C_{P1}}{g_{m1}g_{m2}}\right)\left(1-s\frac{g_{m1}C_{P2}}{g_{mf1}g_{mL}}\right)}{\left(1+s\frac{1}{p_{-3dB}}\right)\left[\begin{array}{l}1+s\frac{g_{O1}g_{O2}C_C C_L}{2g_{mC}(g_{O1}g_{O2}C_L+g_{m2}g_{mL}C_C)}\\ +s^2\frac{C_C C_L(g_{O1}C_{P2}+g_{O2}C_{P1})}{2g_{mC}(g_{O1}g_{O2}C_L+g_{m2}g_{mL}C_C)}\end{array}\right]\left(1+s\frac{C_{P1}}{g_{O1}}\right)} \quad (2)$$

In this equation, $A_0 = +(g_{m1}g_{m2}g_{mL})/(g_{O1}g_{O2}g_L)$ and $p_{-3dB} = -(g_{O1}g_{O2}g_L)/(g_{m2}g_{mL}C_C)$ are the DC gain and the dominant pole, respectively. The GBW is also given as

$$\mathrm{GBW} = A_0 \times |p_{-3dB}| = g_{m1}/C_C \quad (3)$$

The transfer function in (2) has two LHP zeros $z_1 = -2g_{mC}/C_C$ and $z_2 = -(g_{m1}g_{m2})/(g_{mf1}C_{P1})$ and one RHP zero $z_3 = +(g_{mf1}g_{mL})/(g_{m1}C_{P2})$ at very high frequencies. It also contains three non-dominant poles p_2, p_3 and $p_4 = -g_{O1}/C_{P1}$. The two LHP zeros add more phase lead to increase the phase margin and improve stability.

2.2. Stability considerations

The absolute stability condition of an HCFC amplifier can be determined, at first, by neglecting the zeros of (2) and then by analyzing the closed-loop transfer function $A_{CL}(s)$ of the amplifier connected in unity-gain feedback configuration. The closed-loop transfer function is therefore derived as

$$A_{CL}(s) \approx \frac{1}{1+s(C_C/g_{m1})+s^2((g_{O1}g_{O2}C_C C_L/2g_{mC}g_{m1}g_{m2}g_{mL})+C_C C_{P1}/g_{m1}g_{O1}) +s^3\left[\frac{C_C C_L(g_{O1}C_{P2}+2g_{O2}C_{P1})}{2g_{m1}g_{m2}g_{mL}g_{mC}}\right]+s^4\left[\frac{C_C C_{P1}C_L(g_{O1}C_{P2}+g_{O2}C_{P1})}{2g_{m1}g_{m2}g_{mL}g_{mC}g_{O1}}\right]} \quad (4)$$

Applying the Routh–Hurwitz stability criterion on $A_{CL}(s)$ [7], two conditions are resulted as the prerequisites for unconditional stability. The first condition is an inequality which holds always while the second condition sets a low limit to C_L depending on C_C, C_{P1} and C_{P2}

$$C_L > \frac{2g_{mC}g_{m2}g_{mL}g_{O2}C_{P1}^2 C_C}{g_{O1}(g_{O1}C_{P2}+2g_{O2}C_{P1})(g_{m1}g_{O1}C_{P2}+2g_{m1}g_{O2}C_{P1}-g_{O1}g_{O2}C_C)} \quad (5)$$

If and only if condition (5) is satisfied, the amplifier is unconditionally stable.

Depending on the device sizes, the two first non-dominant poles in (2) can be either real or complex conjugate. The expression for phase margin (PM) can thus be different depending on the location of p_2 and p_3. For complex poles, PM is expressed as

$$\mathrm{PM} = 180^o - \tan^{-1}(\mathrm{GBW}/p_{-3dB}) - \tan^{-1}\left(\frac{(\mathrm{GBW}/|p_{2,3}|)}{Q\times[1-(\mathrm{GBW}/|p_{2,3}|)^2]}\right) - \tan^{-1}(\mathrm{GBW}/p_4) + \tan^{-1}(\mathrm{GBW}/z_1) + \tan^{-1}(\mathrm{GBW}/z_2) - \tan^{-1}(\mathrm{GBW}/z_3) \approx 90^o - \tan^{-1}(\mathrm{GBW}/p_4). \quad (6)$$

This approximation for the PM shows that its value depends on the location of p_4 and consequently to C_{P1} and g_{O1}.

2.3. Noise

With reference to the topology illustrated in Fig. 2b, the input-referred noise is generated mostly by M_1, M_2 and M_9 and M_{10}. Other sources including those in intermediate and output stages are significantly suppressed when referred to the input. Neglecting the flicker noise which only dominates at lower frequencies, the total input-referred thermal noise ($\overline{V_{ni}}^2$) is

$$\overline{V_{ni}}^2 \approx 2\times\left(4kT\gamma\frac{1}{g_{m1}}\right)\left(1+\frac{g_{m9}}{g_{m1}}\right) = \frac{8kT\times\gamma\times F}{g_{m1}}, \quad (7)$$

where k is Boltzmann constant, T is absolute temperature, g_{m9} is the transconductance of the differential pair M_9 and M_{10}, $F = 1+g_{m9}/g_{m1}$ is the excess noise factor, and γ is a noise factor that depends on the technology ($\gamma = 2/3$ for long-channel devices operating in strong-inversion saturation [18]). Eq. (7) shows that in addition to input devices which are always critical for input-referred noise, the differential pair M_9 and M_{10} also contributes to F and should be left in an operating point with minimum transconductance.

2.4. Slew-rate and settling time

The effective slew-rate of the HCFC amplifier depicted in Fig. 2b is considered as the minimum between the internal slew-rate of the first gain stage ($\mathrm{SR_{INT}}$) which drives the compensation capacitors (C_{C1} and C_{C2}) and the external slew-rate of the output stage ($\mathrm{SR_{EXT}}$). In Fig. 2b, the feedforward stage g_{mf2} and the output stage g_{mL} form a push–pull stage at the output. This combination along with the balanced formation of the compensation capacitors in the proposed topology equalizes the SR in both rising and falling edges of the settling response. Denoting I_B and I_L as, respectively, the amount of the current available to charge and discharge $C_{C1}+C_{C2}$ and $C_{C1}+C_{C2}+C_L$, $\mathrm{SR_{INT}}$ and $\mathrm{SR_{EXT}}$ are expressed by

$$\mathrm{SR_{INT}} = \frac{I_B}{C_{C1}+C_{C2}}, \quad \mathrm{SR_{EXT}} = \frac{I_L}{C_{C1}+C_{C2}+C_L}. \quad (8)$$

Setting SR equal to both $\mathrm{SR_{INT}}$ and $\mathrm{SR_{EXT}}$ as an optimal design criterion, it can be seen that SR can be improved by either increasing the bias currents (I_B and I_L) or by reducing the compensation capacitors. Without sacrificing more current, higher SR is therefore achieved by selecting a compensation scheme which stabilizes the amplifier with smaller compensation capacitors.

The settling time (t_S) is defined as the moment when the transient response to a step input enters to and remains within an error band around a desired value. For an operational amplifier, t_S is divided into two portions: large-signal settling time t_{LS} (that is a function of the SR and the step amplitude V_{max}) and small-signal settling time t_{SS} (which depends on the GBW and stability criteria) [3]. This observation of the total settling time yields [3,19]

$$t_S = t_{SS} + t_{LS} = \frac{n}{\mathrm{GBW}} + \frac{V_{max}}{\mathrm{SR}}, \quad (9)$$

where n is defined as the equivalent time-constant coefficient of first-order systems that is the number of time constants required for the output response to enter the error band around the final value [3,19]. It depends on the stability conditions of the amplifier and also the required settling error. Eq. (9) predicts that an amplifier can achieve shorter settling times when the employed frequency compensation scheme allows higher GBW and SR for the same stability criteria.

2.5. Matching between elements

Based on the conditions presented in (1) and certain assumptions highlighted earlier, the transfer function of the HCFC amplifier was evaluated in (2). The transfer function may contain an additional pole and zero located at different frequencies when C_{C1}, C_{C2}, g_{mC1} and g_{mC2} of the two feedback loops deviate from (1).

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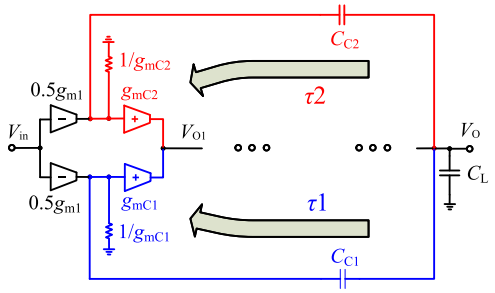

Fig. 3. Different time constant in each loop for the current fedback to the first stage.

In a not so careful design, two unequal time constants are therefore resulted for the ac currents fedback to the first gain-stage output by the output stage (see $\tau 1$ and $\tau 2$ in Fig. 3). The resulting doublet from this incomplete pole-zero cancellation may affect the settling response of the amplifier. This can be avoided even for $C_{C1} \neq C_{C2}$ and $g_{mC1} \neq g_{mC2}$ when $\tau 1$ and $\tau 2$ are forced to be equal i.e.,

$$\tau 1 = \tau 2 \quad \Rightarrow \quad \frac{g_{mC1}}{C_{C1}} = \frac{g_{mC2}}{C_{C2}} \quad \Rightarrow \quad \frac{C_{C2}}{C_{C1}} = \frac{g_{mC2}}{g_{mC1}}. \tag{10}$$

Simulation data concerning this effect will be presented further in Section 4.

3. Comparison between HCFC, CFCC and SMFFC

3.1. Area

In terms of the capacitor size, the HCFC is highly efficient compared to SMFFC. When the poles are real similar to SMFFC, the magnitude of the first non-dominant pole (p_2) can be compared with that of SMFFC ($p_{2,\mathrm{SMFFC}}$) [12], according to

$$\begin{aligned} p_2 &= 2\left(\frac{g_{mC}}{g_{O1}} + \frac{C_L g_{mC} g_{O2}}{C_C g_{mL} g_{m2}}\right) \times \left[\frac{-g_{m2} g_{mL}}{g_{O2} C_L}\right] \\ &= 2\left(\frac{g_{mC}}{g_{O1}} + \frac{C_L g_{mC} g_{O2}}{C_C g_{mL} g_{m2}}\right) \times p_{2,\mathrm{SMFFC}}. \end{aligned} \tag{11}$$

As $g_{mC} > > g_{O1}$, p_2 is located at frequencies much higher than $p_{2,\mathrm{SMFFC}}$. Hence, by adopting GBW$=|p_2|/2$ for sufficient phase margin [12], SMFFC will achieve the same stability as HCFC with a capacitance

$$C_{C,\mathrm{SMFFC}} = 2\left(\frac{g_{mC}}{g_{O1}} + \frac{C_L g_{mC} g_{O2}}{C_C g_{mL} g_{m2}}\right) \times C_C \tag{12}$$

which is larger than C_C ($=2C_{C1}=2C_{C2}$) by one order of magnitude. Consequently, higher GBW and SR can be anticipated by selecting HCFC. In contrast to CFCC, HCFC still enables the non-dominant complex poles of the amplifier to be located at higher frequencies [16]

$$\begin{aligned} |p_{2,3}| &= \sqrt{\frac{2g_{mC}(g_{O1}g_{O2}C_L + g_{m2}g_{mL}C_C)}{C_C C_L (g_{O1}C_{P2} + g_{O2}C_{P1})}} \approx \sqrt{2} \times \sqrt{\frac{g_{mC}g_{m2}g_{mL}}{g_{O2}C_L C_{P1}}} \\ &= \sqrt{2} \times |p_{2,3}|_{\mathrm{CFCC}}. \end{aligned} \tag{13}$$

Fig. 4 compares the pole-zero diagrams of these schemes. For the HCFC, by adopting a third-order Butterworth response and by assuming that $|z_1|=|p_{2,3}|=2\times$GBW as a good design criterion, we will conclude [16]

$$|z_1| = 2 \times \mathrm{GBW} \quad \Rightarrow \quad g_{m1} = g_{mC} \tag{14}$$

$$|p_{2,3}| = 2 \times \mathrm{GBW} \Rightarrow C_C = \sqrt{2 \times \frac{g_{m1}g_{O2}}{g_{m2}g_{mL}} C_L C_{P1}} = \frac{\sqrt{2}}{2} \times C_{C,\mathrm{CFCC}} \tag{15}$$

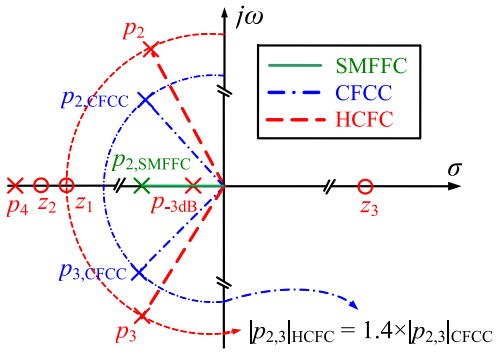

Fig. 4. Pole-zero diagrams of SMFFC, CFCC and HCFC.

Expression (15) shows that HCFC achieves the same stability as CFCC with a roughly 30% smaller capacitor, leading to about 40% increase in GBW and SR (which is equivalent to lower settling times according to (9)). Moreover, it shows that the HCFC amplifier occupies less area for similar stability.

3.2. Power

The proposed HCFC compensation solution can be compared with SMFFC and CFCC in terms of the amount of power required for achieving similar bandwidth and stability. For identical compensation capacitors, Eqs. (3), (12) and (15) show that SMFFC, and CFCC should achieve the same GBW and stability criteria as HCFC when their input device transconductances ($g_{m1,\mathrm{SMFFC}}$ and $g_{m1,\mathrm{CFCC}}$) are related to that of HCFC (g_{m1}) as (see Fig. 2b)

$$g_{m1,\mathrm{SMFFC}} = 2\left(\frac{g_{mC}}{g_{O1}} + \frac{C_L g_{mC} g_{O2}}{C_C g_{mL} g_{m2}}\right) \times g_{m1}, \tag{16}$$

$$g_{m1,\mathrm{CFCC}} = \sqrt{2} \times g_{m1}. \tag{17}$$

For HCFC and CFCC, the required g_{mC} should also be equal to g_{m1} such that the first zero (z_1) is maintained at the desired location (Eq. (14)).

As the bias current of a MOS device is proportional to its transconductance, Expressions (16) and (17) show that the amount of the current required by the first gain stage of the SMFFC and CFCC amplifiers should be about 40% and one order of magnitude larger than the HCFC counterpart. This leads to less power consumption in the proposed topology.

3.3. Minimum supply

Compared to the SMFFC and CFCC architectures, an additional g_m-stage is required in the HCFC topology for complete compensation network. Without any power overhead, this additional g_m-stage (g_{mC2}) is embedded to the first gain stage and realized by M_7 in circuit-level implementation of Fig. 2b. The inclusion of M_7 and M_8, however, although advantageous in terms of DC gain and stability, adds one overdrive voltage ($V_{DS,\mathrm{SAT}}$) to the minimum voltage supply required ($V_{DD,\mathrm{MIN}}$) to bias the amplifier. In brief, the required $V_{DD,\mathrm{MIN}}$ to implement an HCFC amplifier is roughly one $V_{DS,\mathrm{SAT}}$ ($\sim$0.1–0.2 V) higher than SMFFC and CFCC amplifiers.

4. Circuit implementation and results

To verify the effectiveness of the proposed HCFC compensation strategy, the three-stage amplifier shown in Fig. 2b is simulated in a 90-nm CMOS technology. With only 22 μA bias current and

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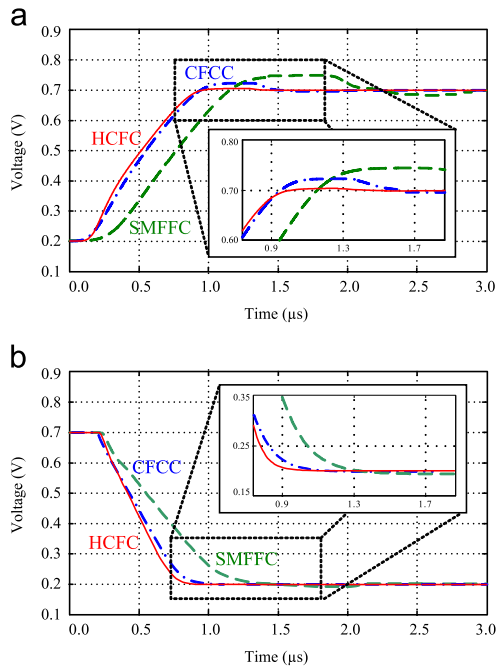

Fig. 5. Comparison between SMFFC, CFCC and HCFC transient step responses: (a) rising edge; and (b) falling edge.

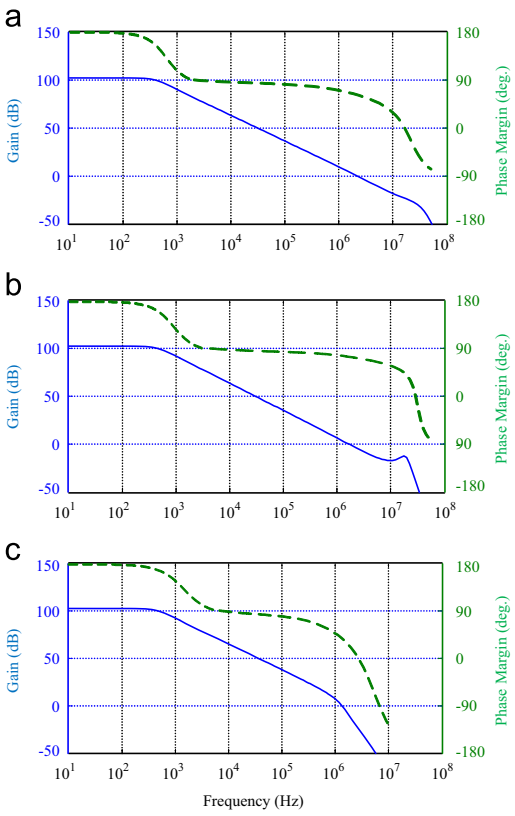

Fig. 6. Comparison between frequency responses: (a) HCFC; (b) CFCC; and (c) SMFFC.

0.8 pF total compensation capacitor, the achieved GBW for 500 pF load capacitor is 2.41 MHz.

Fig. 5 shows the HCFC transient response under unity-feedback configuration for $V_{DD}=1.2$ V, $C_L=500$ pF, $C_{C1}=C_{C2}=0.4$ pF. It also compares the transient response of the amplifier when it is compensated either by SMFFC or CFFC with a same total capacitance value.

Table 1
Results summary of SMFFC, CFCC and HCFC amplifiers.

	HCFC	CFCC	SMFFC
C_L (pF)		**500**	
I_{DD} (mA)		**0.022**	
C_C (pF)	**0.80**	1.10	8.40
GBW (MHz)	**2.41**	1.73	0.26
SR+/SR−(V/μS)	**0.74/0.71**	0.53/051	0.08/0.22
C_L/C_C (pF/pF)	**625**	454	59
IFOMS [(MHz pF)/mA]	**54,770**	39,300	5900
IFOML [(V/μS pF)/mA]	**16,818**	12,045	1818

The bold values are design specifications/simulation results of the proposed HCFC technique.

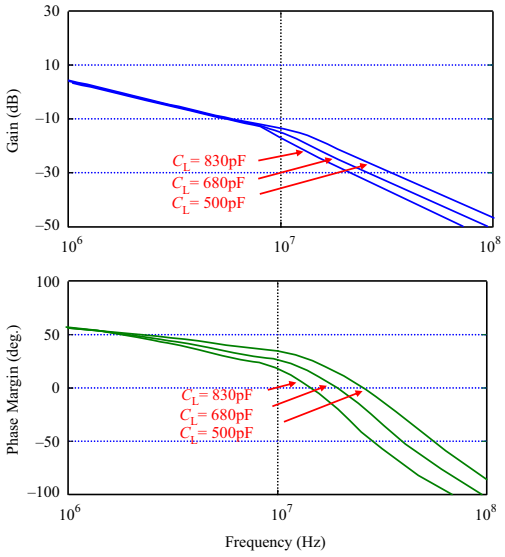

Fig. 7. Frequency response of HCFC amplifier at different C_L.

For the rising edge, the 0.1% settling times increases from 1.42 μs for HCFC to 2.24 μs and 5.53 μs for CFFC and SMFFC, respectively. The same variable increases from 1.33 μs to 2.12 μs and 4.96 μs for, respectively, HCFC, CFCC, and SMFFC during the falling edge.

Fig. 6 compares the resultant bode plot of the amplifier when it is compensated with HCFC, CFCC, and SMFFC. For 0.8 pF total compensation capacitor, the HCFC amplifier achieves a gain-bandwidth of 2.41 MHz with a PM and GM of 51° and 34 dB, respectively. With identical compensation capacitor for CFCC and SMFFC, the GBW, PM, and GM become 2.35 MHz, 53°, 17 dB and 1.73 MHz, 34°, 11 dB, respectively.

For a phase margin of about 50°, Table 1 compares the efficiency of different compensation techniques on the simulated amplifier. To perform a fair comparison, we obtained the performance metrics, IFOMS and IFOML, by simulating the amplifier in SMFFC, CFCC or HCFC configurations. In addition to offering competitive figures of merit, HCFC achieves the highest C_L/C_C ratio and thus requires the least chip area. For the specifications given in Table 1, the layout size of the amplifier has been evaluated and compared in 90-nm technology. Excluding the required compensation capacitors, the total silicon area occupied by the amplifier and its bias network is 6900 μm^2. For identical stability margins, however, the total capacitance size of the HCFC amplifier is approximately 400 μm^2. The area occupied by the compensation capacitor is roughly 37% (530 μm^2) and 90% (4050 μm^2) smaller than in the equivalent CFCC and SMFFC amplifiers, respectively.

The simulated frequency response of the proposed amplifier with different load capacitors is illustrated in Fig. 7. The amplifier achieves a GBW of 2.41, 2.39 and 2.36 MHz with a phase margin

Table 2
Performance of the simulated HCFC amplifier at C_L=500 pF over process and temperature corners.

+27 °C					
Corner	TT	SS	FF	SNFP	FNSP
GBW (MHz)	2.41	2.18	2.53	2.21	2.29
PM (deg)	51	55	48	50	53
SR+/SR–(V/μs)	0.74/0.71	0.69/0.65	0.79/0.75	0.71/0.68	0.70/0.74
−25 °C					
Corner	TT	SS	FF	SNFP	FNSP
GBW (MHz)	2.64	2.24	2.61	2.32	2.35
PM (deg)	53	57	54	55	54
SR+/SR–(V/μs)	0.75/0.74	0.68/0.71	0.81/0.86	0.73/0.71	0.71/0.79
+85 °C					
Corner	TT	SS	FF	SNFP	FNSP
GBW (MHz)	2.23	1.97	2.34	2.13	2.19
PM (deg)	50	55	49	52	53
SR+/SR–(V/μs)	0.73/0.68	0.65/0.61	0.77/0.76	0.69/0.66	0.69/0.72

TT typical; SS slow NMOS/slow PMOS; FF fast NMOS/fast PMOS; SNFP slow NMOS/fast PMOS; FNSP fast NMOS/slow PMOS.

Table 3
Statistical distribution of GBW, PM, and SR from 200 Monte-Carlo simulations due to local mismatches.

Parameter		Result
GBW (MHz)	Mean (MHz)	2.40
	σ (MHz)	0.16
PM (deg)	Mean (deg)	51
	σ (deg)	4
SR+/SR–(V/μs)	Mean (V/μs)	0.74/0.72
	σ (V/μs)	0.053/0.049

Table 4
Variation of 0.1% positive settling time due to intentional mismatch between C_{C1} and C_{C2} and/or g_{mC1} and g_{mC2}.

Settling time		$\delta g_{mC}/g_{mC}$		
		0%	+1%	−1%
$\delta C_C/C_C$	0%	1.42 μs	1.44 μs	1.43 μs
	+1%	1.43 μs	1.43 μs	1.45 μs
	−1%	1.44 μs	1.46 μs	1.43 μs

of 51°, 48° and 45° for C_L=500 pF, 680 and 830 pF, respectively. It is verified to be stable for the load capacitors up to 3 nF.

The effect of process and temperature variations on GBW, phase margin and slew-rate of the amplifier for C_L=500 pF are investigated via corner simulations. The results are summarized in Table 2. From simulations at 27 °C, it is evident that the GBW and phase margin over various corners deviate about 0.23 MHz and 7°, respectively. The positive and negative SR deviate from its nominal value by about 7% and 14%, respectively. The simulated amplifier remains stable with a minimum phase margin of 48° and a GBW of 1.97 MHz, across the extreme temperatures and process corners.

Monte Carlo simulations were executed over a sample of 200 iterations to evaluate the impact of transistor mismatches on the gain-bandwidth, phase margin, and slew-rate. The mean values and standard deviations are reported in Table 3. The standard deviations of the gain-bandwidth and phase margin are about 0.16 MHz and 4°, respectively.

The same variable is 0.053 V/μs and 0.049 V/μs for positive and negative slew-rates, respectively. As it can be inspected, the standard deviations in Table 3 are all lower than 8% with respect to their relevant nominal values.

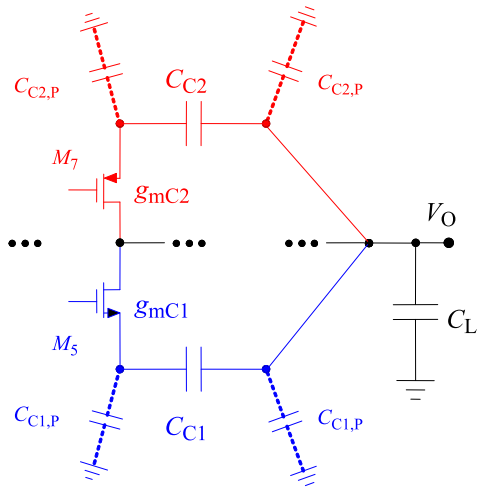

Fig. 8. Conditions of the ac feedback loops in spite of parasitic $C_{C1,P}$ and $C_{C2,P}$.

Table 5
Variation of 0.1% positive settling time in presence of parasitic $C_{C1,P}$ and $C_{C2,P}$.

Parasitic capacitors value	Settling time
$C_{C1,P}=0\times C_{C1}$ $C_{C2,P}=0\times C_{C2}$	1.42 μs
$C_{C1,P}=0.2\times C_{C1}$ $C_{C2,P}=0.2\times C_{C2}$	1.45 μs

As pointed out earlier in Section 2, the settling response of an HCFC amplifier can be degraded by an incomplete pole-zero cancellation when condition (10) is not satisfied.

To investigate the impact of this undesired phenomenon on the settling behavior, Table 4 compares the absolute values of the 0.1% settling time due to an intentional 1% mismatch between C_{C1} and C_{C2} and/or g_{mC1} and g_{mC2}. The settling time deviates by at most 2.8% from its nominal value when both the capacitors and transconductances have mismatch.

Another non-ideal factor which is in connection with the reliability is the effect of capacitor parasitics on the amplifier performance when C_{C1} and C_{C2} are small. In fact, the location of the two capacitors in the proposed architecture makes these parasitics less important. From one side, C_{C1} and C_{C2} are connected to source terminals of M_5 and M_7 with relatively small impedance to the ground (Fig. 8). This makes the role of the parasitic capacitors connected to these nodes ($C_{C1,P}$ and $C_{C2,P}$ in Fig. 8) less significant. From another side, both compensation capacitors are connected to the output node. Therefore, their parasitics only contribute to C_L. To study the significance of these parasitics on the performance, Table 5 summarizes the results for $C_{C1,P}$ and $C_{C2,P}$ as large as $0.2\times C_{C1}$ and $0.2\times C_{C2}$. It shows that the 0.1% positive settling time increases only 0.03 μs when the parasitics are as big as these values.

5. Conclusions and future works

Three-stage CMOS amplifiers are inevitably used to achieve the high accuracy required by many applications in nano-scale technologies. Compared to two-stage amplifiers with equal loading, bandwidth and stability of a three-stage amplifier are highly affected by the employed frequency compensation solution. An HCFC compensation scheme has been proposed for low-power area-efficient three-stage operational amplifiers. To decrease the loading effect of

Please cite this article as: H. Aminzadeh, et al., Hybrid cascode feedforward compensation for nano-scale low-power ultra-area-efficient three-stage amplifiers, Microelectron. J (2013), http://dx.doi.org/10.1016/j.mejo.2013.08.004

the compensation network on the output node, the total compensation capacitor is split and shared between two parallel ac feedback loops in amplifier topology each with one current buffer. With no increase in capacitor size or power, this enhances the amount of the ac current fedback to the first gain stage and, correspondingly, improves stability. Compared to prior art, analysis and simulation of the HCFC technique show significant improvement in terms of capacitor size, power and settling time.

Possible future work could include characterizing the application of HCFC amplifiers for switched-capacitor circuits. To this end, a design methodology based on the settling time of the output response can be very helpful. Another technique worth investigating is the expansion of the proposed compensation scheme to those amplifiers which have more cascaded stages. The analysis and design of such amplifiers also remains for further study.

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