Low-Power MOS Integrated Filter with Transconductors with Spoilt Current Sources

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***Abstract*—It is shown that an MOS weak-inversion differential pair can be linearized considerably by replacing the tail current source with a MOSFET biased in the weak-inversion triode region. Calculations show that the transconductance can be kept constant to within $+5\%/-0\%$ for input voltages up to 130 mV. This linearized differential pair is used in a third-order transconductance-C bandpass filter with 18 Hz and 142 Hz cutoff frequencies, which draws 4.9 nA from a 1.8-V supply. Its dynamic range is 62 dB and its active area is 0.5 mm^2.**

***Index Terms*— Active filters, low power, low voltage, MOS analog integrated circuits.**

I. Introduction

FOR applications such as implantable cardiac pacemakers, very-low-power low-frequency integrated circuits are needed. At very low currents, the voltage drop across a resistor is negligible unless the resistor has a value which is too large to be integrated. Similarly, at low drain currents, MOSFET's cannot be biased in strong inversion unless they are extremely long and narrow (or are used as switches). Hence, only circuits which contain neither resistors nor MOSFET's biased in strong inversion can be used at very low current levels.

In Section II, it is shown that a differential pair of which the current source transistor is biased in the weak-inversion triode region ($V_{\rm DS} < 4kT/q$) can be used as a linearized transconductance amplifier. Because this circuit only consists of MOSFET's biased in weak inversion, it is suitable for very low current levels. Its maximum input voltage is approximately equal to the maximum input voltage of some circuits found in the literature (of the order of 130 mV), but the supply current needed for a given transconductance is lower. Biasing the current source transistor in the triode region obviously makes it lose its current source character; its drain current is no longer independent of its drain voltage. This is why we have called this transistor a *verziekte stroombron*, literally translated a spoilt current source.

In Section III, a transconductance-C bandpass filter is described which consists of these linearized differential pairs, capacitors and current mirrors. Measurement results are presented in Section IV and conclusions are drawn in Section V.

II. The Transconductance Amplifier

Due to the nonlinearity of the MOSFET's, the voltage v_3 at the sources of M1 and M2 in Fig. 1 will rise when the differential input voltage v increases. (In fact, when v becomes very large, M2 is cut off and M1 acts as a source follower, which passes the changing voltage at its gate on to its source). When the output resistance of M3 is finite (because M3 is biased in the triode region), the tail current increases, and the dropping transconductance of the differential pair is compensated. The drain current of a MOSFET biased in weak inversion is given by

$$I_D = I_s e^{\frac{V_{\rm GS}}{\kappa V_T}} e^{\frac{V_{\rm BS}}{\eta V_T}} \left(1 - e^{-\frac{V_{\rm DS}}{V_T}}\right) \tag{1}$$

with $1/\kappa + 1/\eta = 1$ and $V_T = kT/q \approx 26$ mV at room temperature, I_s is a small, temperature-dependent constant. κ is typically about 1.5. Although κ depends slightly on the gate-bulk voltage, it can be considered to be approximately constant [1], [2]. The last factor equals unity when the MOSFET is biased outside the triode region ($V_{\rm DS} \gg V_T$).

If M3 is biased in the triode region, and if M1 and M2 are biased outside this region, the following equations hold:

$$I_1 = I_s e^{\frac{V_{\rm CM}+v/2}{\kappa V_T}} e^{-\frac{v_3}{V_T}} = I_{\rm hop} e^{x} e^{-\frac{v_3}{V_T}} \tag{2}$$

where v_3 is the drain voltage of M3 and $V_{\rm CM}$ is the voltage at the gate of M3 and the average of the gate voltages of M1 and M2, see Fig. 1. $I_{\rm hop}$ and x are defined as

$$I_{\rm hop} = I_s e^{\frac{V_{\rm CM}}{\kappa V_T}} \tag{3}$$

and

$$x = \frac{v}{2\kappa V_T}. \tag{4}$$

Further

$$I_2 = I_s e^{\frac{V_{\rm CM}-v/2}{\kappa V_T}} e^{-\frac{v_3}{V_T}} = I_{\rm hop} e^{-x} e^{-\frac{v_3}{V_T}} \tag{5}$$

$$I_3 = A I_s e^{\frac{V_{\rm CM}}{\kappa V_T}} \left(1 - e^{-\frac{v_3}{V_T}}\right) = A I_{\rm hop} \left(1 - e^{-\frac{v_3}{V_T}}\right). \tag{6}$$

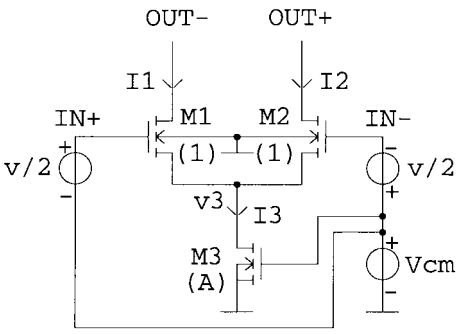

Fig. 1. The transconductance amplifier.

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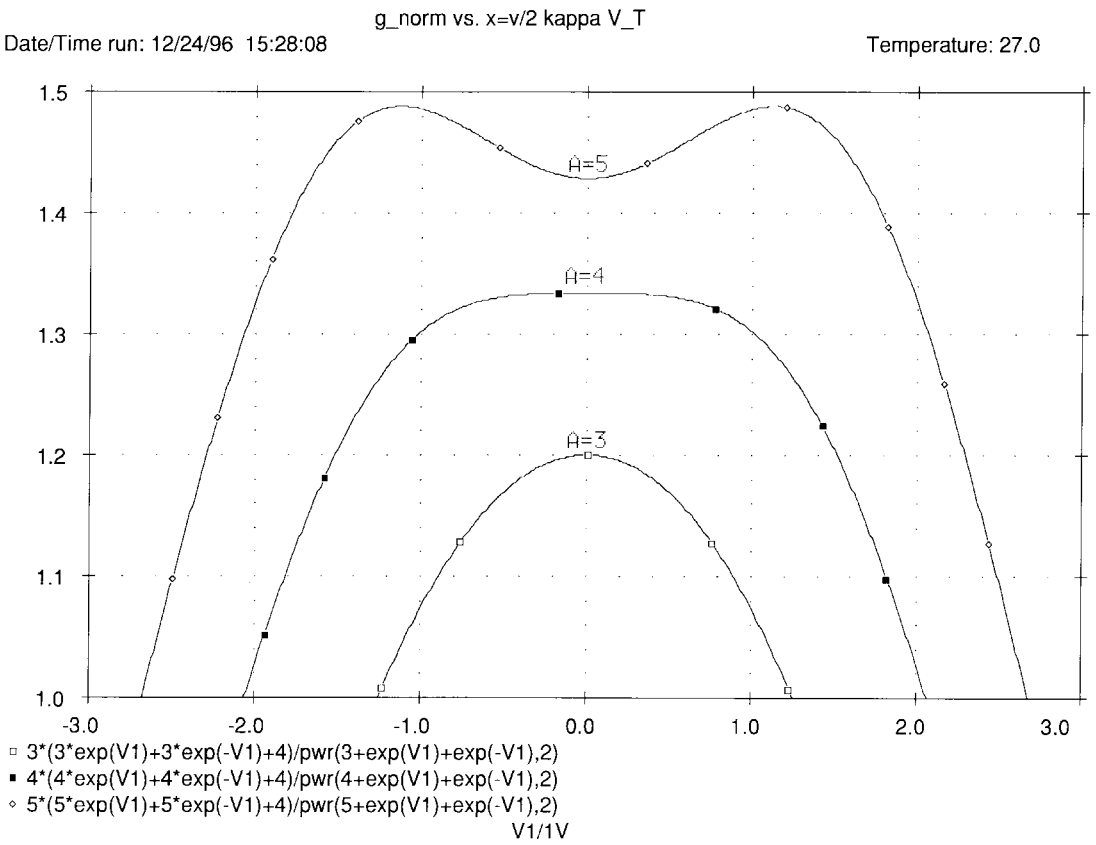

Fig. 2. $g_{\rm norm}$ versus $x = v/2\kappa V_T$.

A is the scale factor between the W/L ratios of M3 and the other transistors. Solving this system of equations gives

$$\frac{I_3}{I_{\rm hop}} = A\frac{e^x + e^{-x}}{A + e^x + e^{-x}} \tag{7}$$

and

$$\frac{I_1 - I_2}{I_{\rm hop}} = A\frac{e^x - e^{-x}}{A + e^x + e^{-x}}. \tag{8}$$

The derivative to x is

$$g_{\rm norm} = \frac{d\frac{I_1 - I_2}{I_{\rm hop}}}{dx} = A\frac{Ae^x + Ae^{-x} + 4}{(A + e^x + e^{-x})^2}. \tag{9}$$

The transconductance of the amplifier equals

$$G = \frac{I_{\rm hop}}{4\kappa V_T} g_{\rm norm}. \tag{10}$$

This is the transfer from the differential voltage to the current which would flow through a floating load.

When the scaling ratio A is large, M3 is biased deeply in the triode region and its output impedance is small. In this case, the dropping transconductance of the differential pair is overcompensated by the rising current through M3. The transconductance now first rises and then drops, as is shown by the upper graph in Fig. 2. The x coordinates of the resulting peaks in the transconductance can be found by taking the derivative of $g_{\rm norm}$ with respect to x, and equating this with zero. These x coordinates can then be substituted into the $g_{\rm norm}$ equation in order to find the peak value of $g_{\rm norm}$. The ratio of the transconductance in the peaks to the transconductance in balance $(x = 0)$ is found to be

$$k = \frac{g_{{\rm norm},p}}{g_{{\rm norm},0}} = \frac{A^2}{8(A-2)}. \tag{11}$$

For example, $A = 5$ gives $k = 25/24 \approx 1.0416$. The transconductance stays within the range from $G_{x=0}$ to $25/24 \cdot G_{x=0}$ for input voltages up to 3.34 κV_T $(x = 1.67)$, or about 130 mV at room temperature. $A = 4$ gives $k = 1$ and corresponds to the maximally flat case.

In this case, the large signal behavior is identical to the large signal behavior of a weak inversion version of the circuit with three transistors and two resistors described by Voorman [3, Fig. 4(b)], which requires $(A+2)/2$ times as much quiescent current for a given transconductance. The differential pair with a single diffuser described in [4] also has a very similar large signal behavior but a higher current usage, as has the circuit with four scaled differential pairs and maximally flat response described in [5]. It can be shown that all these circuits have a Groenewold noise factor $\xi = S(i_{n,\rm out})/(4kTG)$ [6], where G is the transconductance, between $\kappa/2 \approx 0.75$ and unity, so there is little difference in the noise behavior.

Unfortunately, the transconductance amplifier is rather sensitive to changes in the common-mode voltage at the input.

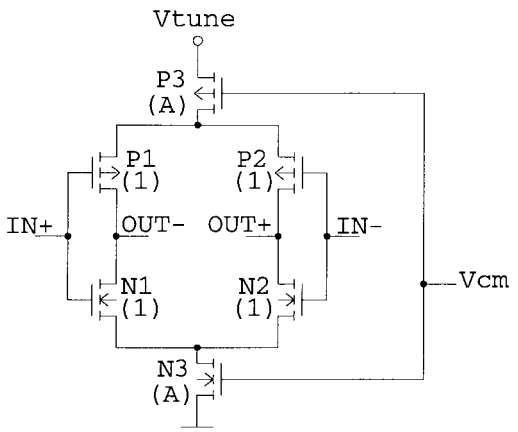

Fig. 3. The NP-version. All NMOS back gates are connected to ground, and all PMOS back gates are connected to Vtune.

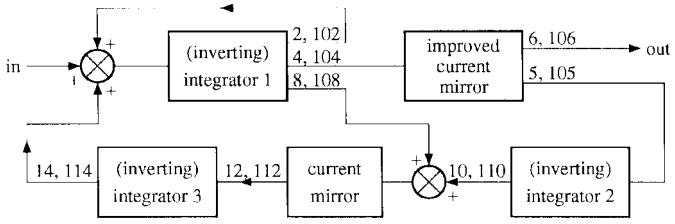

Fig. 4. Block schematic of the filter.

Further, the circuit produces common-mode signals at twice the signal frequency when it is driven (the current I_3 increases two times in each period of the signal). If these transconductance amplifiers are to be used in a transconductance-C filter structure, where the output of one amplifier drives the input of the next one, measures need to be taken to suppress these common-mode signals. Using common-mode loops is possible, but combining an N- and a P-version as in Fig. 3 is simpler.

When the circuit is driven, the current through N3 increases, but the current through P3 increases as well. These currents cancel if $\kappa_N = \kappa_P$ and partly cancel if $\kappa_N \approx \kappa_P$. When the common-mode voltage at the input increases, the transconductance of the N-side increases, but the transconductance of the P-side decreases. So there is a double improvement: the transconductance amplifier produces less common-mode current, and its transconductance becomes less sensitive to common-mode voltage changes [7], [8]. Also, the transconductance at a given supply current doubles. The power supply voltage now sets the quiescent current and thus the transconductance, and must be regulated. In a filter, the power supply voltage is the tuning voltage.

III. The Complete Filter

A block schematic of the filter is shown in Fig. 4. [The numbers 2, 102, and 4, 104, etc., correspond to the transistor numbers in the complete schematic diagram (Fig. 5)]. All integrators operate in the current domain, so the addition points are really just circuit nodes. Although the filter is a fully differential circuit, a single-ended block diagram has been drawn to keep the figure as simple as possible.

The filter is a third-order bandpass filter, which is equivalent to a cascade of a second-order high-pass $(Q \approx 1)$ and a first-order low-pass filter. The transfer equals

$$H = \frac{\omega_4 \alpha_6 s^2}{s^3 + \omega_2 s^2 + \omega_8 \alpha_{12} \omega_{14} s + \omega_4 \alpha_5 \omega_{10} \alpha_2 \omega_{14}} \tag{12}$$

where α_i is the transfer from the input of a current mirror to the output which is marked i, $100+i$. For example, α_{12} is the gain of the normal current mirror. The ω_i's are the unity-gain radian frequencies of the integrators, for example, ω_8 is the radian frequency at which the transfer from the input to the bottom output of integrator 1 is unity.

The complete filter circuit is shown in Fig. 5. Current mirrors are used to change the signal polarity. Because of the circuit being fully differential, the signal polarity could be changed by simply exchanging $+$ and $-$ outputs of the integrators. However, the common-mode transfer of the integrators is inverting and without mirrors, the feedback loop integrator 1–integrator 3 would give positive common-mode feedback, causing common-mode instability.

With current mirrors, the common-mode feedback is negative and makes the common-mode input voltages of the integrators settle at such a value that the currents through the P-sides of the transconductance amplifiers equal the currents through the N-sides. The gate voltage of the diode-connected NMOSFET N50 and PMOSFET P50 settle at the same value and could be used to bias the gates of P51, P52, P54, P55, P56 and the corresponding NMOSFET's. However, in order to avoid impractically large width-length ratios, the gates of the PMOS transistors have been biased at a somewhat lower voltage (node 50P) and the gates of the NMOS transistors at a somewhat higher voltage (node 50N). P57, P58, N57, and N58 are scaled transistors which generate these voltages.

When the ratio of the grounded capacitance to the floating capacitance is equal for all integrators and when the grounded capacitors are large enough, the phase margin of the common-mode loop is essentially equal to the phase margin of the differential-mode loop. In this case, the poles of the common-mode loop lie in the same positions as the differential-mode poles, except for a constant factor. By removing the grounded capacitors of the first integrator, the phase margin can be improved.

We want to use the filter to separate pulses from dc offset and interference. The interference mainly consists of a sine wave at a frequency well above the pass band. This sine wave may be amplitude modulated by a signal which is similar to the desired signal. If the interfering input current were much stronger than the desired signal, it could drive parts of the filter into clipping and it could be demodulated by even-order nonlinearities in an imperfectly balanced filter. Fortunately, its amplitude is smaller than or of the same order as the amplitude of the desired signal current, and it causes less voltage across Cfl1 due to its higher frequency. Hence, the linearity is not critical. The main requirement is that the nonlinearity should not cause more than 10% of compression of the peak value of the filtered pulse. With the 10% compression criterion, a

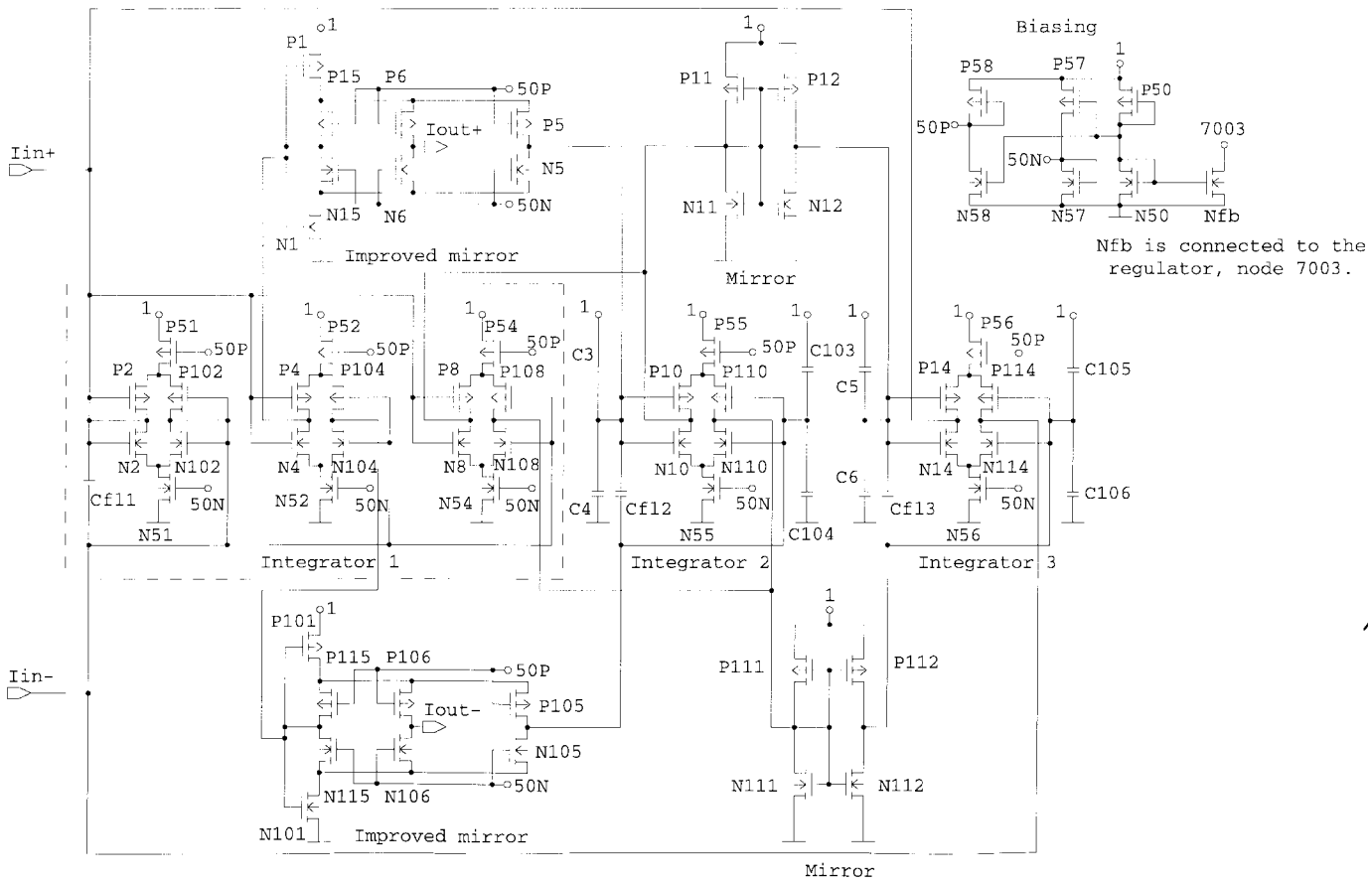

Fig. 5. The complete filter. All NMOS back gates are connected to ground, and all PMOS back gates are connected to the supply (node 1).

linearized transconductor with $A = 5$ can process 14.4 dB greater input signals than a normal differential pair.

The circuit N1, N15, N6, N5 and P1, P15, P6, P5 is a kind of improved current mirror which operates deeply in class AB. Class AB operation is necessary because the offset current at the output has to be very low for our application. In a class A current mirror, mismatch can cause serious offset currents.

A regular class AB current mirror is not good enough. The transistors in a regular mirror must all have a large gate area (around 900 μm^2), because the mismatch between small transistors tends to be large [9], which would make the gain inaccurate. Large transistors have large device capacitances, in combination with the very low class AB quiescent current (of the order of 30 pA), an unacceptably small bandwidth results.

In the improved circuit, the translinear current splitters N15-N6-N5 and P15-P6-P5 act as a feedback network around the high-gain amplifier N1-P1. The gate-bulk capacitances of N15-N6-N5 and P15-P6-P5 are all short-circuited, which is very desirable because in weak inversion, the gate-bulk capacitance is the largest device capacitance. N1 and P1 now limit the bandwidth, but they do not have an influence on the accuracy and can be made much smaller than the other transistors. Hence, the bandwidth of the mirror increases from 117 Hz to 1.72 kHz, according to simulations.

The supply voltage regulator is depicted in Fig. 6. It consists of a relatively fast voltage follower Npaar1-Npaar2-P1b-Preg1 which makes the supply voltage $V1$ of the filter equal to the voltage at Ccomp, and a slow control loop which adjusts the voltage at Ccomp until the current through Nfb (see Fig. 5) equals the tuning current I_{tune} mirrored by P_j2b and P_j3. The bias currents of the regulator are scaled versions of the tuning current.

In the actual application, the tuning current will be trimmed at the factory using a digital-to-analog converter (DAC). Because the circuit need only function over a small temperature range, there is no need to compensate for the temperature dependence. For operation over a large temperature range, the tuning current would have to be proportional to κV_T.

IV. Measurement Results

The circuit was realized in a standard 1.6-μm CMOS process with $V_{\text{TH},N} \approx 0.7$ V and $V_{\text{TH},P} \approx -1$ V. The ratio of the highest to the lowest cutoff frequency was somewhat lower than expected (about eight instead of ten), and the improved class AB current mirror produced some crossover distortion (see Fig. 7). This was not predicted by our simulation program, probably as a result of inadequate modeling of the drain-bulk and source-bulk capacitances. We expect that the crossover distortion can be reduced considerably by using narrower transistors in the translinear current splitters. Fortunately, distortion is not very important for our application.

The circuit uses 4.9 nA of current when it is tuned to 18 Hz and 142 Hz cutoff frequencies ($I_{\text{tune}} = 430$ pA). In the passband, the maximum signal level at the output is 500 pA$_{\text{rms}}$ (this refers to the current that would flow through

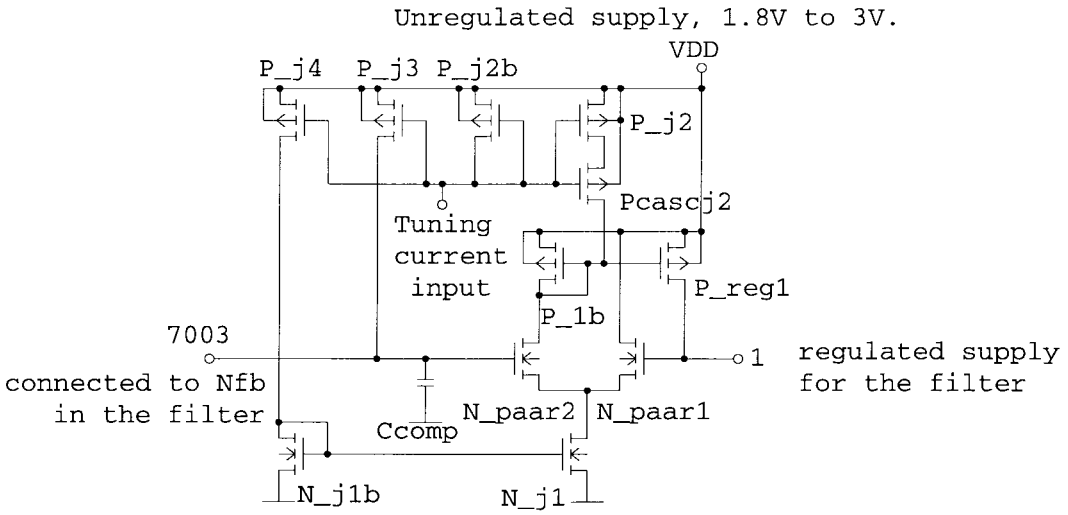

Fig. 6. The voltage regulator. All NMOS back gates are connected to ground.

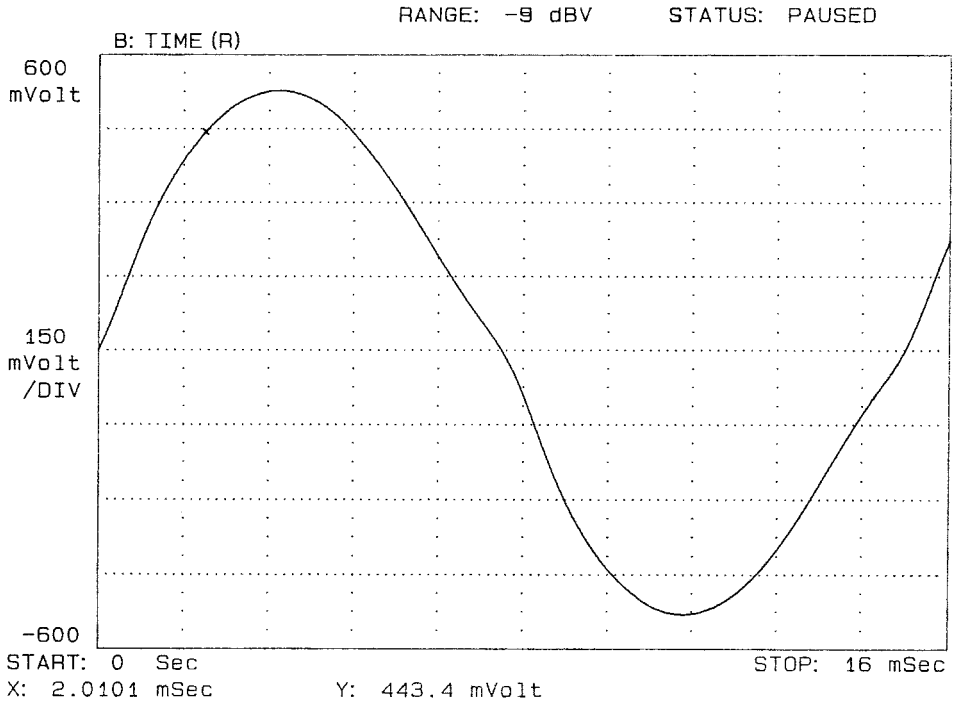

Fig. 7. A 67-Hz sine wave with crossover distortion. The Y-scale is 75 pA/div.

a floating load, that is half the difference between the output currents, and to the 10% compression point). The noise is 0.4 pA in a 500-Hz measurement bandwidth, so the dynamic range is 62 dB. To show that the circuit can be tuned over a wide range, Fig. 8 shows the frequency responses at 100 pA (upper graph), 4 nA (middle graph), and 10 nA (lower graph) tuning currents. The frequency scales are 1.25–126.25 Hz, 50–5050 Hz, and 125–12 625 Hz, respectively. The Y-axis settings are different for each measurement, but in all cases one division corresponds to 2 dB.

The total capacitance is 50 pF, and the chip area is 3.4 mm^2, or 0.5 mm^2 without the area taken by bonding pads, empty spaces between bonding pads, and electrostatic discharge (ESD) protection circuits. The performance of the filter is summarized in Table I.

TABLE I
PERFORMANCE OF THE FILTER (AT $I_{\rm tune} = 430$ pA UNLESS OTHERWISE NOTED)

Cutoff frequencies	18 Hz and 142 Hz
Maximum signal level (10% compression)	500 pA$_{\rm rms}$
Noise	0.4 pA at the output over 500 Hz
Dynamic range	62 dB
Supply current	4.9 nA
Supply voltage	1.8 V to 3 V
Tuning range	greater than 100 : 1
Chip area	0.5 mm^2 active, 3.4 mm^2 including bond pads

V. CONCLUSION

A low-power integrated bandpass filter has been presented. It is based on a new kind of linearized differential pair whose

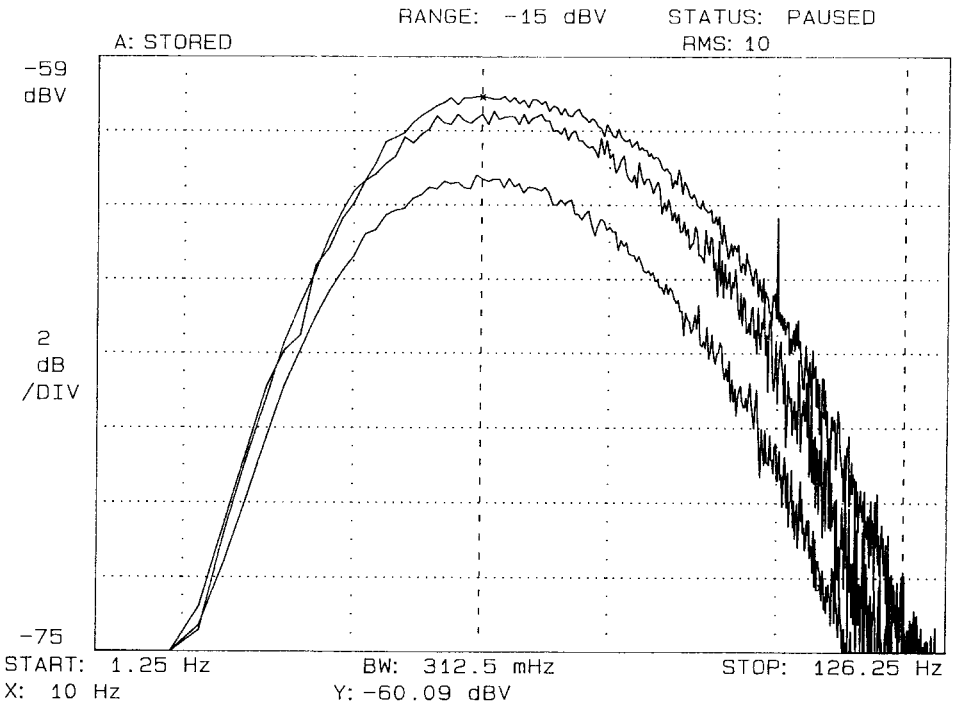

Fig. 8. The frequency responses at $I_{\rm tune} = 100$ pA, 4 nA, and 10 nA, at 1.25–126.25 Hz, 50–5050 Hz, and 12–12 625 Hz frequency scales, respectively. The vertical scales are different for each trace, but in all cases a division corresponds to 2 dB. The measurement was made with a periodic noise source and a fast Fourier transform (FFT) spectrum analyzer.

large signal behavior is similar to the large signal behavior of some circuits found in the literature, but whose supply current is substantially lower. The maximum input voltage of the transconductance amplifier is of the order of 130 mV. The filter has 18 Hz and 142 Hz cutoff frequencies, a 62 dB dynamic range, 50 pF of integration capacitance, and draws 4.9 nA of current from a 1.8-V supply.

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