

A Reduced-Area Low-Power Low-Voltage Single-Ended Differential Pair

J. Mulder, M. van de Gevel, and A. H. M. van Roermund

Abstract— In analog very large scale integratin (VLSI), a high computational density is important. Area savings can be obtained by operating the MOS transistor in the triode region, thus exploiting its symmetrical nature. Applying this theory to a single-ended differential pair results in an area reduction of up to a factor 1.5, which can be significant, e.g., for neural networks, where the basic cells are repeated many times on a single chip. The proposed circuit also has advantages with respect to low-power and low-voltage operation.

Index Terms—Analog VLSI, CMOS analog integrated circuits, neural network hardware.

I. INTRODUCTION

A HIGH computational density is of primary importance in analog neural networks and analog very large scale integratin (VLSI) systems in general [1]. The area required for the implementation of a certain function can often be reduced by exploiting the full functional capacity offered by the MOS transistor. One possibility is to use the body terminal as a second gate [2]–[4]. Another possibility is to use the drain terminal, by operating the MOS transistor in the triode region, instead of in the saturation region [5]–[7].

In this paper, the triode region option is applied to the differential pair. A novel differential pair is proposed which might be interesting, especially for analog neural network applications, where the differential pair is used very often in neurons and synapses, for amplification, to implement the sigmoid function and to facilitate multiplication, e.g., [8]–[10]. Because neurons and especially synapses are repeated many times on a single VLSI neural network chip, area savings in these basic cells becomes significant.

In Section II of this paper, the triode region and the saturation region of the MOS transistor are compared with respect to functionality and a functional relation between the two regions is derived. This theory is applied to the differential pair, in Section III, resulting in the design of a reduced-area low-power low-voltage single-ended differential pair. Measurements in both the weak and strong inversion region are described in Section IV, which verify the operation of the circuit.

II. MOS TRANSISTOR IN THE TRIODE REGION

A striking characteristic of the MOS transistor is its symmetry with respect to source and drain. This symmetry is apparent from the equation for the drain current I_{DS} in the triode region. The drain current can be written as the difference of a forward

current I_F , which is a function of the source voltage V_S , and a reverse current I_R , which is a function of the drain voltage V_D . In the weak inversion triode region, with the substrate connected to ground, the drain current is given by [11]–[13]

$$I_{DS} = \frac{W}{L} I_o \exp\left(\frac{V_G}{nV_T}\right) \left[\exp\left(\frac{-V_S}{V_T}\right) - \exp\left(\frac{-V_D}{V_T}\right) \right] = I_F - I_R \quad (1)$$

where W and L are the width and length of the transistor, I_o is the zero-bias current, n is the subthreshold slope factor, V_T is the thermal voltage kT/q and V_G , V_D , and V_S are the gate, drain, and source voltage, respectively, referenced to the substrate.

In the strong inversion triode region, the MOS transistor shows the same symmetry with respect to its source and drain. The drain current in the strong inversion triode region is given by [12], [13]

$$I_{DS} = \frac{W}{L} \frac{\beta}{2} [(V_G - V_S - V_{th})^2 - (V_G - V_D - V_{th})^2] = I_F - I_R \quad (2)$$

where β is the transconductance factor and V_{th} is the threshold voltage.

Further, (1) and (2) are very similar to the equations for the drain current in the saturation region. The reverse current I_R tends to zero when $V_D \gg V_T$ or $V_D > V_G - V_{th}$, in the weak and strong inversion regions, respectively.

In the weak inversion saturation region, the drain current is described by [11]–[13]

$$I_{DS} = \frac{W}{L} I_o \exp\left(\frac{V_G}{nV_T}\right) \exp\left(\frac{-V_S}{V_T}\right) = I_F. \quad (3)$$

And in the strong inversion saturation region, I_{DS} is given by

$$I_{DS} = \frac{W}{L} \frac{\beta}{2} (V_G - V_S - V_{th})^2 = I_F. \quad (4)$$

Note that (3) and (4) are in fact *simplified* versions of (1) and (2). As a consequence, the functional capacity of an MOS transistor operating in the triode region is higher than the functional capacity of an MOS transistor operating in the saturation region, where the drain terminal has lost control over the drain current.

More specifically: *One transistor operating in the triode region is equivalent to two fictitious transistors operating in the saturation region.* The drain current of one fictitious transistor is I_F and the drain current of the other fictitious transistor is I_R .

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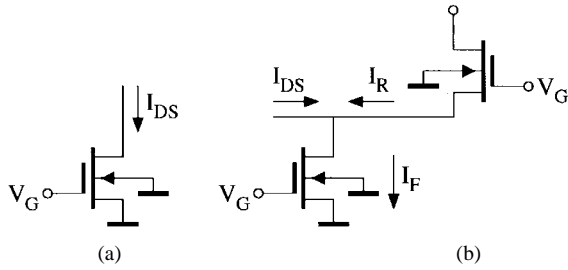


Fig. 1. Equivalence of: (a) one transistor operating in the triode region and (b) two transistors operating in the saturation region.

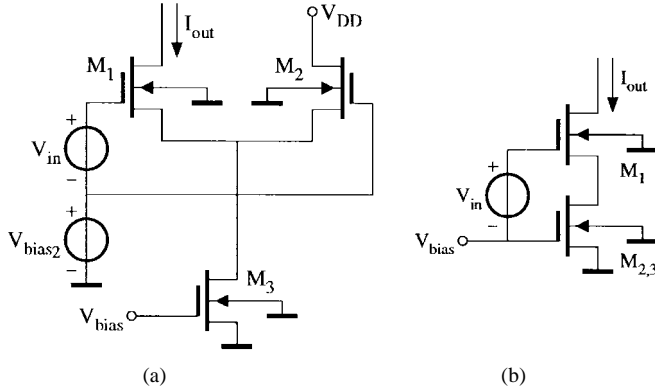


Fig. 2. (a) Conventional and (b) novel single-ended differential pair.

Since the difference of the fictitious drain currents I_F and I_R has to equal the actual drain current I_{DS} , see (1) and (2), it follows from Kirchhoff's Current Law that the drain of one fictitious transistor is connected to the source of the other fictitious transistor. This is illustrated in Fig. 1.

Further, both fictitious transistors have the same gate and substrate potential, and the same aspect ratio W/L , which follows directly from (1)–(4).

III. CIRCUIT DESCRIPTION

A differential pair is biased by a tail current source. In practice, this source is often implemented by a single transistor, which is biased at a certain gate voltage, in most cases the input voltage of a simple current mirror. A single-ended differential pair is shown in Fig. 2(a), where all MOS transistors operate in the saturation region.

The equivalence derived in the preceding section can be exploited to simplify this differential pair. Since the two transistors M_2 and M_3 , which operate in the saturation region, are biased at a dc gate voltage, and the source of M_2 is connected to the drain of M_3 , they can be combined into one MOS transistor operating in the triode region. The novel single-ended differential pair thus obtained is shown in Fig. 2(b). The circuit has a single-ended input and output, but in many situations this limitation poses no problem.

The proposed circuit looks very similar to a differential voltage amplifier published by Johnson in [14], shown in Fig. 3, and therefore, it might be interesting to highlight the differences between these circuits.

First, the body terminal of M_{21} , shown in Fig. 3, is connected to its source. The body terminals of all transistors

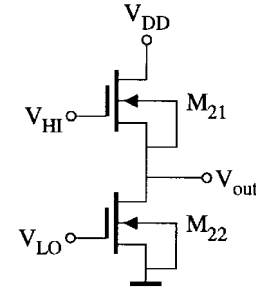


Fig. 3. Differential voltage amplifier [14].

shown in Fig. 2 are connected to ground. The equivalence relation between M_2 and M_3 in Fig. 2(a) and $M_{2,3}$ in Fig. 2(b) is only valid if M_2 and M_3 have the same body potential, as explained in the previous section.

Second, both transistors M_{21} and M_{22} , shown in Fig. 3, operate in the (strong inversion) *saturation* region. Transistor $M_{2,3}$, shown in Fig. 2(b) operates in the *triode* region.

As a result of the above two differences, the proposed circuit has a completely different transfer function than Johnson's circuit. The circuit shown in Fig. 3 acts as a differential voltage amplifier with unity gain. The output *voltage* V_{out} equals the difference of the two input voltages V_{HI} and V_{LO} . The output signal of the proposed differential pair is a *current*. The transfer function describing the relation between the input voltage V_{in} and the output current I_{out} is exactly equal to the transfer function of the conventional differential pair. Only for very large values of V_{in} , when the differential pair is used beyond its usual range of operation, do the circuits become identical, except for the body terminal connection of M_{21} .

An expression for the output current I_{out} of the proposed differential pair can be found by applying (1)–(4) to the differential pair shown in Fig. 2(b). Applying (1) and (3), valid in the weak inversion region, to $M_{2,3}$ and M_1 , respectively, yields

$$I_{out} = \frac{W}{L} I_o \exp\left(\frac{V_{bias}}{nV_T}\right) \left[1 - \exp\left(\frac{-V_{S1}}{V_T}\right)\right] \quad (5)$$

$$I_{out} = \frac{W}{L} I_o \exp\left(\frac{V_{bias} + V_{in}}{nV_T}\right) \exp\left(\frac{-V_{S1}}{V_T}\right) \quad (6)$$

where V_{S1} is the source voltage of M_1 .

Since V_{bias} is assumed to be the input voltage of a current mirror, we can find an expression for V_{bias} in terms of the input current I_{bias} of this current mirror, using (3)

$$V_{bias} = nV_T \ln\left(\frac{L}{W} \frac{I_{bias}}{I_o}\right). \quad (7)$$

We can use this equation to eliminate V_{bias} from (5) and (6). Further, a closed expression for I_{out} can be obtained by elimination of V_{S1} from (5) and (6). This yields

$$I_{out} = \frac{1}{2} I_{bias} \left[1 + \tanh\left(\frac{V_{in}}{2nV_T}\right)\right]. \quad (8)$$

This equation is exactly equal to the equation describing the conventional differential pair shown in Fig. 2(a). Since the large-signal transfer function is identical, the small-signal

transconductance gain of the proposed differential pair will also be equal to the gain of the conventional differential pair.

In strong inversion, two equations for I_{out} are found by applying (2) and (4) to $M_{2,3}$ and M_1 , respectively

$$I_{out} = \frac{W}{L} \frac{\beta}{2} [(V_{bias} - V_{th})^2 - (V_{bias} - V_{S1} - V_{th})^2] \quad (9)$$

$$I_{out} = \frac{W}{L} \frac{\beta}{2} (V_{bias} + V_{in} - V_{S1} - V_{th})^2. \quad (10)$$

From these expressions, V_{bias} can again be eliminated, if we assume V_{bias} to be the input voltage of a current mirror, given by

$$V_{bias} = \sqrt{\frac{L}{W} \frac{2}{\beta} I_{bias}} + V_{th}. \quad (11)$$

Next, a closed expression for I_{out} is found by eliminating V_{S1} from (9) and (10)

$$I_{out} = \frac{I_{bias}}{2} - \frac{W}{L} \frac{\beta}{2} V_{in} \sqrt{\frac{L}{\beta W} I_{bias} - \left(\frac{V_{in}}{2}\right)^2}. \quad (12)$$

This equation is exactly equivalent to the transfer function of the conventional differential pair in strong inversion.

For analog VLSI applications, the most important advantage of the proposed circuit is a reduction of the required chip area. Instead of two transistors M_2 and M_3 , with equal aspect ratio, only one transistor $M_{2,3}$ is necessary. If M_1 , M_2 , and M_3 have equal dimensions, the required area is reduced by a factor of about 1.5.

The proposed differential pair also has advantages with respect to low-voltage and low-power operation. First, no voltage has to be wasted on keeping M_3 in the saturation region. In weak inversion, about 100 mV for both the input and the output voltage range is gained, which is significant, e.g., for single-battery operation where the supply voltage can be as low as 1 V [15].

Second, the total current consumption is equal to the output current and not to the tail current, which comes down to a factor of one half at the bias point; see (8) and (9).

IV. MEASUREMENT RESULTS

Measurements were performed, using a transistor array, to verify the principle described above. Transistors from a standard 2.5- μm process were used. The typical values of the most important parameters are $V_{th} = 0.75$ V, $\beta = 48 \mu\text{A}/\text{V}^2$, and the K-factor, modeling the body-effect, is $0.28\sqrt{V}$. The dimensions of the transistors used are $W = 108 \mu\text{m}$ and $L = 7 \mu\text{m}$.

Measurements were performed both for operation in the weak and in the strong inversion region, by biasing the circuit at $V_{bias} = 0.5$ and 0.9 V, respectively. The results are shown in Fig. 4. Both figures clearly show the well-known input-output characteristic of the differential pair in weak and in strong inversion.

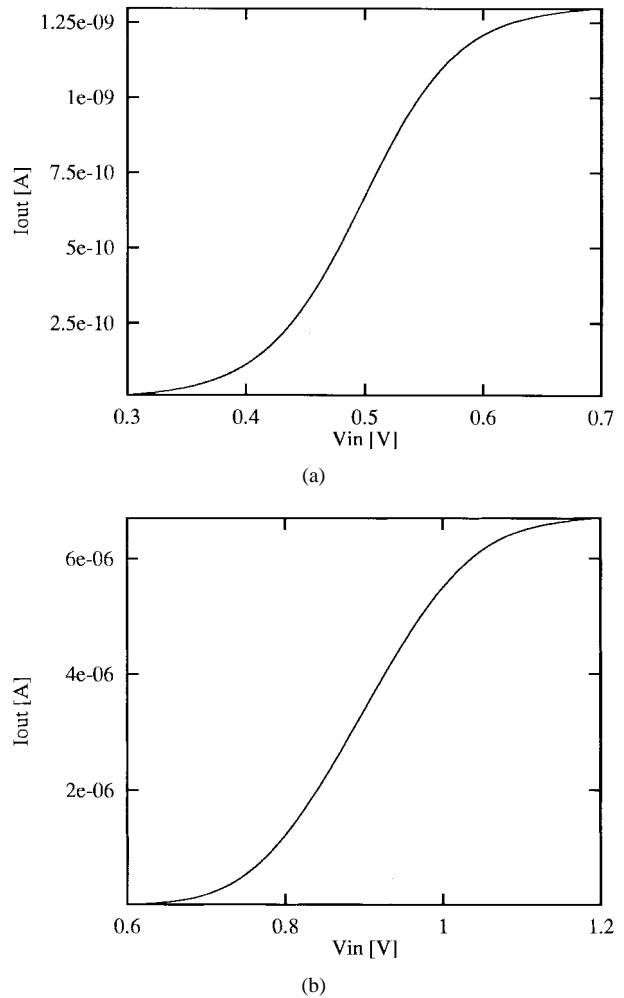


Fig. 4. Measured output current: (a) weak and (b) strong inversion.

V. CONCLUSIONS

By exploiting the relation between the operation of an MOS transistor in the saturation and in the triode region, a higher functional density can be obtained. This was demonstrated for the single-ended differential pair, where the required area is reduced by a factor of up to 1.5, which can be significant in analog VLSI applications, e.g., in neural networks, where the differential pair is often used in neurons and synapses, which are repeated many times on a chip. Other advantages of the proposed differential pair are low-power and low-voltage operation.

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