Regular Brief Papers

Low-Voltage Low-Power Controllable Preamplifier for Electret Microphones

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***Abstract*—A low-voltage low-power analog controllable preamplifier for electret microphones is presented. It has been designed for a single supply voltage of 1.0 V, whereas its average power consumption amounts to some tens of microwatts. A dc current controls its gain directly into decibels. The design meets specifications (listed in Section I) concerning accuracy, bandwidth, noise properties, etc., suitable for most applications in portable telephone equipment, portable transceivers, hearing aids, etc. Much attention has been paid to the dynamic range of the input signal, noise, and offset properties. The circuit has been realized in a semi-custom IC process. Simulation and measurement data of the most important properties are presented.**

I. Introduction and Specifications

During the last decade analog circuits operating at extremely low supply voltages and consuming minimal power have gained much interest. Typical application areas are portable transceivers, portable telephone equipment, and hearing aids. This paper describes the design of a low-voltage/low-power preamplifier for electret microphones, whose gain can be controlled by an analog current. It can operate with a single supply source of 1.0 V, whereas its average power consumption has been minimized. A typical practical problem in the application areas is the large dynamic range of the acoustic input signals. Typical sound pressure levels are between 57 dB (SPL) and 105 dB (SPL) corresponding with typical microphone voltages of $\cong 300\,\mu V_{rms}$ and $\cong 75$ mV_{rms} over 3.5 kΩ, respectively. Therefore, much attention has been paid to the input capability of the amplifier and its noise properties. To restrict harmonic distortion, the input and output signals of the amplifier operate at current level. Hence, the output of the microphone is short-circuited and the sensed current (varying from ≈ 86 nA_{rms} to $\approx 21.5\,\mu A_{rms}$) is amplified, whereas the output delivers a signal current of 1 μA_{peak} after any gain correction.

A. Further Specifications

Bandwidth: 100 Hz to 10 kHz
THD (1 kHz): <7% (maximum output)
Control range: 48 dB
Control resolution: <1.5 dB
Control curve: Exponential
Equivalent input noise: Below the limits shown in Fig. 1.[1]

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[1] Received from "Philips Hearing Instruments," The Netherlands.

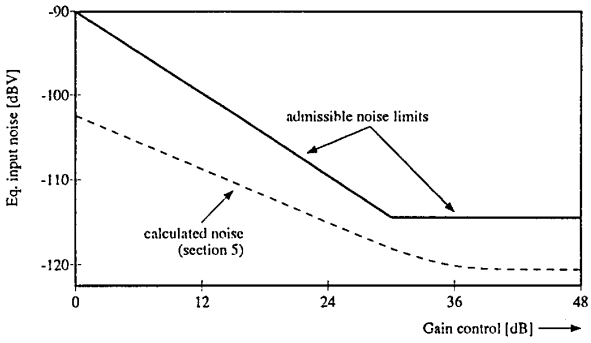


Fig. 1. Admissible noise limits.

B. Process Choice

As the exponential relationship between the collector current and the base–emitter voltage in bipolar devices offers a great advantage in the present design (Section II), a bipolar process has been chosen. The ultimate circuit has been realized in a standard semi-custom process. Only two transistor types are used: a small n-p-n and a lateral p-n-p.

II. Choice of the Basic Circuit Configuration

A. General; Choice of the Values of the Reference Sources

The most commonly employed principle for controllable amplifiers is known as the OTA principle. However, it shows an overwhelming drawback in low-power circuits, because large input signals modulate the control quantity. Hence, linearity is conflicting with power efficiency. Well-known linearization techniques [1] result in complicated and critical circuits. Fig. 2 depicts a totally different solution, where this basic nonlinearity is absent. The amplifier contains a gain-controlled current mirror with the transistors and Q_1 and Q_2 and the additional current amplifier A_i, whereas Q_3–Q_6 deliver the correct value of $I_c(Q_1)$ so that $I_c(Q_2)/I_c(Q_1) = I_o/I_s$ at any gain. Its current gain amounts to

$$\ln |I_o/I_s| = (V_1 - V_2)/V_T$$

or

$$20 \log |I_o/I_s| \approx 334\,(V_1 - V_2)\,[\text{dB}] \qquad (1)$$

where $V_1 - V_2$ is the control voltage. The control quantity and the input signal are independent now. In the present case I_s varies 48 dB, whereas I_o is constant. Hence, for offset and efficiency reasons V_1 should be chosen constant and V_2 the

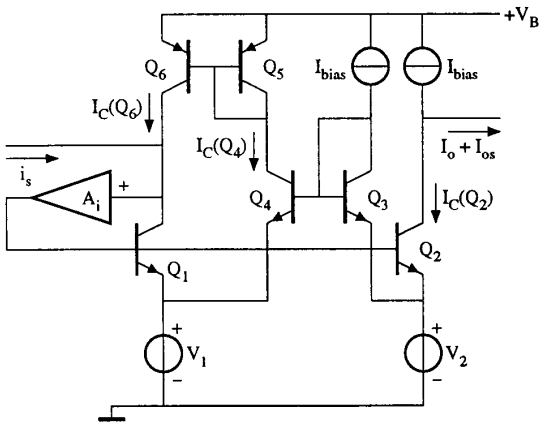


Fig. 2. Basic circuit configuration.

controlling quantity. (Note that the gain in decibels is *inversely* proportional to $V_1 - V_2$.) $I_c(Q_1)$ only has large values at large input signals, whereas $I_c(Q_2)$ remains small. Hence, the configuration is superior with respect to its average efficiency. As the maximal output signal current is 1 μA_{peak}, $I_c(Q_2)$ has been chosen to be 1.5 μA. The gain range follows from the limits of I_s: from −29.6 dB up to +18.3 dB, resulting in a voltage sweep $V_1 - V_2 \approx 144$ mV. V_1 has been chosen to be 65 mV (Section III) so that V_2 must be variable from ≈10 to ≈154 mV. V_1 and V_2 should preferably be PTAT, so that the gain is temperature independent. The extra current amplifier A_i lowers the input resistance of Q_1 with a factor $A_i > 1000$, so that the source is perfectly short-circuited at any control position.

B. Noise Properties (Circuit in Fig. 2)

If I_{bias} and A_i are supposed to give negligible noise contribution, total equivalent rms input noise voltage yields, after some calculation

$$V_{n(t)}(\text{rms}) = ([2kT\{1/g_{m2} + R_s^2 g_{m2}(1/N + 1/N^2)\}]\Delta f)^{1/2} \quad (2)$$

where g_{m2} is the transconductance of Q_2, Δf is the bandwidth, and N is the gain. After substitution of some values and insertion of them into Fig. 1 (dashes), we observe that there is a wide margin between the desired and the calculated noise, lowering the demands for additional noise caused by A_i and I_{bias}.

C. Offset Calculation

Disregarding the effects of mismatch the offset current in Fig. 2 yields

$$I_{os} = I_{bias}\left[1 - \frac{N}{\{1 + 2/h_{FE(p)}\}\{N + (1+N)/h_{FE(n)}\}}\right]. \quad (3)$$

In the applied process $h_{FE(p)}$ (min) and $h_{FE(n)}$ (min) are 15 and 70, resulting in maximum offset currents of $I_{os} = 0.39 I_{bias}$ (at minimum gain) and $0.13\, I_{bias}$ (at maximum gain). As these values are too large, the offset properties must be improved. This will be effectuated by offset feedback and offset compensation (Section III).

III. The Complete Circuit

Fig. 3 depicts the complete circuit including offset reduction, the implementation of A_i, and the reference sources.

A. Offset Reduction

Offset feedback is effectuated by copying I_o by Q_{11} and feeding it back via a low-pass filter (C_t, R_t). The dynamic behavior can easily be calculated with the aid of the simplified diagram of Fig. 4. The results is

$$I_o/I_s = \frac{\{N/(1+NM)\}\{(sR_sC_s(1+sR_tC_t)\}}{\{1 + sR_tC_t/(1+NM)\}(1+sR_sC_s)}. \quad (4)$$

The transfer shows two zeros and two poles $p_{1,2}$. A reasonable choice for the frequencies of both poles is $f(p_1) = f(p_2) = 50$ Hz at maximum gain ($N = 8.2$). Taking other design qualities into account, good choices for C_s, R_t, C_t, and the scaling factor M are 1 μF, 500 kΩ, 100 nF, and 2, respectively.

The offset feedback is only effective if the loop gain $M \cdot N > 1$ (hence at gain levels $|N| > 1/2$). At lower values we resort to offset *compensation*. The offset caused by the p-n-p mirror Q_5, Q_6 can be coped with by adding an extra current mirror (Q_{12}, Q_{13}), so that the collector currents of Q_2 and Q_1 are derived from identical sources. This modification has been inserted in Fig. 3.

B. The Extra Current Amplifier (A_i)

A simple solution is found in a cascade of two CE stages (Q_9 and Q_{10} in Fig. 3). The added current gain then amounts to β_{ac}^2, which exceeds the demand. Two RC compensation networks from the bases of Q_9 and Q_{10} to ground accomplish stable operation in all circumstances.

C. The Voltage and Current Sources

As $I_c(Q_2)$ is constant and small, V_2 is allowed to be rather high-ohmic. However, to prevent extra distortion, V_2 must be low-ohmic. Although very low-ohmic sources can easily be designed, the loose distortion demands make the simple solutions in Fig. 3 feasible. V_2 is realized by a current-fed resistor, whereas for V_1 a saturated transistor with "forced beta" is used (Q_8). V_1 is a PTAT voltage, independent of $I_c(Q_1)$ provided that I_c/I_B is kept constant (=5, accomplished by the current mirror Q_5, Q_7 in Fig. 3) and that the collector bulk resistance can be disregarded (large transistor) [2]. In the applied transistor process $V_{sat} \approx 65$ mV at $I_C/I_B = 5$. The output resistance appears to be in the order of $1/g_m(Q_1)$. This is low enough to prevent excessive distortion. As the emitter current of Q_1 equals the collector current of Q_8, this solution hardly needs extra supply current. To restrict additional noise, bias currents are derived from the central bias current I_{bias} (=4.5 μA) by down-scaling. The control current varies from 4 to 64 μA, yielding the desired limits of V_2 (10–154 mV). Because

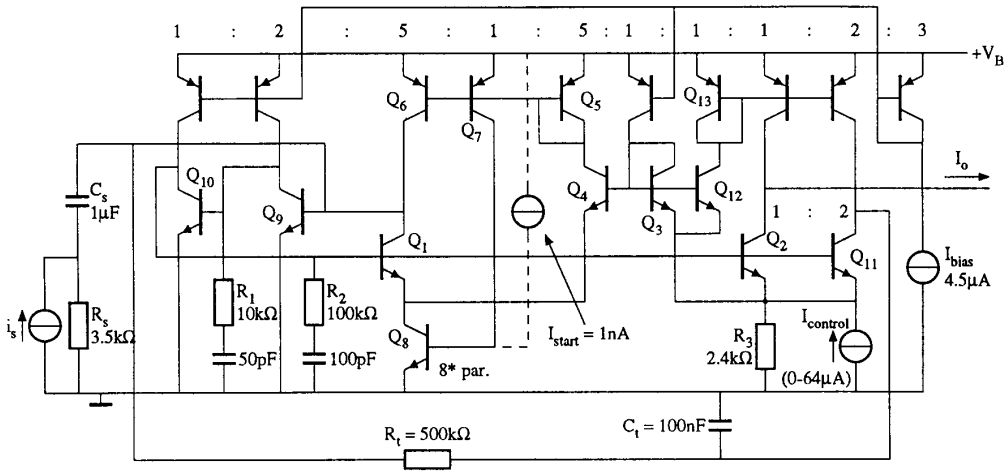


Fig. 3. Complete circuit.

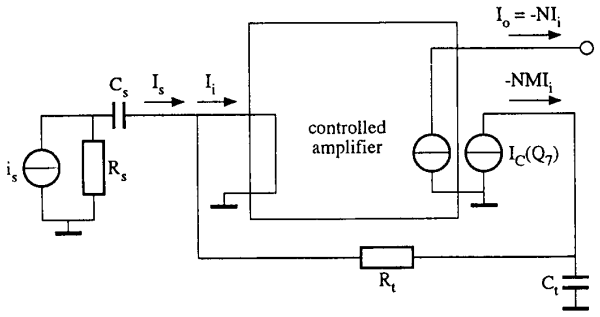


Fig. 4. Simplified circuit for offset calculation.

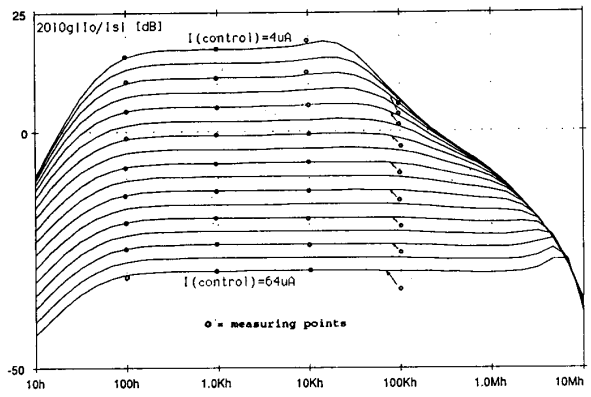


Fig. 5. Simulated and measured gain as a function of frequency. The control current was varied from 4 to 64 μA.

the circuit containing Q_1, Q_6, Q_7, and Q_8 has a second stable biasing condition, where all currents are zero, a starting current (I_{start}=1 nA) has to be added (dashed in Fig. 3).

IV. SPICE Simulations and Measurement Results with a Semi-Custom Chip

A. Frequency Transfers as a Function of the Control Current (Fig. 5) (Gain Step: 3 dB)

At any controlled gain the bandwidth is sufficiently large. Deviations between simulated and measured values at higher frequencies are probably caused by inadequate high-frequency characterization of the employed transistor models at very low bias currents.

B. Simulated and Measured Offset

Fig. 6 depicts the simulated and measured output offset current as a function of the controlled gain. As shown, the offset remains below 2% of I_o(peak).

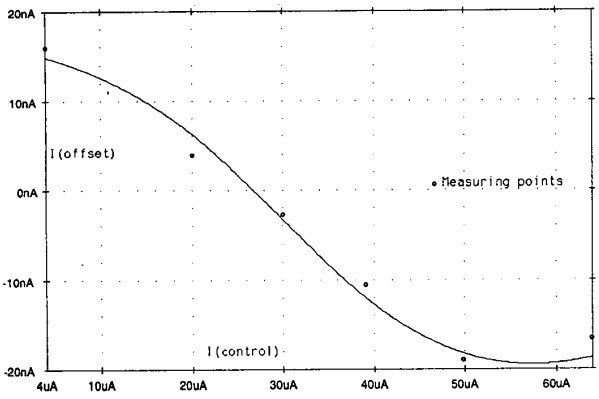


Fig. 6. Simulated and measured offset as a function of gain.

C. Simulated Input Noise Spectra; Measured Output Noise and Distortion

The spectra of the equivalent input noise voltage versus gain are shown in Fig. 7. The rms input noise voltages calculated

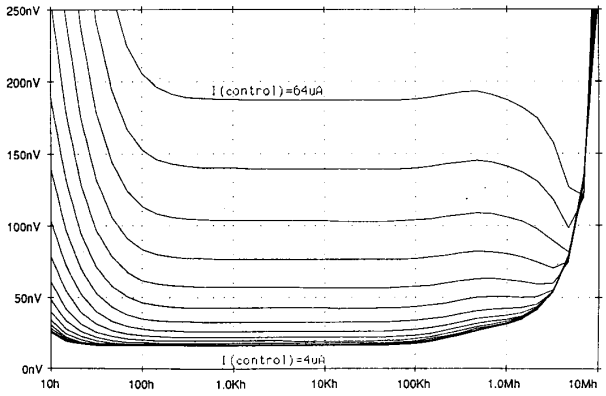


Fig. 7. Simulated equivalent input noise spectra as a function of gain.

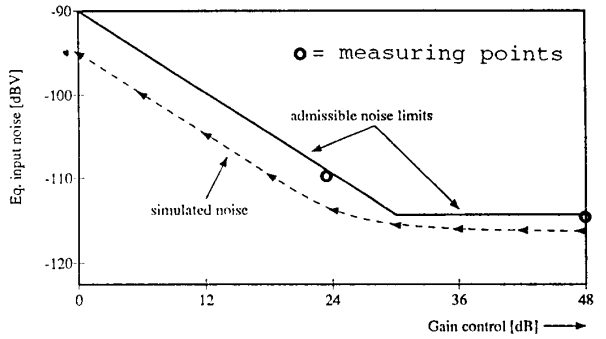


Fig. 8. RMS input noise voltage as a function of gain.

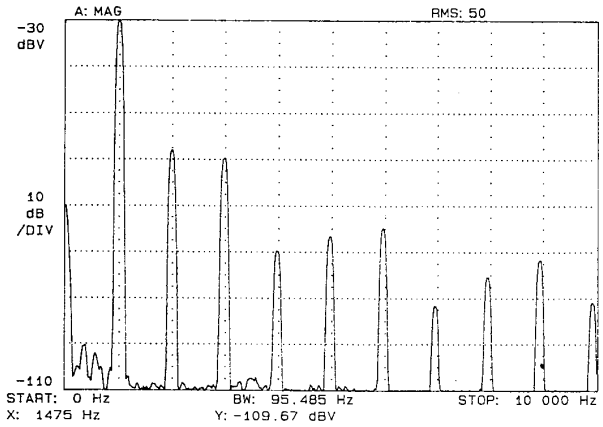
from these curves are shown in Fig. 8 (redrawn from Fig. 1). Fig. 9(a) through (c) shows the measured output spectra with a 1-kHz input signal at maximum output and three gain positions: 0, 24, and 48 dB. The noise floors (only at 24 and 48 dB, the noise at 0-dB gain was not measurable) have been converted into equivalent input voltages and added to Fig. 8. THD remains below 7% in all cases.

D. Supply Current

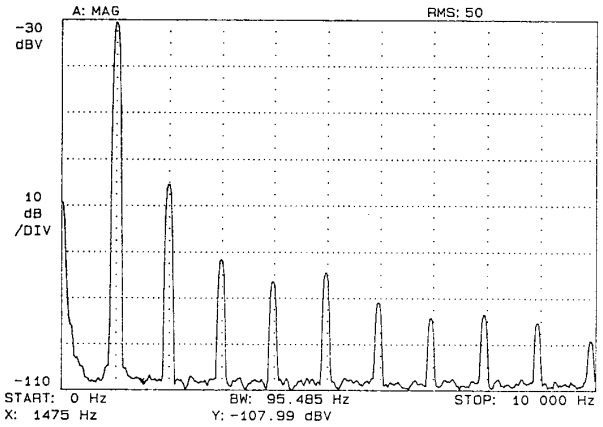
The supply current (including the control current) varies from 17.5 μA at maximal gain to 164 μA at minimal gain. Because the amplifier will hardly ever be used at minimal gain, the average power consumption will be small in practice (some tens of microwatts).

V. Conclusions

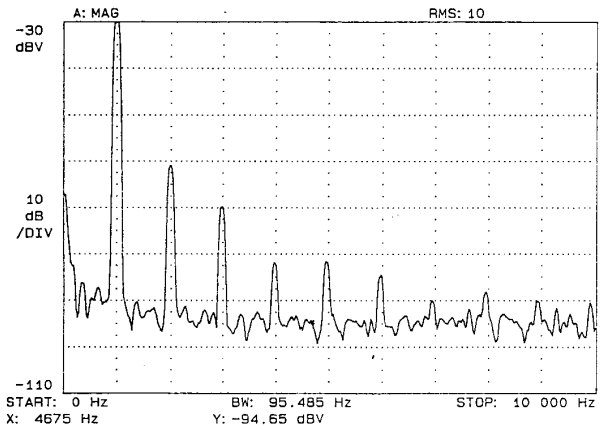
A controllable preamplifier for electret microphones has been presented. The amplifier is biased with a single supply voltage of 1 V. Its gain control is effectuated with a dc current directly into decibels. The amplifier operates at current level and can handle very large input signals, whereas the average power consumption remains small. Its dynamic range and linearity meet most common specifications in the production areas of hand-carried equipment, hearing aids, etc.



(a)



(b)



(c)

Fig. 9. Measured output spectra at gain positions of (a) 0 dB, (b) 24 dB, and (c) 48 dB.

References

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[2] I. E. Getreu, *Modeling the Bipolar Transistor*, New York: Elsevier, Scientific, 1978.