Design of Adaptive Multimode RF Front-End Circuits

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***Abstract*—Migration towards higher data rates and higher capacities for multimedia applications, and provision of various services (text, audio, video) from different wireless standards with the same device require integrated designs that work across multiple standards, can easily be reused, and achieve maximum hardware share at minimum power consumption. This can be achieved by using adaptive circuits that are able to trade off power consumption for performance. The design of an adaptive multimode image-reject downconverter (oscillator and two mixers) is presented in this paper. In the highest performance mode, the image-reject downconverter (the quadrature mixers) has an IIP3 of +5.5 dBm, a single-side band noise figure of 13.9 dB and a conversion gain of 1.4 dB, while drawing 10 mA from a 3 V supply. The adaptive oscillator achieves −123 dBc/Hz phase noise at 1 MHz offset from a 2.1 GHz carrier with a bias current of 6 mA in the highest performance mode. Adaptivity in the downconverter is achieved by trading off RF performance for current consumption, ranging from 10 mA for the relaxed mode (e.g., DECT) to 20 mA in the highest performance mode (e.g., DCS1800) of operation.**

***Index Terms*—Adaptive circuits, image-reject downconverter, mixer, multistandard circuits, RF front-end, voltage-controlled oscillator.**

I. Introduction

TODAY'S portable communication devices enable a growing variety of applications, ranging from text messaging, telephony and audio to full video. These modern wireless devices must maintain connectivity, they must track position, and may (in the near future) be wearable rather than just portable. However, the energy supply for portable devices is fixed by the size and weight of the batteries in a hand-held device. Consequently, the current consumption of circuitry in multistandard and multifunctional handhelds must be reduced in order to meet increasing functional and concurrent operational requirements. This can be achieved by using *adaptive circuits* that are able to trade RF performance (e.g., gain, noise figure, linearity) for power consumption on the fly. Realization of adaptivity functions requires scaling of current consumption to the demands of the signal-processing task [1].

The results of an exploratory multimode adaptive (MMA) image-reject (IR) downconverter circuit for a radio frequency (RF) front-end are described in this paper. This quadrature downconverter (comprising an oscillator and two mixers) allows adaptation between different operating modes by trading RF performance for current consumption in an adaptive way.

Section II outlines the application of adaptivity to multistandard low-power wireless RF circuits. Section III describes a multimode receiver concept in the framework of second- and third-generation communication standards. The design of the adaptive quadrature downconverter circuits used in the experimental implementation is described in Section IV. Measurement results of the multimode test circuit presented in Section V demonstrate a factor of approximately two saving in power consumption when adaptivity is employed in the multimode receiver.

II. Adaptive Multimode Low-Power Wireless RF IC Design

Mobile wireless equipment today is shaped by user/application demands and RF microelectronics.

Progress in silicon integrated circuit (IC) technology [2] and innovations in IC design have enabled mobile products and services [3], [4]. Wireless systems for new applications [5]–[9] require an extension of the capabilities for these RF devices, creating an opportunity for low-power adaptive and multifunctional RF ICs.

A. Low-Power and Adaptive RF Circuit Design

The communication devices of the near future will not only have to support applications ranging from text, telephony, audio, and graphics to video, but they will also have to maintain connections with many other devices in a variety of environments. Moreover, they should be position aware, and perhaps wearable rather than just portable [10]–[12].

A combination of multiple functional requirements and limited energy supply from a battery is an argument for the design of both adaptive low-power hardware and software [10], [11].

An adaptive design approach poses unique challenges: from hardware design to application software, and ultimately throughout all layers of the underlying communication protocol [10]–[15].

A block diagram for the receiver in an adaptive mobile device is shown in Fig. 1. This receiver consists of adaptive analog RF front-end circuitry, adaptive analog baseband circuitry, and an adaptive digital signal processor in the back-end.

Whereas the transceiver circuits determine instantaneous power consumption, the average power consumption depends on the power management of the complete system [12]. This implies that not only local, but also global power optimization and awareness (i.e., at all layers and at all times) are important

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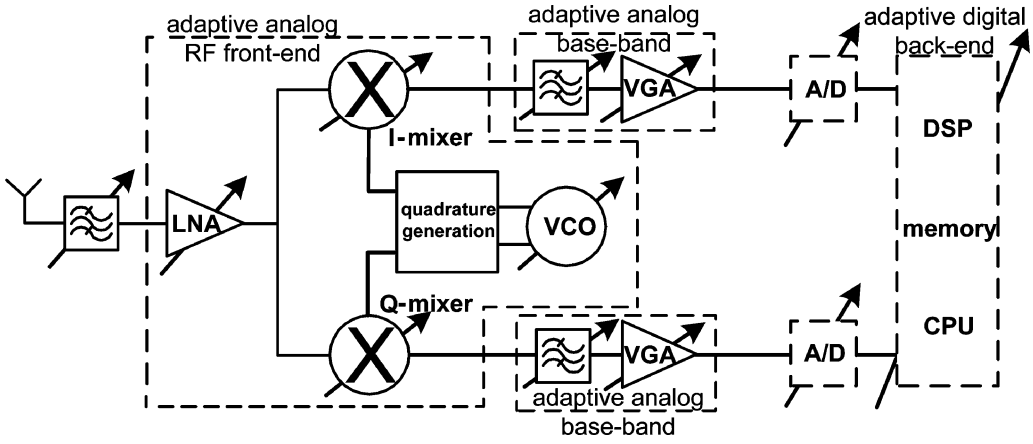

Fig. 1. Topology of an adaptive receiver.

to extend the "lifetime" (i.e., time between battery charges) of mobile devices.

Setting the performance parameters of an RF front-end by means of adaptive circuitry is a way to manage power consumption in the RF path of a receiver [1]. An adaptive low-noise amplifier (LNA), an adaptive mixer, and an adaptive voltage-controlled oscillator (VCO) allow more efficient use of scarce battery resources, thereby extending the lifetime of a mobile device. Furthermore, adaptive analog baseband and digital back-end circuits enable complete hardware adaptivity. Analog and digital baseband signal processing functions could be used to monitor quality of service (e.g., bit-error rate) and adjust the receiver parameters (e.g., tune a single or multiple bias currents) in real-time to meet the performance requirements.

B. Multimode and Adaptive RF Circuit Design

In order to provide various services from different wireless communication standards at high data rates requires not only adaptive and low-power designs, but also designs that work across multiple bands and standards [16]–[20].

When different standards do not operate simultaneously, circuit blocks of a multimode handset can be beneficially shared. By using circuits that are able to trade off power consumption for performance on the fly (i.e., adaptive multimode circuits), power can be saved.

For adaptive low-noise amplifiers and mixers, power consumption is traded off for dynamic range, whereas adaptive oscillators trade off power consumption for phase noise and oscillation frequency. The design of such an adaptive multimode RF front-end circuit is discussed in this paper.

After a signal is downconverted to the baseband, it is filtered, amplified, and digitized. In order to accommodate multiple radio standards with different bandwidths and modulation schemes, multimode low-pass filters need to compromise bandwidth, center frequency, selectivity, and group delay, for optimal dynamic range and power consumption [21]–[23]. Multimode analog-to-digital converters have to quantize signals belonging to different standards, tailoring different sample rates, dynamic range, and linearity requirements [24], [25].

The ability to share circuit functions between different standards in a receiver can offer the advantages of reduced power consumption and smaller chip area. Most importantly, there is the potential for lowering cost compared to other multstandard receiver implementations, such as multistandard receivers implemented using circuits designed for the worst case condition [26] and multistandard receivers implemented with one receiver circuit per standard [16].

System requirements for multimode circuits and design of adaptive multimode RF front-end circuits are discussed in the next sections.

III. Multimode Receiver Concept

The rationale behind the choice of a receiver architecture supporting multiple standards is detailed in this section. Multimode receiver operation is then introduced to describe the multistandard scenario.

Wireless devices may use a common receiver if the protocols of the radio standards support inter-system operability. One multistandard receiver scenario is shown in Fig. 2. Impedance matching, packaging and prefiltering requirements are relaxed and simplified by using multiple LNAs. An RF switch selects the mode of interest. If the VCO and mixer performance is adequate to cover the range of signals anticipated for each application, the quadrature downconverter enables a multistandard receiver realization with a single circuit block (MMA-QD IC in Fig. 2) [20].

We consider the application of the design for adaptivity to multimode RF front-end circuits in the framework of the requirements of the standards listed in Table I [16], [18], [27]–[34]. Situated between 1.8 GHz and 2.4 GHz, these standards may be combined in a single wireless device.

In the remainder of this paper, we will refer to the multiple modes of operation for the adaptive receiver shown in Fig. 2: with respect to noise figure, linearity, and phase-noise requirements of Table I, the receiver operating modes are classified as *demanding*, *moderate* and *relaxed*, as given in Table II.

In the context of the noise figure (*NF*) and third-order input intercept point (*IIP3*) requirements of the standards listed in Table I, the demanding mode of operation may be related to the DCS1800 and W-CDMA standards, the moderate mode to the

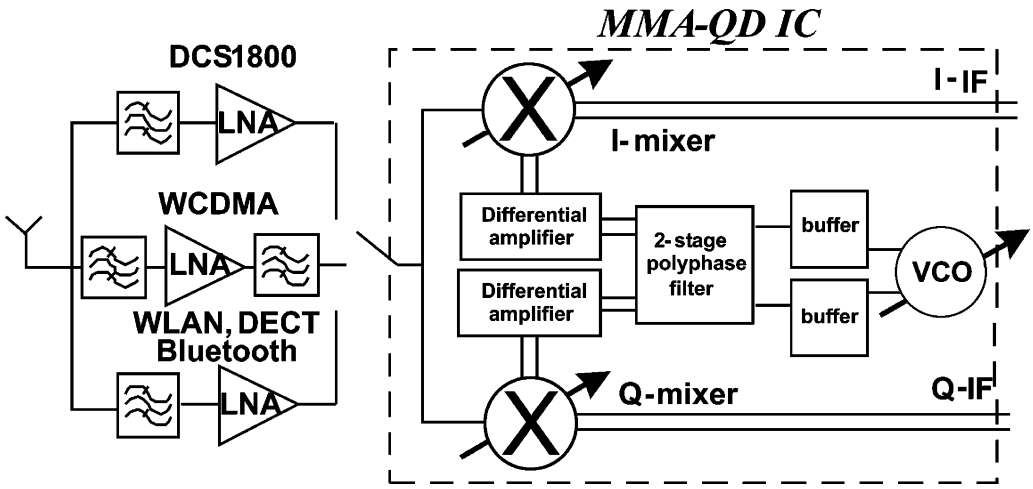

Fig. 2. Multistandard and adaptive receiver RF front-end.

TABLE I
REQUIREMENTS FOR DIFFERENT STANDARDS REFERRED TO THE INPUT OF AN LNA

	DCS1800	WCDMA	WLAN	Bluetooth	DECT
f_0 [GHz]	1.8	2.1	2.4	2.4	2.4
NF [dB]	9	6	10	23	18
*IIP*3[dBm]	-9	-9	-12	-16	-20
PN@1MHz	-123	-110	-110	-110	-100

TABLE II
RECEIVER NOISE AND LINEARITY REQUIREMENTS PER MODE OF OPERATION

specification/mode	demanding	moderate	relaxed
NF [dB]	6	10	18
*IIP*3 [dBm]	-9	-12	-16
PN@1MHz	-123dBc/Hz	-110dBc/Hz	-100dBc/Hz

IEEE 802.11b WLAN standard, and the relaxed mode to the Bluetooth and DECT standards. Table II also summarizes the phase noise (*PN*) requirements for different modes of operation: the demanding phase-noise mode is related to the DCS1800 specification, moderate to the W-CDMA and 802.11b/Bluetooth specifications, and relaxed to the DECT specification.

Referring to Table II, the adaptive oscillator has to cover a range of phase noise of around 21 dB [19]. Based on the noise figure and linearity requirements for each mode, the ranges of the *NF* and *IIP3* to be realized by the adaptive multimode receiver are calculated from Table II as 12 dB and 7 dB, respectively.

Given the bandwidth requirement, 1.8–2.4 GHz, and the noise and linearity requirements listed in Table II, a single adaptive quadrature downconverter has been realized to interface the RF and baseband sections of the multimode receiver, shown in Fig. 2. The design of the downconverter circuits suiting this multimode implementation is described in the next section.

Referring to the channel spacing of the standards considered [27]–[31], zero intermediate-frequency (IF) and low-IF receiver configurations may be supported. For example, the multimode adaptive quadrature downconverter may operate in zero-IF mode for all standards considered except the (200 kHz) narrowband DCS1800 standard where low-IF operation would be favored.

The standards considered are chosen to illustrate the feasibility of the application of the adaptivity design concept to multimode receivers. The procedure of designing for adaptivity presented in this paper can be applied to any combination of standards.

IV. DESIGN OF A MULTIMODE ADAPTIVE RF FRONT-END

Selection of the specifications for the multimode quadrature downconverter and choice of the downconverter circuits suiting adaptivity and sharing are described next in this section. The design of a quadrature signal generator and quadrature mixers is then presented.

The test circuit of the multimode quadrature downconverter consists of an adaptive VCO, oscillator buffers, a two-stage poly-phase filter to generate quadrature local oscillator signals, mixer buffer amplifiers, and two double-balanced mixers, as illustrated in Fig. 2.

A. Multimode Adaptive Quadrature Signal Generator

The VCO shown in Fig. 3 is used to implement the adaptive oscillator. As the VCO design details are described in [19], only a brief description of this multimode oscillator design is presented here.

The VCO consists of an *LC* tank (inductor L and p-n junction varactor C_V), two capacitive voltage dividers (C_A and C_B), and a cross-coupled transconductance amplifier (Q_{O1}–Q_{O2}). A resonant-degenerated tail current source is implemented with the degeneration inductor L_{RID}. This on-chip inductor is chosen to resonate with the base-emitter capacitor of Q_{CS} at twice the oscillation frequency (2_{f0}) in order to reduce the contribution of noise from the bias circuit to the phase noise of the oscillator [19], [35].

The relationships between the parameters of the oscillator are summarized in Table III. R_L and R_C model the inductors' and varactors' series losses, G_{TK} is the effective tank conductance, n is the capacitive divider ratio, $-G_{M,TK}$ the small-signal conductance seen by the LC-tank, k the small-signal loop gain, g_m

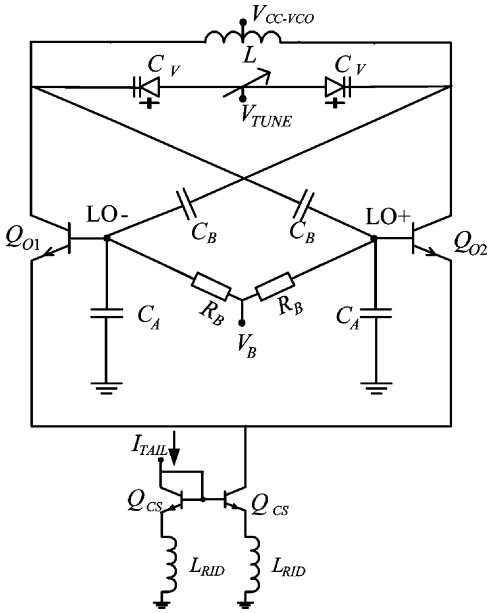

Fig. 3. Adaptive *LC* oscillator.

TABLE III
PARAMETERS OF THE ADAPTIVE *LC*-VCO

parameter	expression
G_{TK}	$\frac{R_L}{(\omega_0 L)^2} + R_C(\omega_0 C_V)^2$
n	$1 + \frac{C_A + C_\Pi}{C_B}$
$G_{M,TK}$	$\frac{g_m}{2n}$
k	$\frac{G_{M,TK}}{G_{TK}}$
g_m	$\frac{I_{TAIL}}{2V_T}$
L_{TOT}	L
C_{TOT}	$\frac{1}{2}(C_V + \frac{C_A C_B}{C_A + C_B})$
f_0	$\frac{1}{\sqrt{L_{TOT}C_{TOT}}}$

the transconductance of bipolar transistors Q_{O1} and Q_{O2}, C_Π their base-emitter capacitance, f_0 the oscillation frequency, and V_T the thermal voltage.

In this adaptive VCO, the loop gain and voltage swing across the *LC*-tank can be varied by changing current I_{TAIL}, as shown in Fig. 3. This allows adaptation of the oscillator phase noise to different operating conditions and specifications. We have named this phenomenon phase-noise tuning, and the phase-noise tuning range (*PNTR*) as its figure of merit [36].

The minimum and the maximum loop gain and tail current are estimated from the *PNTR* requirement, as described in [19]. A *PNTR* of around 20 dB can be realized from a loop gain of around 20, which is sufficient to accommodate the requirements of the multiple modes defined for this demonstration circuit in Table II. For the maximum loop gain and lowest phase noise, a voltage swing across the bases $(v_{S,B})$ of the transconductor devices of 1.2 V is estimated from

$$v_{S,B} = \frac{8}{\pi} k V_T. \tag{1}$$

Once the maximum loop gain is known, the oscillator bias point can be determined. The choice of the base bias voltage V_B is a compromise between a large output voltage swing and saturation of transconductor devices Q_{O1} and Q_{O2} [19]. To avoid the saturation of the transistors in the active part, the maximum voltage swing across the bases $v_{S,B,MAX}$ should satisfy

$$v_{S,B,MAX} \leq 2\frac{V_{CC} - V_B + V_{BE} - V_{CE,SAT}}{n+1} \tag{2}$$

where $V_{CC} = 3$ V is the supply voltage, V_{BE} is the base–emitter voltage, and $V_{CE,SAT}$ is the collector–emitter saturation voltage. For a capacitive divider ratio n of around 1.4, a base potential V_B of around 2.1 V is obtained.

These calculations indicate that more than a factor of 10 reduction in power consumption can be realized between the phase-noise demanding and phase-noise relaxed modes of the adaptive VCO under consideration.

A 3 nH tank inductor L is chosen as a compromise between low power consumption and high quality factor in the 2.1 GHz band. The inductor is fabricated using 4-μm-thick aluminum top metal in a 50 GHz SiGe bipolar technology [37]. This differentially-shielded symmetric three-turn inductor uses a ladder metal filling, has an outer diameter of 320 μm, metal width of 20 μm, and metal spacing of 5 μm [38]. The varactor consists of two base–collector diodes with 32 fingers, each 4 μm wide and 20 μm long. Metal–insulator–metal (MIM) capacitances $C_A = 150$ fF and $C_B = 600$ fF have been chosen. The degenerative inductance L_{RID} has been set to 3.4 nH using the resonant-inductive degeneration noise-reduction method [35].

Common-collector buffers interface the polyphase filter and the oscillator. They consist of 0.5×1.7 μm^2 transistors and consume 1 mA each.

Given the frequency band of the experimental downconverter implementation, 1.8–2.4 GHz, and the configurations supported, zero- and low-IF, the quadrature oscillator signals that drive the mixers are derived from a two-stage polyphase filter (PPF) (see Figs. 2 and 4). This PPF is chosen compromising between the rejection of the image signals and attenuation of the oscillation signals.

The first and second stages of the polyphase filter provide rejection at 1.75 GHz and 2.15 GHz, respectively. This allows for a higher image rejection in the 1.8 GHz band where a low-IF operation is presumed: an image-rejection ratio (*IRR*) in excess of 30 dB suffices the downconversion to a 100 kHz intermediate frequency [39]. Image-rejection requirements are relaxed around 2.1 GHz and 2.4 GHz, as a zero-IF operation is assumed

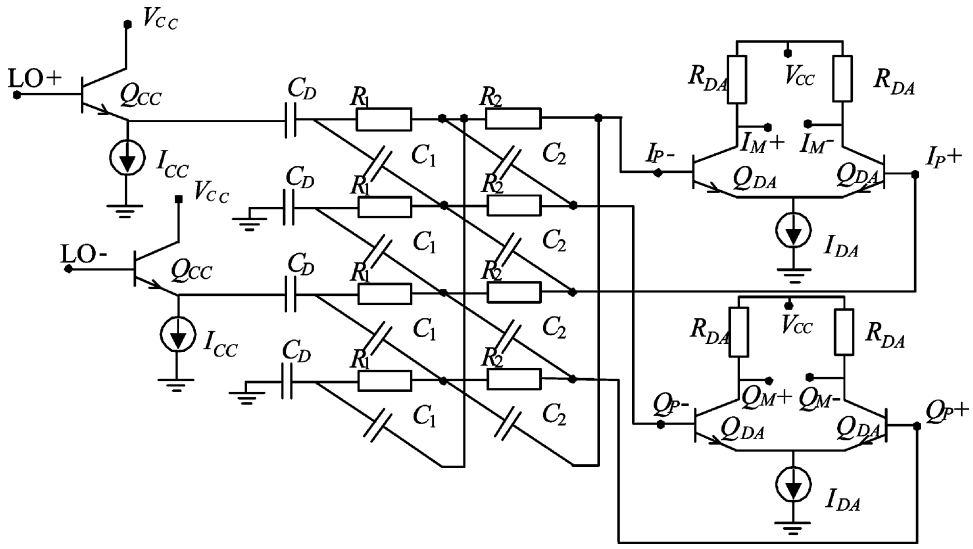

Fig. 4. Polyphase filter and buffer circuits.

in these bands: an *IRR* in excess of the signal-to-noise ratio requirement is needed [39]. Taking into account noise and distortion sources accumulated throughout a receiver, some margin has to be added to the *IRR* requirement.

The attenuation of the oscillation signal through the passive PPF necessitates a second buffer stage between the filter outputs and the mixer quads. Each buffer provides 160 mV signal swing and consumes 1.1 mA of bias current.

B. Multimode Adaptive Quadrature Downconverter

Selection of specifications for receiver circuits is a complex task, taking into account the relationships and tradeoffs between gain, noise figure, linearity, and power consumption [1]. For adaptive circuits, the performance relationships are even more difficult to describe.

In order to facilitate the selection of the specifications for the experimental adaptive quadrature downconverter, we assume each LNA has a noise figure of 2 dB, an *IIP3* of 1 dBm, and 13 dB gain. For the (quadrature) baseband circuitry (i.e., the cascade of baseband circuits, such as IF filters and amplifiers), a NF_{BB} of 14 dB and an $IIP3_{BB}$ of 9 dBm are assumed [32], [40], [41].

Given the multimode receiver requirements (see Table II) and the specifications for the LNA and baseband circuitry, the noise figure and linearity performance of the quadrature downconverter can be determined for each mode of operation using the cascaded *NF* and *IIP3* formulas [42], [43]. They are summarized in Table IV. When the quadrature downconverter *NF* and *IIP3* are adapted between 12.7 dB/−0.87 dBm and 28.8 dB/6.74 dBm, respectively, the multimode receiver satisfies the requirements listed in Table II: the demanding-mode performance is met with a 0 dB gain of the downconverter.

Note that by compromising between the performance of the LNA and baseband circuitry, a different (more relaxed or more demanding) set of the downconverter requirements results.

The second-order intermodulation (IM2) performance of the quadrature mixers determines this type of distortion for the complete receiver. As the IM2 products fall close to DC, they interfere with the desired signal in zero-IF mode of operation. However, the IM2 products from an LNA can be filtered by a tuned LNA load or AC-coupling between the LNA and mixer. Typically, a receiver with an input-referred second-order intercept point (*IIP2*) better than 45 dBm would suffice for zero-IF operation within the framework of the standards under consideration [44]. Assuming an LNA with 13 dB gain requires an *IIP2* of 58 dBm from the quadrature downconverter.

TABLE IV
REQUIRED PERFORMANCE FOR THE MULTIMODE QUADRATURE DOWNCONVERTER IN DIFFERENT MODES OF OPERATION FOR 0 dB OF GAIN

specifications/mode	demanding	moderate	relaxed
NF_{QD} [dB]	12.7	19.75	28.8
$IIP3_{QD}$ [dBm]	6.74	3.35	-0.87

The choice of the mixer circuit stems from the receiver architecture chosen and the receiver bandwidth and performance requirements. The 1.8–2.4 GHz bandwidth requires a mixer circuit with a relatively broad (and flat) frequency response to accommodate the receiver operation in the different modes.

Fig. 5 shows the schematic of the double-balanced (micro)mixer that is used to implement the quadrature downconverter [45]. It suits adaptivity and circuit sharing, and has the potential to meet the downconverter performance requirements in different modes or operation.

The mixer consists of a class-AB input stage (Q_{M1-M4}) for improved linearity, cascoded by switching quad Q_{M5-M8}. The single-ended input is converted into a differential current via common-base stage Q_{M1} and current mirror Q_{M2}, Q_{M3}. Distortion and RF input impedance matching are improved by resistors R_{M1}–R_{M4}. Transistor Q_{M4} improves symmetry in the input stage and attenuates local oscillator leakage to the RF input.

A relatively low input impedance of the micromixer facilitates the matching of the downconverter over a relatively wide range of frequencies. Only a simple input matching network is

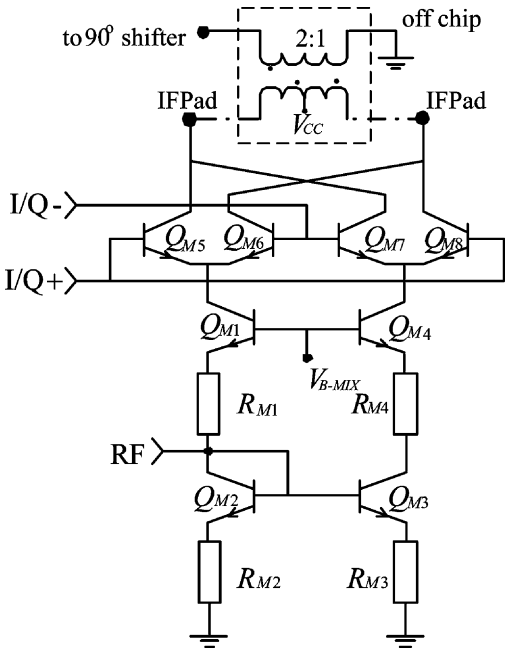

Fig. 5. Mixer with output transformer balun.

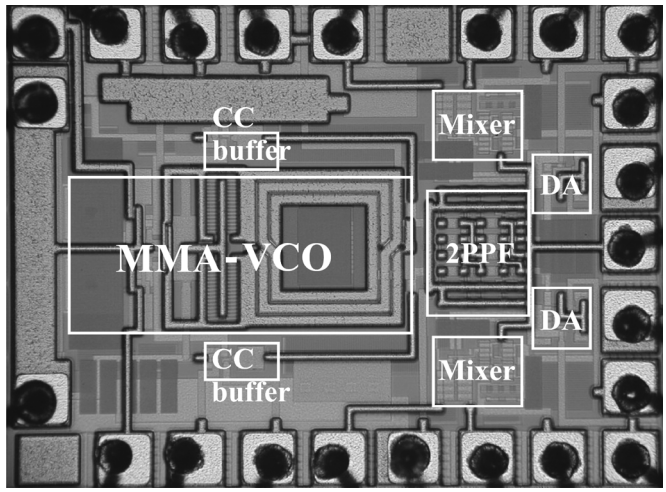

Fig. 6. Photomicrograph of the adaptive quadrature downconverter.

required when characterizing the gain, noise figure, and linearity performance of the mixer.

Linearity performance in the mixer can be traded for noise figure. By reducing the mixer bias current, the switching noise contribution is reduced. However, this tends to degrade the linearity of the switching quad. On the other hand, the emitter area of the quad transistors is a compromise between a small transistor, which allows for better linearity, and a large transistor, which generates less thermal noise in the switching quad. Faster switching of the quad (and accordingly better linearity and noise figure) can be insured to a certain level by a large amplitude of the VCO signal. Linearity and noise figure of the transconductance stage can be also traded off by adjusting the bias current and area of transistors Q_{M1-M4} [45].

The transistors and resistors are therefore sized to optimize conversion gain, noise figure, and linearity. For the mixer input stage, transistors Q_{M1-M4} have a length/width ratio of 40 μm/0.5 μm and resistors R_{M1-M4} are 21 Ω. For the switching quad, transistors Q_{M5-M8} have a length/width ratio of 8 μm/0.5 μm. The mixer performance parameters can be adaptively adjusted by changing the mixer bias current, which is set by the voltage applied to the base terminals of Q_{M1} and Q_{M4}.

Simulations show that the downconverter satisfies the demanding-mode requirements drawing 10 mA of current from a 3 V supply, and that a factor of 2 reduction in power consumption can be realized between its moderate and demanding modes of operation. Performance tradeoffs in the micromixer have been extensively studied in [45].

The performance of the voltage-driven quadrature downconverter has been characterized. However, if a complete receiver had been implemented, the mixer circuits could have been driven from a current output of an LNA, obviating the need for the resistors R_{M1}, R_{M4}. The linearity performance of the mixer would improve as expected, given the current-driven common-base input-stage of the mixer [46]. Different mixer circuit parameters could then be selected in order to meet the multiple requirements of Table II.

V. Experimental Results for the Image-Reject Downconverter

The 0.65×1.0 mm^2 testchip (excluding bondpads), shown in Fig. 6, was wirebonded into a 32-pin quad package. A custom printed-circuit board (see Fig. 7) with bias and supply line filtering was designed for testing. The differential quadrature IF signals are converted to single-ended form via external transformers with a 2:1 turn ratio. A 50 Ω quadrature hybrid combines the mixers outputs at baseband, giving an effective mixer load of 200 Ω. A block diagram of the complete test setup is shown in Fig. 8 (see Figs. 3, 4, and 5 for notation).

The performance of the complete adaptive quadrature downconverter has been characterized for the demanding mode of operation in the 2.1 GHz frequency band. The measured results for the image-reject downconverter in the demanding mode are summarized in Table V [20], after de-embedding from the test setup shown in Fig. 8.

Capacitors on the IF output signal lines (10 pF at each IF output) suppress high-frequency signals, and for the 70 MHz IF used in gain testing attenuate also some of the desired signal. The gain of the quadrature downconverter is around $+1.4$ dB. A higher gain can be achieved for a higher mixer load impedance.

The noise and linearity performance has been measured within the bandwidth of the commercial hybrid, ranging from 70 MHz to 150 MHz. The low input impedance of the downconverter facilitates a broadband response of the input network. This provides similar gain for the input RF signals over the range of frequencies assessing the linearity performance of the quadrature downconverter. For the intermodulation products falling within the bandwidth of the hybrid, second- and third-order intercept points have been determined. An *IIP3* of 5.5 dBm and an *IIP2* of 51 dBm have been measured for a bias current of 5 mA per mixer. An improvement of around 5 dB can be expected for the *IIP2* after low-frequency baseband

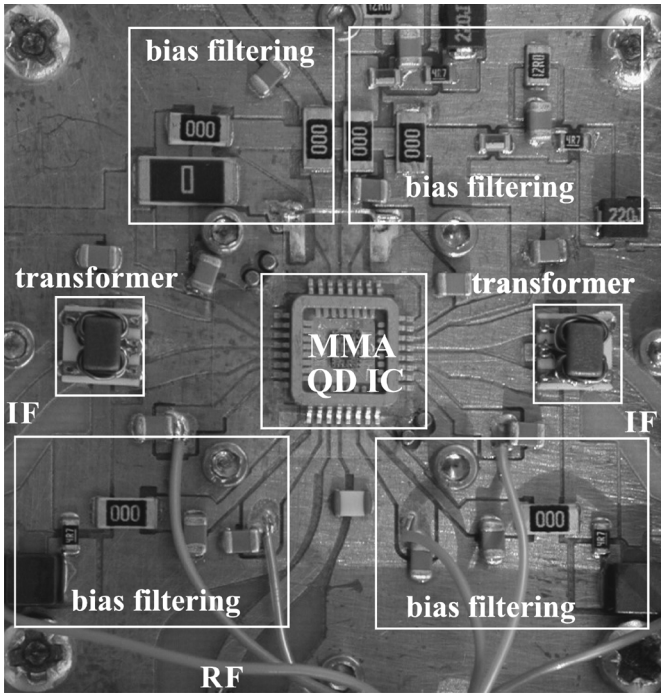

Fig. 7. Packaged multimode adaptive quadrature downconverter IC in the test fixture.

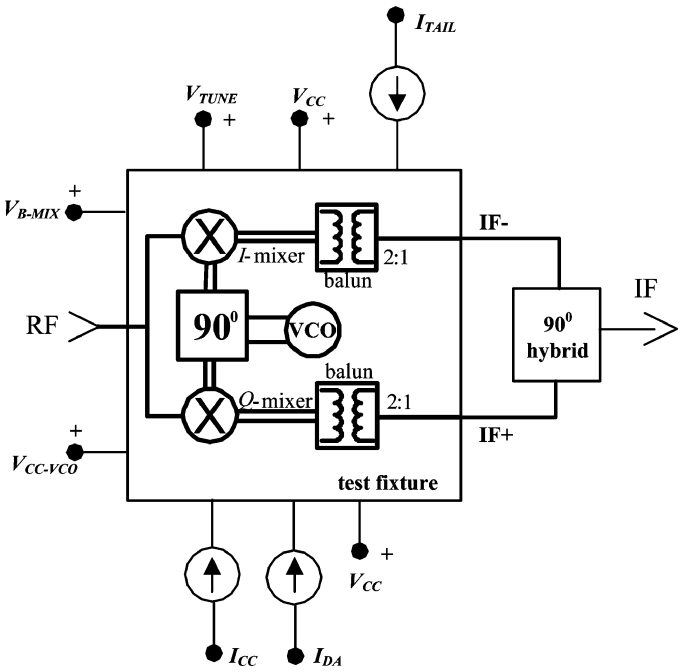

Fig. 8. Block diagram of the test setup.

filtering [32], [33]. Moreover, increasing the amplitude of the applied quadrature VCO signals (at the cost of increased power consumption of the VCO and/or differential amplifiers) improves the second-order intermodulation distortion [47]. The quadrature downconverter has a single-side band noise figure of 13.9 dB in the demanding mode while drawing 10 mA of bias current.

The measured image-rejection of 20 dB is satisfactory for the zero-IF mode of operation. For the low-IF operation, a better image-rejection would be required. Quadrature combining implemented on-chip at baseband (or in a digital back-end) and a three-stage polyphase filter implemented for oscillator quadrature signal generation are ways to improve the *IRR* in excess of 30 dB. Isolation between the oscillator port of the quadrature downconverter and the measured input RF port is approximately 45 dB.

TABLE V
MEASURED IMAGE-REJECT DOWNCONVERTER PERFORMANCE AT 2.1 GHz IN THE DEMANDING MODE

Conversion Power Gain [dB]	1.4
Noise Figure [dB]	13.9
Input Third-Order Intercept Point [dBm]	5.5
Input Second-Order Intercept Point [dBm]	51
Phase Noise at 1MHz offset [dBc/Hz]	-123
Image-Rejection Ratio [dB]	20
LO-to-RF coupling [dB]	-45
Power Consumption of Mixers [mW]	30
Power Consumption of Oscillator [mW]	18
Power Consumption of Buffers [mW]	12.6
Total Power Consumption [mW]	60.6

The oscillator performance was characterized separately from a stand-alone test circuit implemented in the same technology [19]. Operating from a 3 V supply, the adaptive VCO achieves a tuning range of 600 MHz, ranging from 1.8 GHz to 2.4 GHz, as shown in Fig. 9. In order to relax the requirement of a large frequency tuning range from a varactor, switched capacitor banks can be used [48]. They would allow for switching between standards, whereas varactors would perform fine frequency tuning within a band. The complete 2.4 GHz band could be covered using this method.

The oscillator achieves a phase noise of -123 dBc/Hz at 1 MHz offset from the carrier at 2.1 GHz for bias current of 6 mA, fulfilling the demanding-mode phase-noise requirement. This is shown in Fig. 10.

The image-reject downconverter testchip (comprising the VCO, two mixers and buffers) consumes around 20 mA in the demanding mode of operation. For the performance of the LNA and baseband circuits as given in Section IV, the multimode image-reject downconverter has the potential to meet the multimode receiver specifications in the demanding mode of operation, as summarized in Table V.

For the (less stringent) receiver requirements in the other modes of operation, the performance of the quadrature downconverter circuits may be relaxed accordingly. The multimode receiver noise and linearity performance required in the moderate and relaxed modes, as listed in Table II, may be satisfied while reducing power consumption of the oscillator and mixer circuits. Control of the circuits' bias currents for the different

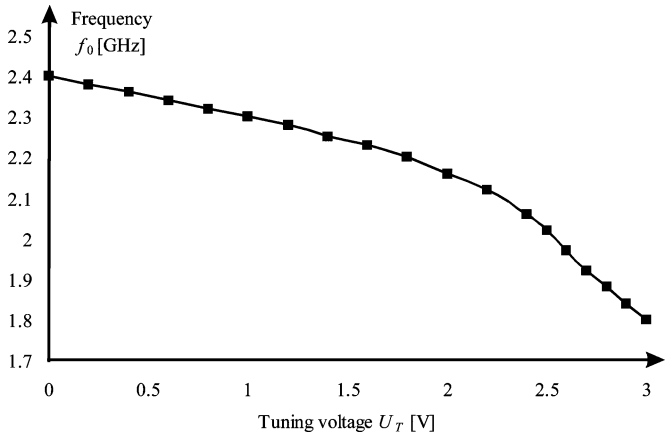

Fig. 9. Oscillator frequency-tuning curve for a 3 V tuning voltage.

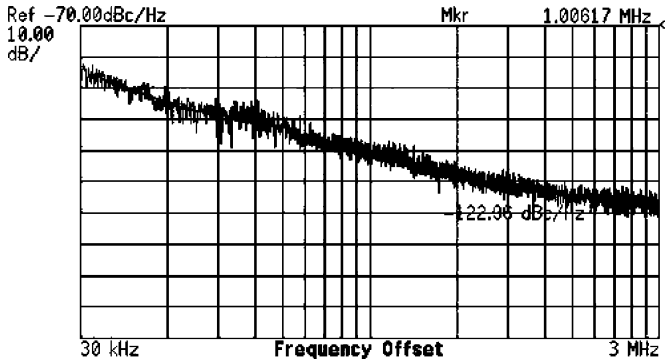

Fig. 10. Oscillator phase noise at 1 MHz offset from the 2.1 GHz carrier.

operating modes can be realized by additional baseband circuitry, for example.

By trading power consumption for phase noise, the operation of the VCO may be adapted between different modes: more than a factor of 10 reduction in current consumption suffices the phase-noise requirement in the relaxed mode of operation [19]. By adapting the bias currents of the mixers, the gain, the noise figure and the linearity of the image-reject downconverter may be varied [20], [45]: the noise and linearity performance requirements in the relaxed mode of operation, as listed in Table II, allow for more than a factor of 2 reduction in power consumption of the mixers.

The experimental multimode image-reject downconverter presented in this paper allows for a factor of 2 saving in power consumption between the demanding and relaxed modes of operation, from around 60 mW to 30 mW. Compromising between the performance of the LNA and baseband circuits, a different set of performance requirements for the quadrature downconverter would result. This may then result in different realizations of the downconverter circuits and different performance/power-consumption tradeoffs.

VI. Conclusion

In multistandard applications, sharing functional blocks between different standards using adaptive circuits offers low power consumption and small chip area, and may reduce overall cost. The exploratory multimode adaptive image-reject downconverter test design presented in this paper satisfies the requirements of the demanding second- and third-generation standards in the 1.8–2.4 GHz band at current consumption of around 20 mA. It offers more than a factor of 2 saving in power/current consumption between the demanding and relaxed applications, while still maintaining sufficient functionality.

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