A PPM Gaussian Monocycle Transmitter for Ultra-Wideband Communications

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ABSTRACT

A Gaussian pulse generator incorporating a pulse position modulator for use in an impulse radio ultra-wideband system is described. The pulse generator is preceded by a programmable pulse-position modulator and comprises of a cascade of complex first-order systems, which, in turn, are made up of differential pairs employing partial positive feedback. The resulting PPM Gaussian pulse generator is designed in IBM 0.18µm Bi-CMOS IC technology. Simulations predict the correct operation of the circuit for supply voltages of 1.8V and a power consumption of 30mW. The output monocycle indeed approximates a Gaussian monocycle; having a pulse duration of about 250ps. Proper modulation of the pulse in time is confirmed.

Keywords **-** ultra-wideband, impulse radio, complex first-order systems, pulse position modulation, analog integrated circuits, transceiver

1 INTRODUCTION

The United States Federal Communications Commission (FCC) has officially endorsed ultra-wideband (UWB) technology for commercial wireless applications. When implemented as impulse radio, this new technology may revolutionize the way we think in wireless technology by modulating data in time rather than in frequency, which promises enhanced data throughput with low-power consumption. Transmitted pulses of ultra-short duration with very low power spectral density, a wide fractional channel bandwidth and excellent immunity to interference from other radio systems, are typical characteristics of UWB systems **[1]**. The implementation of an active Gaussian pulse generator is the focus of this work. Gaussian pulses offer an excellent time-frequency resolution product **[2].** Pulse position modulation is used to encode the binary transmitted data **[3] [4]**.

The Gaussian pulse generator comprises a cascade of a fast triangular pulse generator and a Gaussian filter (i.e., a filter with a Gaussian impulse response) **[2]** and is described in the following two sections of this paper. It is central to the ultra-wideband transmitter design. The filter is implemented as a cascade of three complex first-order systems (CFOS), which, in turn, consist of gm-C sections that employ differential pairs with partial positive feedback. The CFOS is described in Section 3. When driven by the triangular pulse generator, which is presented in Section 4, the filter provides an output signal that approximates a Gaussian monocycle. The pulse is modulated in time by means of a programmable binary pulse position. The modulator is composed of a variable slope generator and a comparator (Section 4). Simulation results are presented in Section 5.

2 TRANSMITTER ARCHITECTURE

Two possible setups of the transmitter model are presented (Figure 1).

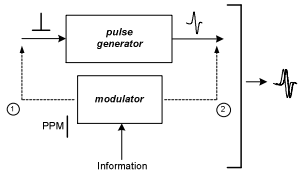

Figure 1 (1) PPM precedes the pulse generator; (2) PPM succeeds pulse generator

The pulse generator may either precede or succeed the pulse position modulation (PPM) as the delay circuit used to implement PPM can either act on the incoming binary data or on the pulses ready for transmission. It is known that delaying continuous time signals requires a higher degree of hardware complexity as compared to delaying a binary signal. Hence, the modulator will be located in front of the pulse generator.

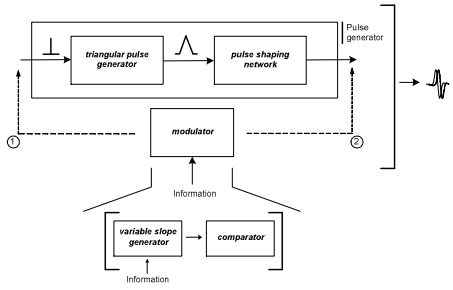

Figure 2 PPM based pulse generator.

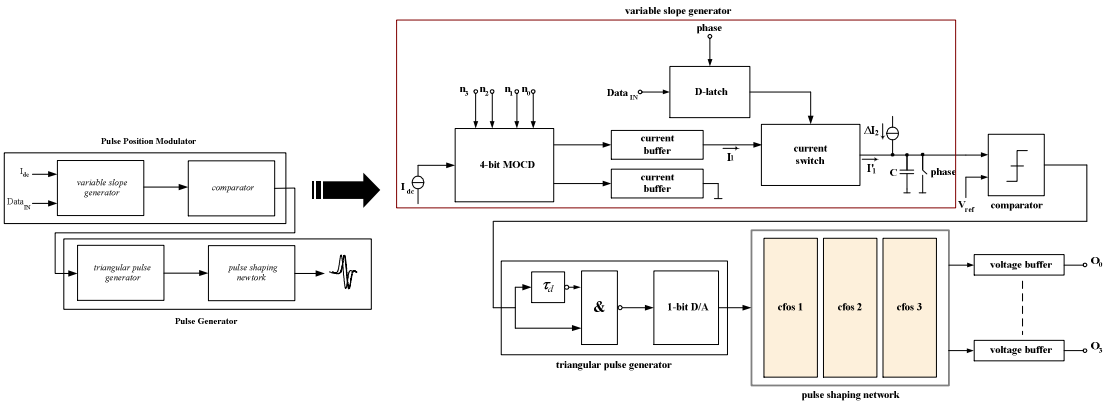

Figure 3 UWB transmitter

Figure 2 shows the triangular pulse generator as part of the overall pulse generator. The triangular pulse generator is used to avoid cross talk and to approximate an impulse-like waveform to evoke the Gaussian monocycle. The pulse shaping network or Gaussian filter is implemented by using cascaded active CFOS stages. In order to obtain pulse position modulation, a ramp is being generated, whose slope depends on the information signal (See Figure 4) **[5] [6]**. The ramp is then fed to the input of the comparator that compares the momentary value of the ramp with a fixed threshold and generates a trigger **[7]**.

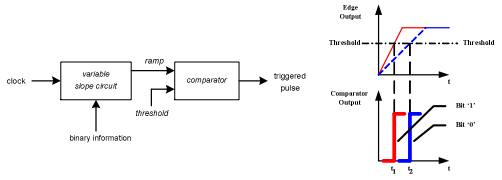

Figure 4 PPM modulator comprising a variable slope circuit and a comparator; waveforms

The PPM modulator comprises a 4-bit MOCD (MOSFET only current divider), which delivers a DC current (I_1) derived from its input code $\{n_0 \ldots n_3\}$ and I_{dc}, according to $I_1 = I_{dc} \cdot \sum_0^3 n_i \cdot 2^{(i-4)}$ (See Figure 3). The current switch conveys I_1 to I'_1 only if its input bit is "high". The D-latch synchronizes the incoming binary data with the clock phase. As a result, when the incoming binary data is high and the clock phase becomes high as well, I_1 is added to ΔI_2. Likewise, on a "low", only ΔI_2 is used as the input to capacitance C. This capacitance acts as an integrator, generating a ramp signal voltage. The slope of the ramp depends on the total current (I_1+ΔI_2 or ΔI_2) through the capacitance, according to the well known constitutive relation:

$$u_C(t) = \frac{1}{C}\int_0^t (ic)d\tau + u_C(t)\big|_{t=0}$$

The output voltage of the capacitance, u_C, in turn is fed to the comparator that compares the momentary value of the ramp with a fixed threshold and generates an edge. This edge is then used to drive the "triangular pulse generator", which consecutively performs the task of generating an impulse-like function to evoke the impulse response of the succeeding pulse shaping network, being a Gaussian filter.

3 CFOS REALIZATION

The key to the Gaussian filter is a cascade of complex first order systems. A complex first-order system (CFOS) is basically an extension of an ordinary first-order filter to complex variables. Its structure exhibits similar characteristics as an ordinary second order system. Two real equations are used to express the behavior of a CFOS instead of one complex equation **[2]**.

$$\frac{d}{dt}x(t) = (\sigma + j\omega)x(t) + (cr + jci)u(t) \quad x(t) = xr(t) + xi(t) \tag{1}$$

where u is a real input signal, x is a complex state variable, xr and xi being its real and imaginary part, respectively. σ, ω, cr, ci are system parameters, for which it holds that $\sigma \leq 0$, $\omega > 0$, and ci and cr are real numbers. The CFOS impulse response equals:

$$h(t) = (cr + jci)e^{(\sigma_0 + \omega_0 j)t}U^{-1}(t) \tag{2}$$

The output voltage xr can be designed using an integrator, whose input current is the sum of u/Rr, $-xi/R\omega$, and $-xr/R\sigma$, according to:

$$xr = \int\left(\frac{-xr}{R\sigma C} + \frac{-xi}{R\omega C} + \frac{ur}{RrC}\right)dt \tag{3}$$

Likewise, the output voltage xi too can be written as:

$$xi = \int\left(\frac{-xi}{R\omega C} + \frac{xr}{R\sigma C} + \frac{ur}{RiC}\right)dt \tag{4}$$

Subsequently, one expresses the real (xr) and imaginary outputs (xi) as follows:

$$xr = \frac{-R\sigma}{1 + R\sigma C}\left(\frac{ur}{Rr} + \frac{xi}{R\omega}\right) \tag{5}$$

$$xi = \frac{R\sigma}{1 + R\sigma C}\left(\frac{xr}{R\omega}\right) \tag{6}$$

From (5) and (6) one easily calculates the transfer function of the CFOS cell for the real and imaginary outputs, which are given as follows.

$$\frac{xr}{ur} = \frac{-R_\sigma R_\omega^2 (1 + R_\sigma C s)}{R_r(R_\omega^2 + R_\sigma^2)(\frac{R_\omega^2 R_\sigma^2 C^2}{R_\omega^2 + R_\sigma^2} s^2 + 2\frac{R_\omega^2 R_\sigma C}{R_\omega^2 + R_\sigma^2} s + 1)} \tag{7}$$

$$\frac{xi}{ur} = \frac{-R_\sigma R_\omega^2}{R_r(R_\omega^2 + R_\sigma^2)(\frac{R_\omega^2 R_\sigma^2 C^2}{R_\omega^2 + R_\sigma^2} s^2 + 2\frac{R_\omega^2 R_\sigma C}{R_\omega^2 + R_\sigma^2} s + 1)} \tag{8}$$

As illustrated by (7) and (8), the complex first-order system does show similar characteristics of that of a second order system and this confirms the statement made earlier. One also establishes the expressions for σ, ω and *cr*, which are, respectively:

$$\sigma = \frac{1}{R_\sigma C} \quad ; \quad \omega = \frac{1}{R_\omega C} \quad ; \quad c_r = \frac{1}{R_r C} \tag{9}$$

Now, going back to (2), one may validate the results obtained for σ, ω and *cr*. Considering the Laplace transform of the two functions, shown in (10) and (11), it is unambiguous that the impulse response of the real output is equal to $c_r e^{-\sigma t}\cos(\omega t)$ and similarly, the impulse response of the imaginary output is equal to $c_r e^{-\sigma t}\sin(\omega t)$.

$$L[c_r e^{-\sigma t}\cos(\omega t)] = \frac{-c_r\sigma}{\omega^2 + \sigma^2}\frac{1 + \frac{s}{\sigma}}{\frac{s^2}{\omega^2 + \sigma^2} + 2\frac{\sigma}{\omega^2 + \sigma^2}s + 1} \tag{10}$$

$$L[c_r e^{-\sigma t}\sin(\omega t)] = -\frac{c_r\omega}{\omega^2 + \sigma^2}\frac{1}{\frac{s^2}{\omega^2 + \sigma^2} + 2\frac{\sigma}{\omega^2 + \sigma^2}s + 1} \tag{11}$$

From (2), the impulse response of a cascaded (n+1) CFOS system (as depicted in Figure 5) is given by:

$$h_{n+1}(t) = A(c_r + jc_i)^{n+1}\frac{t^n}{n!}e^{(\sigma + j\omega)t}U(t) \tag{12}$$

As one can infer from the term t^n/n, the more the stages in cascade, the better the approximation to the Gaussian envelope.

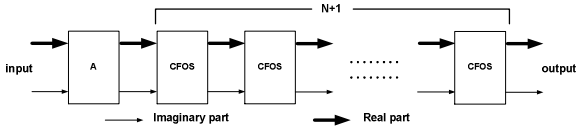

Figure 5 Cascaded CFOS

4 CIRCUIT DESIGN

4.1 PULSE GENERATOR

4.1.1 gm-C cell CFOS

To satisfy (5) and (6) and for high frequency applications, one uses small and fast transition blocks such as transconductance-capacitance (gm-C) cells (Figure 6) **[8]**.

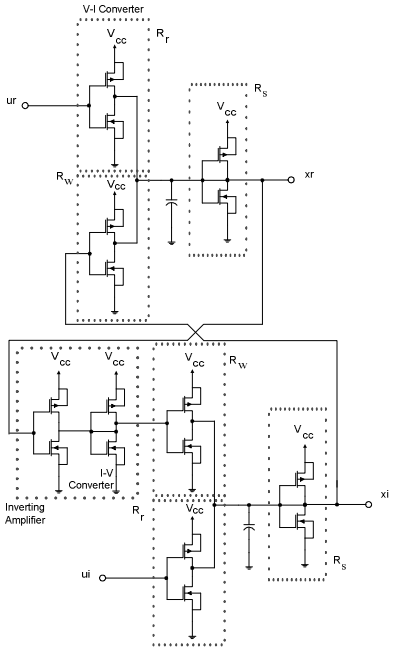

Figure 6 gm-C single stage CFOS

However, due to the four cascaded transconductance stages in the feedback ring, the response time of the CFOS stage becomes too large. Moreover, from simulations it follows that ten stages need to be cascaded to achieve a reasonable approximation to the Gaussian envelope. As a result, the power consumption becomes too large. To solve this, a differential transconductance structure is used to get rid of the required inverters and thus enhance the response time of the CFOS.

4.1.2 Pulse shaping network

The differential pair arrangement in Figure 7 with partial positive feedback (PPF) also satisfies equations (7) and (8) [9].

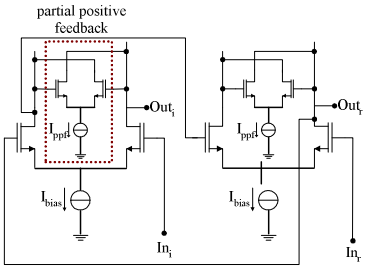

Figure 7 CFOS employing two differential pairs with gain enhancement by partial positive feedback

The inclusion of the PPF stage as active load enhancement not only increases the DC gain but also the unity gain frequency. The significant increase in the gain and the bandwidth is contributed to the increase in the effective transconductance of the stage. If L is the loop gain, then the gain of the amplifier is enhanced by a factor of $1/(1- L)$. When L tends to 1, the gain tends to infinity. If L is made too large or too small, it will either make the system unstable or have little to no effect on the performance of the amplifier at all. Thus, L should be bounded by the following equation.

$$0< L <1 \qquad (12)$$

A significant improvement in the response time is seen due to the PPF loop. One could even use PMOS pull-ups as a positive feedback load to save power.

4.1.3 Triangular pulse generator

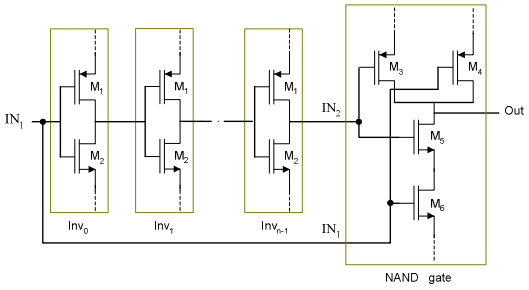

Figure 8 Triangular pulse generator

The triangular pulse generator is made up of a cascade of inverter stages, followed by an *NAND* gate function (Figure 8). The key purpose of this block is to generate an impulse-like function that is able to evoke the impulse response of the succeeding pulse shaping network. The input pulse (IN_1) and its delayed self (IN_2) act as the two inputs to the *NAND* gate. Only when both inputs for a *NAND* gate are "high", its output is low. Hence, an impulse like waveform is generated, with its pulse width approximately being equal to the propagation delay of a single inverter times the total number of inverters (See Figure 9).

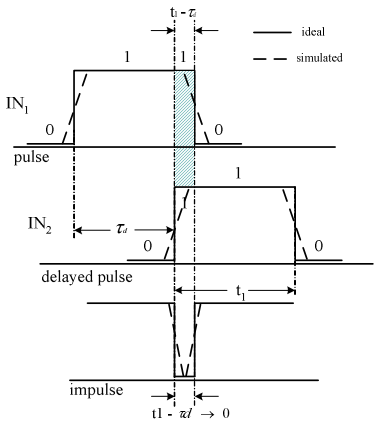

Figure 9 Triangular pulse generator input and output waveforms

4.2 MODULATOR

4.2.1 Variable slope generator and comparator

4-bit MOCD - The schematic of the MOCD together with its current buffers is shown in Figure 10. The output currents of the MOCD are digitally programmable fractions of the applied input current I_{dc}, **[10]**. To ensure correct operation, both outputs (13) have to be held at the same potential or $V_A \approx V_B$

$$mocd = I'_1 = \sum_0^i I_{Oi} \quad \& \quad dumped = I_{dc} - I'_1 = \sum_0^i I_{O'i} \qquad (13)$$

This necessitates the need for two current buffers, which compose of current sources (M_0, M_3, M_6, and M_9) delivering a reference current of I_{dc} and a cascode current mirror configuration (M_1, M_2 and M_4, M_5). M_8 mirrors the current ($I_{dc}+I'_1$) and in conjunction with the output of the D-latch, the output current I'_1 is subsequently delivered to the current switch).

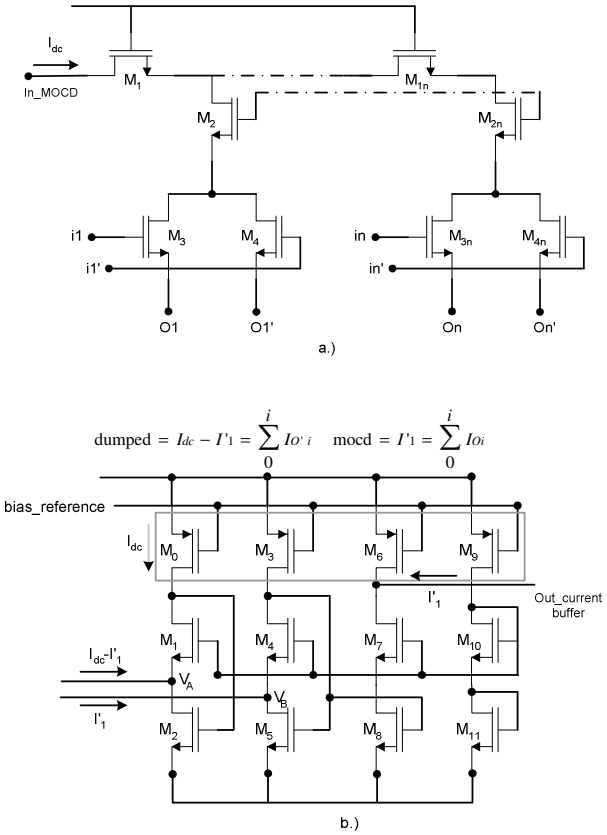

Figure 10 a) 4-bit MOCD b) current buffers

The D-latch - The binary data (the information) is fed to the input of the D-latch and is acquired by the latch as soon as the clock/phase goes high. Its circuit diagram is shown in Figure 11.

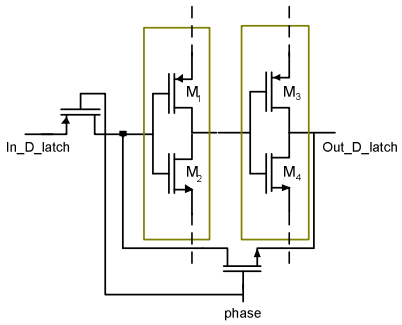

Figure 11 D-latch

Current switch, variable slope circuit and comparator - The key ingredients which make up the current switch seen in Figure 12 a) are the current mirrors formed by transistors M_1, M_2 (mirror current I'_1 from current buffer) and the current switch M_3. The entire variable slope circuit behaves as an intermediate between the preceding current buffers and the following comparator. To briefly recapitulate, as soon as the incoming binary data is high and the clock phase also becomes high, I_1 is added to ΔI_2. Likewise, on a "low", only ΔI_2 is used as the input to capacitance C to generate a ramp. This resulting ramp serves as the input to the comparator (See Figure 12 b)), which makes a comparison of the momentary value of the ramp with a fixed threshold to generate an edge. Henceforth this edge is used to drive the "triangular pulse generator" of the Gaussian pulse generator.

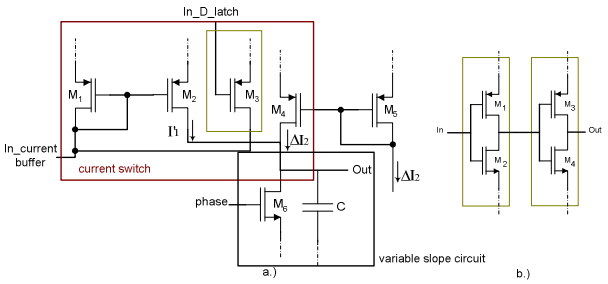

Figure 12 a) current switch, variable slope circuit b) comparator

5 SIMULATION RESULTS

All circuit simulations were carried out using IBM 0.18µm Bi-CMOS IC technology. The target of achieving 200ps Gaussian pulses was not feasible because of the significant contribution of parasitic capacitances. The smallest possible pulse width attained was 230ps before layout extraction and roughly 250ps after layout extraction with amplitude of 0.2Vp-p. The power consumption was approximately equal to 30mW at a power supply of 1.8V. Picoseconds and nanoseconds delays can be obtained by using this programmable delay circuit (Figure 13).

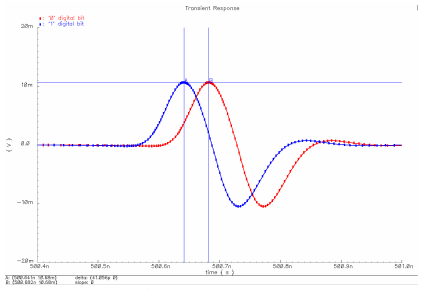

Figure 13 PPM of 1st derivative of Gaussian monocycle

6 CONCLUSIONS

A fully programmable on-chip Gaussian pulse generator incorporating a pulse position modulator for use in an impulse radio ultra-wideband system has been presented. Proper modulation of the information as well as an excellent approximation of the Gaussian monocycle has been achieved. Design is currently being fabricated in IBM 0.18µm Bi-CMOS technology. A minimum pulse width of about 250ps is attainable.

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