4.10 A 34dB SNDR Instantaneously-Companding Baseband SC Filter for 802.11a/g WLAN Receivers

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In wireless receivers, large dynamic range (DR) input signals necessitate additional power consumption in baseband active filters. A 5th order Chebychev, ladder type, companding SC low-pass filter is described in this paper which provides gain switching based on the instantaneous value of the signal to handle peak-to-average-power ratio (PAPR), thereby reducing power dissipation for a given DR. Companding compresses the high DR input signal, processes it in a lower DR system (the filter in our case) and then expands the signal at the output [1]. Companding is an alternative to AGC, which sets the filter internal gains during the preamble/midamble so that the signal level in the filter is optimal to provide the minimum SNDR required by the specifications. The IEEE 802.11a/g WLAN receiver [2] presents 2 limitations to the use of AGC. First, the standard puts a stringent AGC settling time requirement (<5.6µs). Since the filter needs extra settling time, AGC is implemented after the filter and before the ADC in the receiver baseband. Secondly, the high PAPR of OFDM signals requires headroom of at least 12dB in the DR of the filter. While dynamic impedance and gain scaling techniques have been proposed in the past as an alternative to AGC [3], this work addresses the PAPR problem.

Figure 4.10.1 shows an example of a companding SC discrete integrator [4]. The two non-overlapping clock phases are Φ1 (sampling/hold phase) and Φ2 (integration phase). S_{i1}, S_{i2}, S_{o1}, S_{o2}, Inc and Dec are digital signals. Based on the OTA's output at the end of Φ2, S_{i1} and S_{i2} change the input sampling capacitance C_{s1} to switch the integrator gain by a factor of 2 in the next Φ2 (compression). S_{o1} and S_{o2} change the output sampling capacitance C_{s2} to provide an inverse gain for the subsequent stage (expansion). The charge (memory) on the integration capacitance C_I is then updated. When the gain is decreased by 2 (when Dec becomes high), one half of C_I is disconnected and discharged to ground during Φ1 without affecting the output. When it is reconnected to the other half of C_I during Φ2, it halves the output voltage. Another capacitor (C_{Inc}) of same value as C_I is charged to the output voltage during Φ1. When the gain is increased by 2 (when Inc becomes high), C_{Inc} is discharged to the input of the OTA during Φ2, thereby doubling the output voltage. These compression, expansion and memory update operations are synchronized in discrete time. To reduce complexity, the expansion at the output of each stage is combined with the compression at the input of the following stage resulting in an equivalent gain for the following stage. For each stage, the companding algorithm works on a finite-state machine (FSM) run by a controller consisting of comparators and digital circuits.

Since a companding filter is a nonlinear system internally, its performance is affected by any spurious signals arising from within the system. In our case, the OTA's DC offset gives rise to even-order distortion since the DC offset has the same sign in both positive and negative half cycles of the input signal. In a SC ladder type filter, each OTA's output is sampled in both clock phases for both feedforward and feedback paths. Thus, the DC offset of the OTAs should be eliminated in both phases. We use a continuous-time auto-zeroed (AZ) OTA using feedforward [5], which results in a residual offset of 500µV under worst case process and mismatch conditions. Correlated double sampling [5] is also used to make the integration phase offset-free. Using both techniques, a worst case THD of -50dB is achieved from simulations. The AZ OTA consumes 40µW from 1.2V compared to 6mW consumed by the main OTA.

For an 802.11a WLAN receiver, Fig. 4.10.2 shows how signal levels vary throughout the receiver chain for a range of desired signal strength and worst case adjacent (Int. 1) and alternate-adjacent (Int. 2) interferers. The first stage of the filter has a gain of 12, 6 or 0dB and the expansion amplifier stage (Exp) after the filter has a gain of -12, -6 or 0dB respectively. Thus, the companding FSM has 3 states corresponding to 3 gain settings. The differential filter is implemented in 0.13µm CMOS using 2-stage Miller compensated, Class-A type OTAs with a DC loop gain of 60dB, GBW of 300MHz and a slew rate of 300V/µs. The OTAs can be further optimized to reduce power. The filter cut-off frequency is 10.5MHz. The 100MHz clock frequency ensures that companding is almost instantaneous for the input signals. A first order filter is needed for anti-aliasing. Separate analog and digital 1.2V supplies are used. A digital 1.5V supply is used for extra clock buffers that drive low-V_t CMOS switches.

Figure 4.10.3 shows the plots of signal-to-distortion ratio (SDR) vs. the desired input signal power in dBm for a single-tone test (at 2MHz) in the presence of interferers and a 2-tone test (at 4.6MHz and 5MHz). The interferers at various stages of the filter are low enough not to trigger companding when the desired signal is weak (see Fig. 4.10.2). Signal-to even-order distortion ratio (SDR_2) for the 2-tone test shows similar behavior to the single-tone test and is not plotted separately. Companding starts at -10dBm sinusoidal input signal level (required at 1dBm) to allow headroom for jumps in the OTA's output voltage at high input frequencies before a decision to compress the signal is made by the FSM. For OFDM signals, the companding can be switched on when the EVM degrades beyond an acceptable value. Figure 4.10.4 shows the output frequency spectrum for the 2-tone test when the input power is –7dBm. The higher order distortion components are below -65dB and do not affect the total SNDR. Figure 4.10.5 shows the output of the filter before and after expansion for a 2MHz tone and at –4.4dBm. The measured EVM_{rms} in the companding case is less than 3.8% for a 64-QAM OFDM signal [2]. The long OFDM training symbols are used for channel equalization. Figure 4.10.6 summarizes the measured results. It is estimated that companding by a factor of 4 should result in a power savings of 4 times compared to a non-companding filter for a given DR [4]. However, the control circuitry, comparators and the expansion stage consume 10mW, which reduces the power savings to 3.3 times. By performing expansion in the digital domain (multiplication by 2 or 4), the power savings can come close to 4 in addition to reducing the DR required from the ADC by 12dB [4]. Other ADC specifications are not affected since the filter output is in discrete time domain and digital information about the expansion is available from the FSM of the last filter stage. Figure 4.10.7 shows the die photograph. The active chip area (not optimized) is limited by capacitance (≈60pF), which is 2/3 times of that needed by a non-companding SC filter designed for 79dB DR and a signal swing of $1.4V_{pp\text{-}diff}$ [6].

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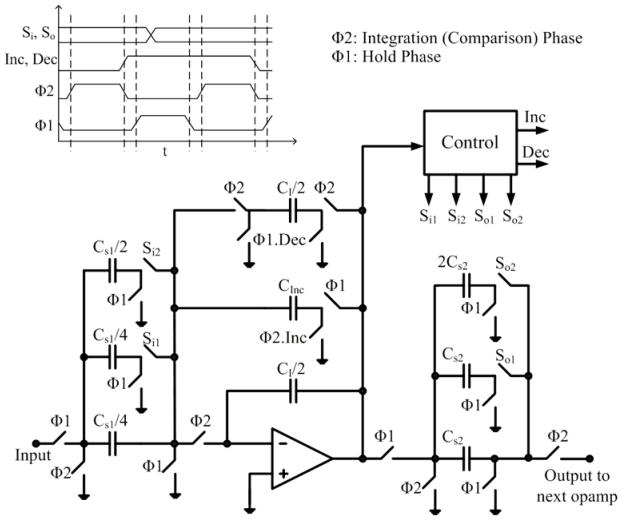

Figure 4.10.1: Companding SC discrete integrator with timing diagram for the control signals.

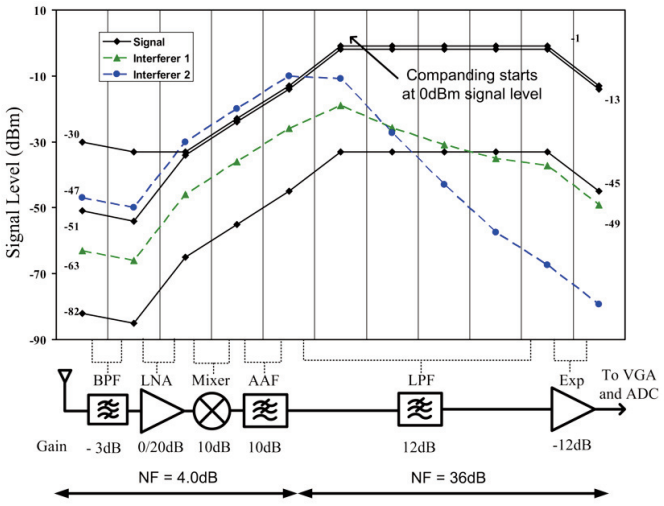

Figure 4.10.2: 802.11a WLAN receiver gain distribution for 6 Mb/s rate and 3 input signal levels at -82dBm, -51dBm and -30dBm.

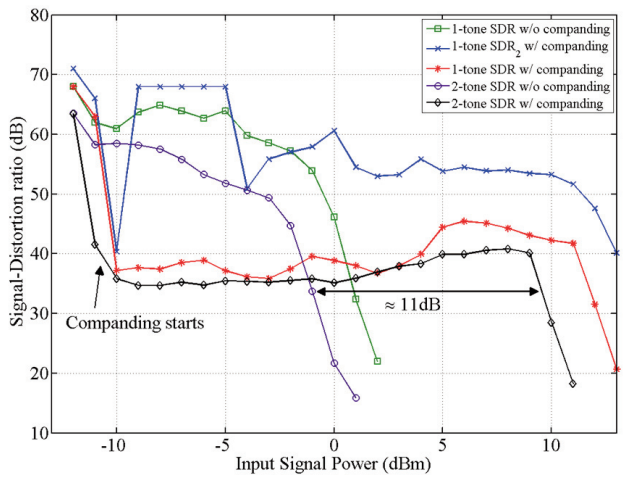

Figure 4.10.3: Signal-to-distortion ratio for single-tone (2MHz) and 2-tone (4.6MHz and 5MHz) tests vs. input signal power in dBm.

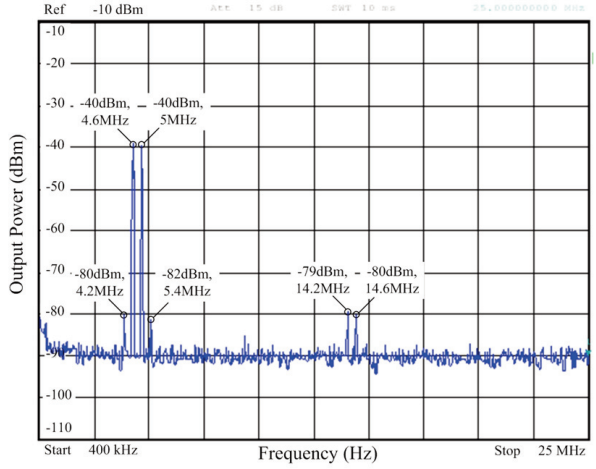

Figure 4.10.4: Output frequency spectrum for a 2-tone test (4.6MHz and 5MHz) at an input signal power of -7dBm.

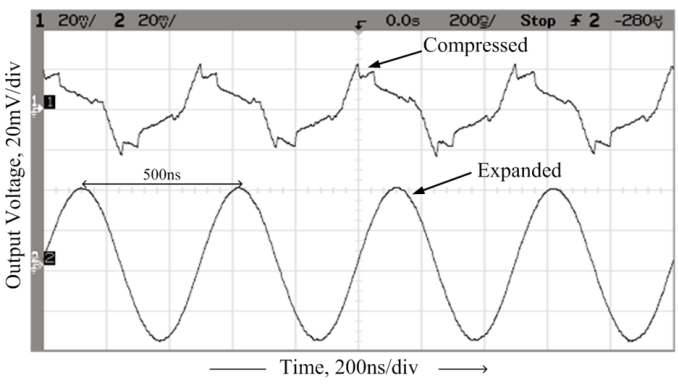

Figure 4.10.5: Single-tone test (2MHz) output voltage waveforms before and after expansion at an input signal power of -4.4dBm.

Order and type	5th order, 0.1dB in-band ripple, Chebyschev ladder type LPF, companding by factor 4, f_{-3dB} = 10.5MHz, f_s = 100MHz
Technology	IBM 0.13µm 1P8M CMOS
Supply voltages	1.2V, 0.6V (Common mode reference), 1.5V (Clock buffers) & 2.5V (I/O buffers)
SNDR	> 34dB
Input referred noise (IRN)	$29nV_{rms}/\sqrt{Hz}$ ($97\mu V_{rms}$)
Dynamic Range (DR)	79dB
EVM_{rms} (64-QAM)	< 3.8%
Power consumption	48mW (analog), 4.5mW (digital), total power = 53mW
Chip active area (excl. clock generation, I/O buffers, ESD & supply bypassing)	≈ 2.2mm²

Figure 4.10.6: Performance summary.

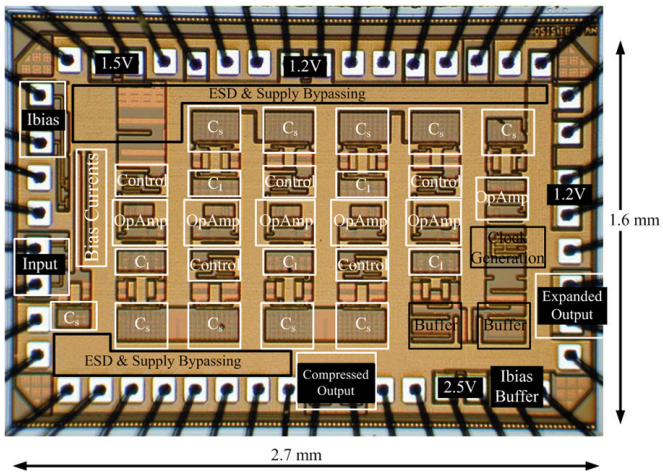

Figure 4.10.7: Die photograph.

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