Stochastic Resonance Mixed-Signal Processing: Analog-to-Digital Conversion and Signal Processing Employing Noise

Insani Abdi Bangsa[*,‡,§,†], Dieuwert P. N. Mul[*,§], and Wouter A. Serdijn[*]
iabdi.bangsa@ft.unsika.ac.id, dpnmul@gmail.com, and w.a.serdijn@tudelft.nl
[*]Bioelectronics Section, Department of Microelectronics
Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology, the Netherlands
[‡]Faculty of Engineering, State University of Singaperbangsa Karawang, Indonesia

***Abstract*—Stochastic resonance (SR) is a phenomenon in which noise can be employed to increase the performance of a system. It can e.g. be used to improve the performance of comparator-based circuits. This paper presents the analytical derivation of input-output relation, harmonic distortion, and noise behaviour of a 1-bit ADC using SR. Furthermore, the design of a new signal multiplier based on SR-ADCs is presented. The predicted behaviours are demonstrated by means of simulations. The work presented in this paper shows the potential for analog to digital conversion and integrated signal processing fully based on stochastic resonance.**

***Index Terms*—stochastic resonance, analog-to-digital converter, multiplier, 1-bit processing.**

I. Introduction

Noise has been mostly considered as something undesirable in the world of signal processing. When mixed with a signal, it is thought to obstruct the extraction of information contained in the signal. However, the occurrence of a phenomenon called stochastic resonance shows that the presence of noise can improve the performance of a system.

Stochastic resonance (SR) is a phenomenon in which the performance of a nonlinear system is better than it is without noise [1]. By adding noise to, e.g., a comparator-based circuit, a system based on SR can be built [2], [3]. The addition of noise will increase the frequency of changes of the output states, which, when averaged, will lead to an input-output relation that is more linear than that of a noiseless system. An SR system has a performance peak for a specific noise level.

This paper focuses on using SR to design a 1-bit analog-to-digital converter (ADC) and to integrate mathematical operations with the ADC. First, the SR-ADC (Fig. 1) is introduced in Section II and analytic derivations of the behaviour of the proposed system are presented in Section III. This derivation allows designers to predict the performance of the SR-ADC, and thereby enables them to determine the optimal values of the design parameters. Furthermore, 1-bit stochastic resonance signal processing operators are discussed and the design of a SR-multiplier is presented in Section IV. Finally, the conclusions are presented in Section V.

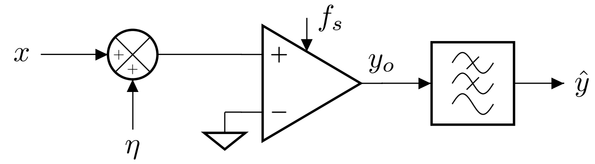

Fig. 1. Stochastic resonance system.

II. Stochastic Resonance System

A stochastic resonance system has a non-zero optimal noise value. To achieve this property, the system needs to be nonlinear, and should have two (or more) stable states [4]. In sub-threshold SR, the signal without noise cannot reach the threshold to switch from one state to another [1]. In this case, the noise is necessary to reconstruct any information from the signal. A second class of SR systems is supra-threshold SR. The signal without noise can reach the threshold to switch from one stable state to another. However, adding noise can cause the system to switch from one state to another more often, which increases the performance [5], [6]. For higher noise levels, the system behaves (close to) linearly.

Fig. 1 shows the proposed system, where x, η, y_o, and $\hat{y}$ are the input signal, input noise, 1-bit output, and averaged output, respectively. The output of the quantiser is a pulse density modulated (PDM) signal. By averaging the PDM signal using a low-pass filter, the output is transferred back to the amplitude domain. The quantiser amplifies the signal, since it can be driven by a weak noisy input signal. Besides performing the amplification, the signal is directly transformed to the binary domain, and can thus be defined as a stochastic resonance analog-to-digital converter (SR-ADC). The mechanism employed in this system shows large similarities to dithering [3], [7].

[§]I. A. Bangsa and D. P. N. Mul contributed equally to this work.

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III. Analytical Derivation

The behaviour of stochastic resonance systems can be found in literature [3], [7]. However, although a similar idea has been mentioned in [8], to the knowledge of the authors, an analytical derivation targeting a designers guide for a SR-ADC is not reported on yet. This section presents a method to predict the performance of the considered SR-ADC. To validate the method, an example is given using white Gaussian noise and a sine wave input. However, the method can be used for any input signal, and any type of white noise.

A. Input-Output Relation

The output of the quantiser is a stochastic signal. By averaging this signal, the average of multiple samples is calculated. As a result of the averaging, the expected transfer is defined by the probability of each of the two states, either Q_+ or Q_-. The expected output $\hat{y}$ is described by (1), where x is the input signal value, η is the noise value. The quantiser outputs are normalized to $Q_+ = 1$ and $Q_- = -1$.

$$\begin{aligned}\hat{y}(x,\eta) &= \mathbf{E}[y\,|\,x] \\ &= P\big((x+\eta) > 0\,|\,x\big) - P\big((x+\eta) < 0\,|\,x\big) \\ &= P(\eta > -x\,|\,x) - P(\eta < -x\,|\,x) \\ &= 1 - 2\cdot P(\eta < -x\,|\,x)\end{aligned} \tag{1}$$

The probability $P(\eta < -x\,|\,x)$, and thus the expected transfer, can be calculated using the cumulative distribution function of the noise. The noise is assumed to be white Gaussian noise, which gives:

$$\begin{aligned}P(\eta < -x\,|\,x) &= \int_{-\infty}^{-x} \frac{1}{\sigma\sqrt{2\pi}} \cdot \exp\left(\frac{-\eta^2}{2\sigma^2}\right) \mathrm{d}\eta \\ &= \frac{1}{2} + \frac{1}{2}\mathrm{erf}\left(\frac{-x}{\sqrt{2}\sigma}\right).\end{aligned} \tag{2}$$

Thus the expected output for a given input value x is

$$\hat{y}(x,\sigma) = \mathrm{erf}\left(\frac{x}{\sqrt{2}\sigma}\right). \tag{3}$$

The expected transfer of the system for different noise levels is shown in Fig. 2. The expected output is compared with simulations of the system. Averaging is performed over $10,000$ samples.

B. Gain and Harmonic Distortion

The performance of the SR-ADC is a trade-off between noise and harmonic distortion. Thus, an accurate quantisation of the harmonic distortion is crucial in the performance analysis. The total harmonic distortion (THD) is derived in the time domain. The expected output $\hat{y}(x,\sigma,t)$ is split into a linear component $\hat{H}(x,\sigma)\cdot x(t)$ and harmonic distortion $HD(t)$, which leads to

$$\hat{y}(x,\sigma,t) = \hat{H}(x,\sigma)\cdot x(t) + HD(t). \tag{4}$$

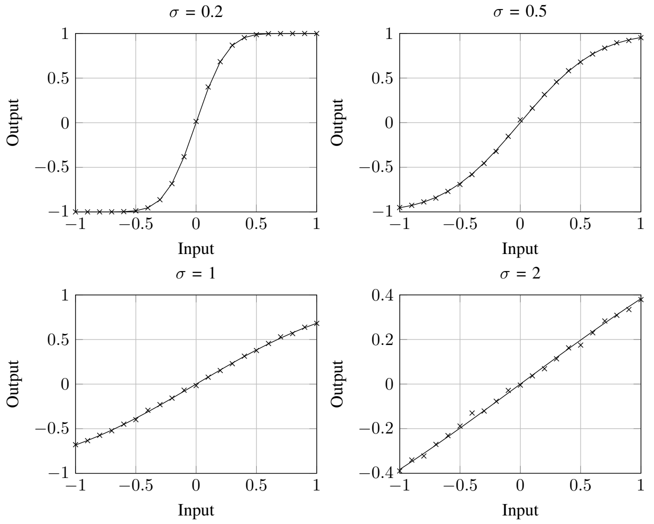

Fig. 2. Expected transfer for different noise levels. The simulation results are marked with 'x'.

The linear gain $\hat{H}(x,\sigma)$ is derived by performing a least square error fit. The gain $\hat{H}(x,\sigma)$ is scaled such that it produces the least mean squared error, and thus the power of the harmonic distortion is minimized. Since the fitted signal only affects the fundamental frequency, minimizing the error power ensures that the error only contains harmonics.

C. Noise

The noise power at the output of the quantiser can be calculated directly from the expected output ($\hat{y}(x,\sigma,t)$). Since the output of the quantiser is either 1 or -1, the power at the output of the quantiser is 1. The noise power is thus at

$$\begin{aligned}P_{\eta,Q} &= 1 - P_{\hat{y}(x,\sigma)} \\ &= 1 - \frac{1}{T}\int_0^T \hat{y}(x,\sigma)^2\,\mathrm{d}t\,,\end{aligned} \tag{5}$$

where $x(t)$ is the input signal and T is the signal period.

Since every sample of white noise is independent of each other, the noise at the output of the quantiser is also independent, and thus white. The noise at the output of the system is averaged by a filter, which leads to an output noise power formulated as:

$$P_{\eta,out} = \frac{f_{ENBW}}{\frac{1}{2}f_s} P_{\eta,Q}, \tag{6}$$

where f_{ENBW} is the equivalent noise bandwidth of the filter and f_s is the sampling frequency.

D. Signal-to-Noise-and-Distortion Ratio

The performance of the system can be defined using the signal-to-noise-and-distortion ratio (SNDR). This measure gives the ratio between the output signal power and the combined harmonic distortion and noise power. The SNDR is defined by

$$\mathrm{SNDR} = \frac{P_{out,signal}}{P_{HD} + P_{\eta,out}}. \tag{7}$$

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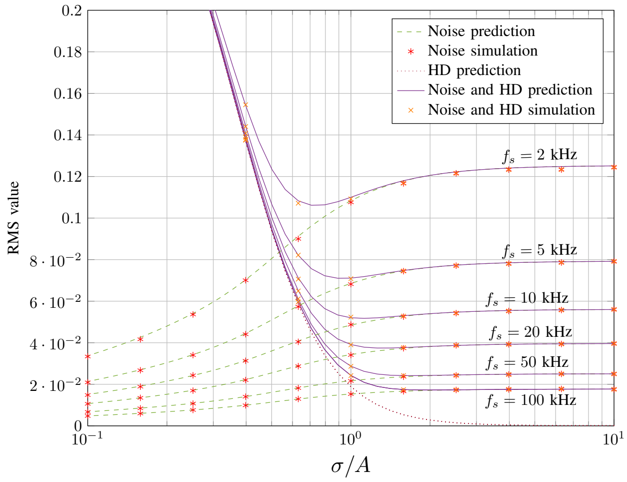

Fig. 3. RMS output error of the SR-ADC for a sine-wave input with a frequency of 1 Hz and $f_s = [2, 5, 10, 20, 50, 100]$ kHz. The output is filtered by a first-order Butterworth LPF with a cut-off frequency of 10 Hz. The RMS input noise σ is set to 1, while the input signal amplitude A is shifted from 0.1 to 10.

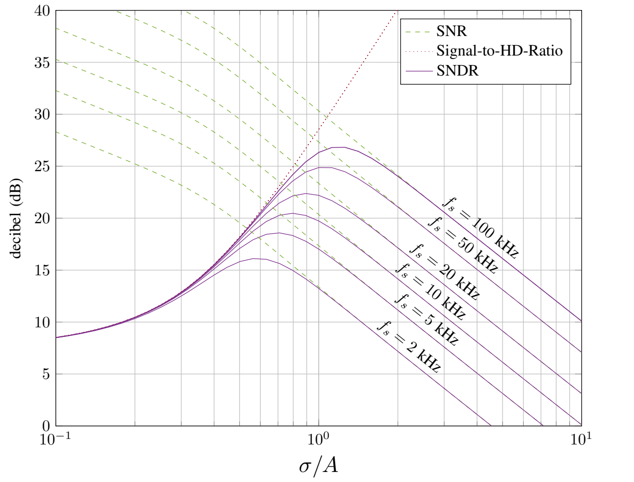

Fig. 4. Signal-to-noise-and-distortion ratio of the SR-ADC for a sine-wave input with a frequency of 1 Hz and $f_s = [2, 5, 10, 20, 50, 100]$ kHz. The output is filtered by a first-order Butterworth LPF with a cut-off frequency of 10 Hz. The RMS input noise σ is set to 1, while the input signal amplitude A is shifted from 1 to 10.

The output signal and harmonic distortion power are given by

$$P_{out,signal} = \hat{H}(x, \sigma)^2 P_{in,signal} \tag{8}$$

and

$$P_{HD} = \frac{1}{T} \int_0^T \Big(\hat{y}(x, \sigma, t) - \hat{H}(x, \sigma) \cdot x(t) \Big)^2 \, \mathrm{d}t \,, \tag{9}$$

respectively.

The results of the proposed method are verified for the case of a sine-wave input. In this example, the signal frequency is set to 1 Hz, the cut-off frequency is 10 Hz and the filter is a first-order Butterworth LPF. The input noise is white Gaussian noise with $\sigma = 1$, while the input signal amplitude (A) is shifted from 0.1 to 10. Fig. 3 shows the output error for $f_s = [0.2, 0.5, 1, 2, 5, 10]$ kHz. Alongside the analytical results, simulation results of the system are shown to validate the method. The final SNDR results for the same sample ratios are shown in Fig. 4. The figure clearly shows the performance peak. A higher sampling ratio gives a higher SNDR. For low noise levels, the distortion limits the behaviour, while for high noise values, the noise becomes the dominant source of error. It should be noted that these results only hold for a single sine-wave input. The waveform of the signal affects the noise as well as the harmonic distortion behaviour.

IV. SR-Based Mathematical Operations

Not only limited to analog-to-digital conversion and amplification, SR can also be used to do mathematical operations on signals. There are four fundamental mathematical operations: addition, subtraction, multiplication, and division. An SR-adder can be built by implementing a half-adder after the SR-ADCs. Consequently, a subtractor can be implemented by using a half-adder while inverting one of the SR-ADC outputs.

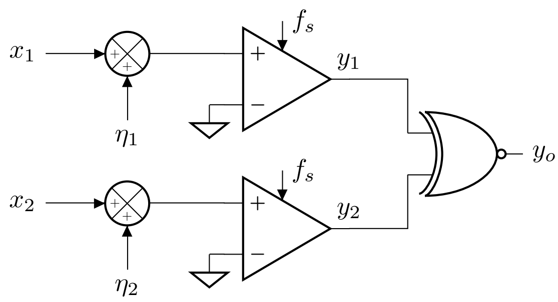

Fig. 5. Proposed SR-multiplier using an XNOR gate in combination with two SR-ADCs.

While a division might be difficult to implement due to the large value of $1/x$ when x is close to zero, a multiplication is feasible. In the next part, we demonstrate the design of a signal multiplier using two SR-ADCs.

A. SR-Multiplier

The output of the SR-ADCs is either $+V$ or $-V$ which corresponds to a logic "1" or "0", respectively. Therefore, the output of the proposed SR-multiplier should be "1", i.e. positive, when both outputs of the SR-ADCs are the same, and "0", i.e. negative, when they are different. Therefore, an SR-multiplier can be implemented with a combination of two SR-ADCs and an XNOR gate. The block diagram of the SR-multiplier is shown in Fig. 5. x_1 and x_2 denote the input signals while η_1 and η_2 are the input noise signals corresponding to each SR-ADC. η_1 and η_2 are independent of each other.

Using the probability of the SR-ADC output derived in

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Section III, the probability of $y_o = 0$ is

$$\begin{aligned}P(y_o = 0 \,|\, x_1, x_2) &= P(y_1 = 1 \,|\, x_1)P(y_2 = 0 \,|\, x_2) \\ &\quad + P(y_1 = 0 \,|\, x_1)P(y_2 = 1 \,|\, x_2) \\ &= -2P(\eta_1 < -x_1 \,|\, x_1)P(\eta_2 < -x_2 \,|\, x_2) \\ &\quad + P(\eta_1 < -x_1 \,|\, x_1) + P(\eta_2 < -x_2 \,|\, x_2).\end{aligned} \tag{10}$$

From (1) and (10), the expected output $\hat{y}(x_1, x_2, \sigma_1, \sigma_2)$ can be calculated by

$$\begin{aligned}\hat{y}\left(x_1, x_2, \sigma_1, \sigma_2\right) &= V\big(1 - 2P(y_o = 0 \,|\, x_1, x_2)\big) \\ &= V\Big(1 + 4P(\eta_1 < -x_1 \,|\, x_1)P(\eta_2 < -x_2 \,|\, x_2) \\ &\quad - 2\big(P(\eta_1 < -x_1 \,|\, x_1) + P(\eta_2 < -x_2 \,|\, x_2)\big)\Big).\end{aligned} \tag{11}$$

By substituting the $P(\eta_n < -x_n \,|\, x_n)$ with $\hat{y}_n$ using (1), as long as η_1 and η_2 are independent of each other, (11) can be rewritten as

$$\hat{y}\left(x_1, x_2, \sigma_1, \sigma_2\right) = \frac{\hat{y}_1(x_1, \sigma_1) \cdot \hat{y}_2(x_2, \sigma_2)}{V}, \tag{12}$$

which shows that the proposed operator is a multiplier. For an SR-multiplier using white Gaussian noise sources, (12) becomes

$$\hat{y}(x_1, x_2, \sigma_1, \sigma_2) = V \operatorname{erf}\left(\frac{x_1}{\sqrt{2}\sigma_1}\right) \operatorname{erf}\left(\frac{x_2}{\sqrt{2}\sigma_2}\right). \tag{13}$$

B. Signal-to-Noise-and-Distortion Ratio

To determine the gain, distortion, and output noise power, the methods presented in Section III can be used by substituting (13) for $\hat{y}$ in (5). The gains $\hat{G}$ in case of two sinusoidal inputs $\sin(2\pi t)$ and $\sin(2\pi t + \phi)$ are shown in Fig. 6. The SR-multiplier is subjected to independent white Gaussian noise sources with equal power, denoted by σ^2. V is set to 1 and $\phi = \left[-\frac{\pi}{2}, -\frac{\pi}{2} \pm \frac{\pi}{6}, -\frac{\pi}{2} \pm \frac{\pi}{2}\right]$, such that the correlation coefficient of the input signals, $\rho = [0, \pm 0.5, \pm 1]$. The signals are sampled with $f_s = 100$ kHz and the outputs are filtered by a second-order Butterworth LPF with a cut-off frequency of 10 Hz. The case with zero correlation ($\phi = -\pi/2$) has the biggest gain due to its output having zero mean, which leads to a lower distortion power. As the noise RMS value σ goes up, the gains go down approaching $2V/\left(\pi\sigma^2\right)$, shown by the solid line.

The simulated and predicted SNDRs for the same cases are presented in Fig. 7. SNDR peaks can be observed for every case where noise is present due to the stochastic resonance.

V. Conclusions

In this paper, a novel signal conversion and signal processing technique has been discussed. As two examples, an SR-ADC and an SR-multiplier have been introduced.

In Section III, an analytical method to determine the performance of a fully stochastic resonance ADC is proposed. Based on the expected output of the quantiser, the signal power, distortion power and noise power are derived. Since the spectrum of white noise is preserved by the quantisation step, the filtered output noise can be calculated. The method can be used for all (periodic) input signals combined with Gaussian, as well as non-Gaussian white noise. The method is developed to allow structured analysis of SR-ADC systems for design purposes and can also be applied to SR-ADCs with integrated signal processing.

In Section IV, we have shown that SR can be used to do mathematical operations. Using the stochastic properties of the 1-bit signal acquired by the SR-ADC, a compact and efficient signal multiplier using an XNOR logic gate can be designed. It is proven that the proposed operator works as a multiplier as long as the noise sources are independent of each other.

The observations presented in this paper show a potential for analog to digital conversion and integrated signal processing fully based on stochastic resonance. For low-frequency signal reconstruction in high-noise environments, the SR-ADC can be a simple and efficient alternative for conventional analog front-ends and signal processing.

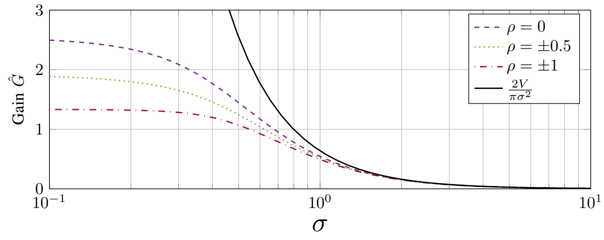

Fig. 6. Gain of the SR-multiplier for $x_1 = \sin(2\pi t)$ and $x_2 = \sin(2\pi t + \phi)$. V is set to 1 and $\phi = \left[-\frac{\pi}{2}, -\frac{\pi}{2} \pm \frac{\pi}{6}, -\frac{\pi}{2} \pm \frac{\pi}{2}\right]$ such that $\rho = [0, \pm 0.5, \pm 1]$. η_1 and η_2 are white, independent, and have equal RMS values σ. As σ goes up, the gain approaches $2V/\left(\pi\sigma^2\right)$.

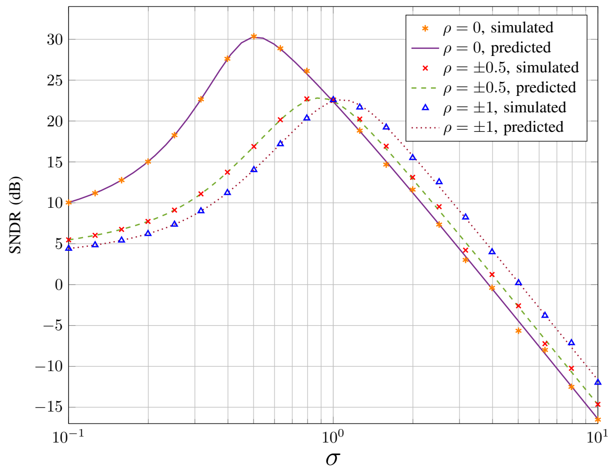

Fig. 7. Signal-to-noise-and-distortion ratio of the SR-multiplier for $x_1 = \sin(2\pi t)$ and $x_2 = \sin(2\pi t + \phi)$, sampled with $f_s = 100$ kHz and filtered by a second-order Butterworth LPF with a cut-off frequency of 10 Hz. V is set to 1 and $\phi = \left[-\frac{\pi}{2}, -\frac{\pi}{2} \pm \frac{\pi}{6}, -\frac{\pi}{2} \pm \frac{\pi}{2}\right]$ such that $\rho = [0, \pm 0.5, \pm 1]$. η_1 and η_2 are white, independent, and have equal RMS values σ. The marks indicate the simulated results and the lines are the predicted results based on the formula. SNDR peaks can be found at different σ for different cases.

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