Subsampling based Software Defined Radio with Jitter Compensation

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***Abstract*—The subsampling based Software Defined Radio (SuSDR) architecture features low power consumption and reconfigurability. However, the major drawback of the SuSDR is its poor reliability and robustness due to the poor noise performance. Although jitter compensation techniques have been proposed to improve the noise performance of the SuSDR, those methods are very complicated to implement in hardware. Moreover, since the accuracy of the numerical operation is not taken into consideration in those methods, the effectiveness of those compensation methods can be questioned. In this paper, a SuSDR architecture with jitter compensation is proposed, and implementation imperfections like the accuracy of the ADC are taken into account. Using the analysis, the requirements for the ADCs and the reference frequency can be derived from the system specifications, and this will lead to a practical implementation of the proposed architecture. In conclusion, the SuSDR with the proposed jitter compensation technique can be a promising low power, reconfigurable and robust wireless architecture for wireless sensor networks (WSN).**

I. Introduction

The subsampling based Software Defined Radio (SuSDR) architecture [1] [2] is one of the promising receiver architectures which might fulfill the features of low power consumption and reconfigurability. In the traditional subsampling based SDR, the signal will be first down-converted into a lower frequency band by the subsampling operation, and then digitized by an analog-to-digital converter (ADC) working at a lower frequency compared to the Nyquist rate sampling of the RF carrier frequency, yet still the sampling frequency should be large enough to capture the signals in the target frequency band. In this way, the reconfigurability of this receiver architecture can be guaranteed since the digital signal processing algorithm can be easily programmed.

In order to minimize the power consumption of the SuSDR, the sampling frequency will be relatively low. In such a situation, major concerns for the SuSDR are its reliability and robustness as they suffer from the poor noise performance. In the SuSDR, there are two main noise sources, namely the folding noise and jitter introduced noise [3] [4]. Because of the spectrum folding in the sampling process, wideband noise will be folded into the sampling bandwidth, which increases the in-band noise power. However, by applying an anti-aliasing band selection filter at the receiver front-end, the folded noise can be greatly reduced. To reduce the jitter introduced noise, a clock generator with low jitter is needed. However, a low jitter clock is not always available. As a result, methods to mitigate the jitter introduced noise in the presence of a noisy clock have been developed [5][6][7]. In these methods, a reference is injected into the signal path, and then by filtering of the sampled output, the reference signal and the wanted signal can be separated. The jitter information can be estimated from the sampled reference, and the jitter in the sampled wanted signal can be compensated.

Although these methods can effectively reduce the jitter introduced noise power in theory, in the implementation, there are more issues to consider. First of all, filtering operations will be required in order to separate the reference and wanted signals, which likely increase the complexity and power consumption. Secondly, in those methods, all the jitter cancellation is done assuming the accuracy of the sampled signal is very high. However, in practice, all the numerical operations can only be done within a certain accuracy. Finally, the injected reference may be a strong interferer since it might be close to the desired channel.

To overcome these problems, a new SuSDR architecture is proposed [8] as shown in Fig 1. In this architecture, the reference is injected into another path which is subsequently sampled by the same sampling clock. In this way, since the sampling clocks for the two sampling branches are the same, the jitter information can still be estimated from the reference without interfering with the wanted signals.

In this paper, firstly the jitter compensation technique for the proposed architecture is presented in Section II. In Section III, the accuracy of the ADC is taken into consideration for the noise analysis, and the effectiveness of the compensation technique is examined. Then simulation results are presented in Section IV, and finally we conclude this paper in Section V.

II. Proposed Jitter Compensation Technique

The receiver input signal can be presented in its complex form $\hat{x}(t)$ as

$$\hat{x}(t) = \hat{X}(t)e^{-j2\pi f_c t}. \quad (1)$$

$\hat{X}(t)$ is the baseband complex signal, and f_c is the carrier frequency.

The jittered samples of the complex signal can be written as:

$$\hat{x}_k = \hat{X}(kT_s + \delta t_{jk})e^{-j\phi_k}, \quad (2)$$

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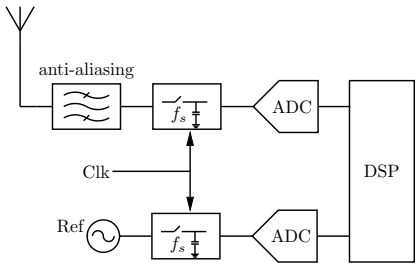

Fig. 1. Proposed Subsampling SDR architecture with jitter compensation. The reference and the RF signal are sampled by the same clock in separated paths.

$$\phi_k = 2\pi f_c(kT_s + \delta t_{jk}) \tag{3}$$

where T_s is the sampling clock period, $f_s = 1/T_s$ is the sampling frequency, and δt_{kj} is the clock jitter.

Assuming that a reference signal at frequency f_{ref} is sampled by the same sampling clock as the input signal, then the sampled reference complex signal $\hat{x}_{k_{ref}}$ is

$$\hat{x}_{k_{ref}} = \hat{x}_{ref}(kT_s + \delta t_{jk}) = e^{\phi_{k_{ref}}}, \tag{4}$$

$$\phi_{k_{ref}} = 2\pi f_{ref}(kT_s + \delta t_{jk}). \tag{5}$$

As shown in the equation, the jitter can be expressed as phase noise in the sampled output reference, and hence the phase information of the reference can be used to compensate the sampling jitter. If N is defined as

$$N = f_c/f_{ref}, \tag{6}$$

the compensated output $\hat{y_k}$ will become

$$\hat{y_k} = \hat{X}(kT_s + \delta t_{jk})e^{-j(\phi_k - N\cdot\phi_{k_{ref}})} = \hat{X}(kT_s + \delta t_{jk}). \tag{7}$$

This suggests that the jitter compensation can be done in the following way, as shown schematically in Fig. 2. First the complex input signal and a clean reference will be sampled by the same sampling clock. The phase information in both sampling branches will be estimated and the amplitude information in the sampled signal branch will be estimated. Since the sampled signals are already digitized, this estimation can be done in a DSP quite easily. By subtracting N times the reference signal phase information from the sampled target signal, as suggested in (7), cleaner phase information with less jitter will be derived. Finally, using this clean phase information and the amplitude information of the signal, an output sampled signal with less jitter introduced noise can be reconstructed.

III. Noise Analysis

In reality, there are also some imperfections which introduce additional noise, for example the noise in the reference signal, the phase mismatch in the sampling clock for the two branches caused by aperture jitter, circuit noise, aperture jitter for the two samplers, etc. However, all these effects can be equivalently modeled as noise in the reference clock. This equivalent noise will affect the compensation performance.

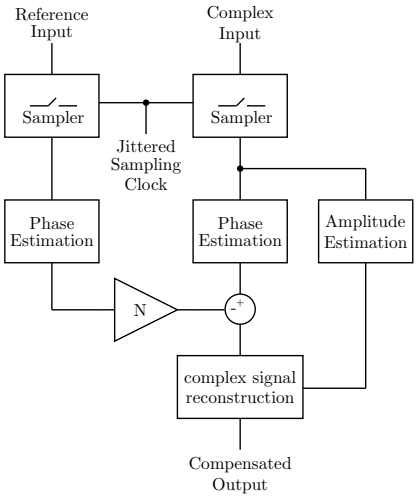

Fig. 2. Diagram for jitter compensation. The operations except for the sampling are carried out in a DSP. The phase estimation and the amplitude estimation can be easily implemented from the sampled complex values.

Meanwhile, the accuracy of the the ADC, which determines the accuracy of the numerical operations in the DSP, also plays an very important role in the compensation performance. Both effects will be discussed in the following subsections.

A. Noise in the reference

For simplicity, all the noise effects can be modeled as an equivalent noise in the reference signal, and its influence can be described as another jitter term in the sampled reference signal. The detected phase of the noisy reference signal can then be expressed as

$$\phi_{k_{ref}} = 2\pi f_{ref}(kT_s + \delta t_{jk} + \delta t_n), \tag{8}$$

in which δt_n stands for the jitter term from the noise in the reference signal. This reference jitter term can be calculated using the sampled reference $\mathrm{SNR_{Ref}}$ using the following equation.

$$\mathrm{SNR_{Ref}} = -20\log(\phi_{k_{ref}}), \tag{9}$$

In this proposed compensation technique, the phase information of the reference signal will be amplified by N as defined in (7), the noise in the reference signal will also be amplified. Thus, considering the noise in the reference signal, the compensated output is

$$\begin{aligned} \hat{y_k} &= \hat{X}(kT_s + \delta t_{jk})e^{-j(\phi_k - N\cdot\phi_{k_{ref}})} \\ &= \hat{X}(kT_s + \delta t_{kj})e^{-j2\pi f_c \delta t_n}. \end{aligned} \tag{10}$$

Comparing (10) with (2), it is clear that this compensation technique will be effective only if the jitter in the reference signal is much smaller than the jitter in the sampling clock.

B. Accuracy of the ADC

The accuracy of the ADC is also very important to the performance. It is known that the quantization noise of the

ADC can be viewed as white noise, and the quantized output SNR can be calculated using

$$\text{SNR}_{\text{ADC}} = 6.02 \cdot \text{ENOB} + 1.76, \tag{11}$$

where ENOB is the effective number of bits.

In the proposed system, after the quantization of the ADC, the RF signal and the reference can be expressed as

$$\hat{x}_{kAD} = \hat{X}(kT_s + \delta t_{jk}) e^{-j\phi_k} e^{-j\phi_m}, \tag{12}$$

$$\hat{x}_{kAD_{ref}} = \hat{x}_{ref}(kT_s + \delta t_{jk}) = e^{\phi_{k_{ref}}} e^{-j\phi_n}, \tag{13}$$

where ϕ_m and ϕ_n are the effective phase noise terms caused by the quantization noise. The root mean square (RMS) value of ϕ_m and ϕ_n can be calculated as

$$\text{SNR}_{\text{ADC}} = -20\log(\text{RMS}(\phi_m)) = -20\log(\text{RMS}(\phi_n)) \tag{14}$$

The compensated output $\hat{y}_{kAD}$ is

$$\hat{y}_{kAD} = \hat{X}(kT_s + \delta t_{kj}) e^{-j(\phi_m + N\phi_n)} \tag{15}$$

Comparing (15) with (2), it is clear that this compensation technique will be effective only if the power of the noise term $e^{-j(\phi_m + N\phi_n)}$ in (15) is smaller than the noise term $e^{-j(2\pi f_c \delta t_{jk})}$ in (2). If a compensation gain G in SNR is expected compared to the uncompensated signals, this means

$$\text{SNR}_{\text{ADC}} - 10\log(N^2 + 1) > -20\log(2\pi f_c \delta t_{jk}) + G \tag{16}$$

This gives the requirement for the ENOB of the ADC, which is

$$\text{ENOB} > \frac{10\log(N^2 + 1) - 20\log(2\pi f_c \delta t_{jk}) - 1.76 + G}{6.02} \tag{17}$$

This equation gives the boundary condition for the effective compensation. For example, if the clock jitter is 10 ps, the RF carrier frequency is 2.4 GHz, the reference clock is 30 MHz and the compensation gain is 3 dB, then ADCs with a least an ENOB of 9.25 bit should be used. If the ENOB cannot satisfy this equation, then the compensation method only introduces more noise to the output signal. In that case, it is better not to use the compensation technique.

IV. Simulation Results

Both the spectrum and the bit error rate (BER) are compared in this section for the evaluation of the proposed jitter compensation technique.

Fig. 3 shows the spectrum of the sampled signals with and without jitter compensation. The input is a 8 differential phase-shift keying (D8PSK) modulated signal with a symbol rate of 1 MHz centered at 2.4 GHz. An additive white Gaussian noise (AWGN) channel is assumed. The sampling frequency is 40 MHz. Meanwhile, the reference signal is a 10 MHz clean sinusoidal signal. The ADCs are assumed to have very high accuracy. In the simulation the sampling clock RMS jitter is 20 ps, and the input signal has a good SNR so that the noise in the sampled signal without compensation is dominated by the clock jitter. After compensation, the noise in sampled signal

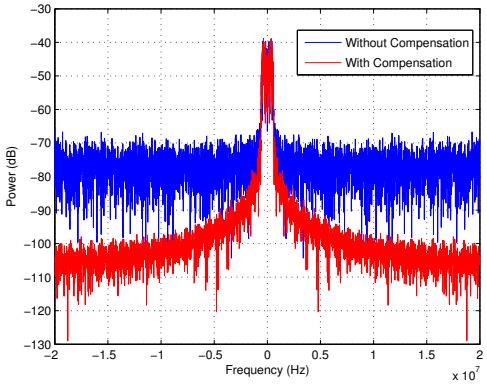

Fig. 3. Spectrum comparison of a sampled narrow band signal with and without jitter compensation. A clean 2.4 GHz input signal is down-converted to 0 Hz by a 40 MHz jittered sampling clock.

is greatly reduced. Clearly, the jitter compensation technique improves the noise performance.

In another simulation scenario, again a D8PSK signal with a symbol rate of 1 MHz centered at 2.4 GHz is sampled with varying sampling clock jitter. Fig. 4 shows the changing BER with respect to the RMS jitter value when the input signal with an Eb/No of 20 dB is sampled by a 100 MHz clock. The reference is 10 MHz and clean. The ADCs are also assumed to be ideal. Without compensation, the BER performance decreases as the clock jitter increases, since the noise in the clock will decrease the SNR of the output signal. On the other hand, the BER performance remains almost the same for the compensated output, since in this case the BER performance is dominated by the SNR performance of the input signal, while the jitter introduced noise can be well compensated. Compared to the compensation method proposed in [6], our proposed method can still have good performance even when the clock jitter is very large.

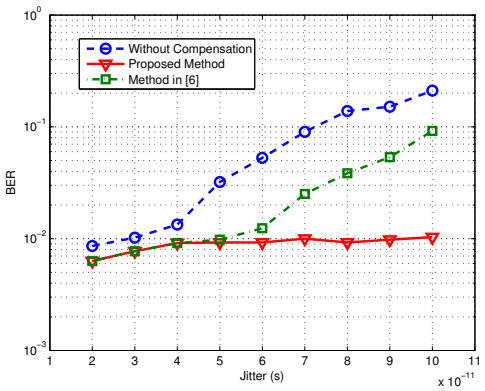

Fig. 4. BER performance comparison for modulated signals without compensation, with compensation method in [6] and our proposed method.

Fig. 5 demonstrates the BER performance as a function of the reference signal jitter. This time, the same RF input modulated signal as in the previous cases has a fixed Eb/No of

10 dB, and the 100 MHz sampling clock has an RMS jitter of 10 ps. Ideal ADCs are also applied here, however, the 10 MHz reference signal has a certain noise power which is expressed as an RMS jitter here. As expected from the previous analysis, the compensation effectiveness is now mainly relying on the RMS jitter value of the reference signal. If the jitter in the reference clock is almost the same as in the sampling clock, then the BER performance is the same. Only when the jitter in the reference clock is smaller than that of the sampling clock, the BER performance enhancement can be observed. Normally, signals from quartz crystal oscillators are pure and clean compared to sampling clocks, thus they are good candidates for the reference signals.

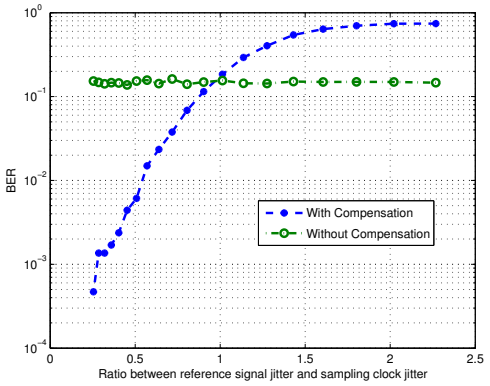

Fig. 5. BER performance for different reference jitters with and without compensation.

In the previous simulations the accuracy of the ADCs is not taken into consideration. Fig. 6 demonstrates the SNR performance of the compensated output as a function of the ENOB of the ADCs and N, which stands for the ratio between the RF carrier frequency and the reference frequency. In this case, a 2.4 GHz RF tone is sampled by a 100 MHz clock with an RMS jitter of 50 ps. As expected, the SNR of the compensated output will increase with respect to the increasing ENOB, and decrease when N increases. The contour lines suggest that if the RF carrier frequency is known, the reference frequency and the ENOB of ADCs along the contour line should have the same performance.

Concluding the above discussions, with this jitter compensation technique, the jitter requirements for the sampling clocks can be much relaxed since jitter introduced noise can be reduced. Also, from the jitter performance and the RF carrier frequency, the design parameters like the reference frequency and the accuracy of the ADCs can be chosen. Hence, even in the presence of clock jitter, good reliability and performance can be reached by applying this jitter compensation technique.

V. Conclusion

The SuSDR architecture is one of the candidate receiver architectures to achieve both low power consumption and reconfigurability for WSN. A SuSDR architecture as well as its jitter compensation technique is proposed to deal with the clock jitter and improve the performance. By applying this technique, the noise due to the clock jitter can be reduced. The compensation performance related to the accuracy of the ADCs in the architecture is examined, and the requirements for the ADCs and the reference frequency can be derived from the system specifications. This will lead to a realistic implementation of the proposed SuSDR. In conclusion, the SuSDR with the proposed jitter compensation technique can be a promising low power, reconfigurable and robust wireless architecture for WSN.

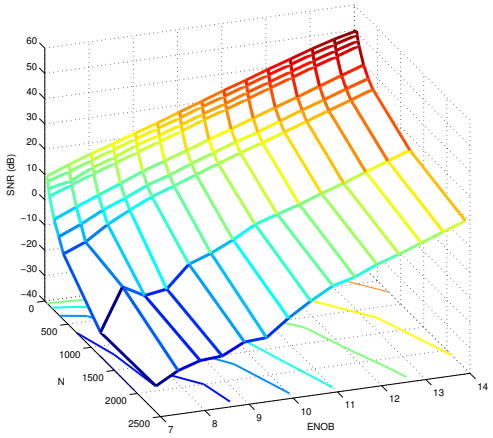

Fig. 6. SNR performance of the compensated signal with different ADC accuracy ENOB and the ratio N between carrier frequency and reference frequency.

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