A 2.6nW, 0.5V, 52dB-DR, 4th-order G_m-C BPF: Moving Closer to the FoM's Fundamental Limit

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***Abstract*— A nano-power 4th-order band-pass filter operating from a 0.5 V supply voltage with an adjustable center frequency, ranging from 250 Hz to 4 kHz (4 octaves), is presented. The filter is constituted from cascadable 2nd-order circuit cells that are realized by a network of three transistors and two capacitors comprising only one branch of bias current. As a result of the compact low voltage circuit architecture, a dynamic range of 52 dB is obtained, which leads to best figure of merit achieved among other existing designs.**

I. INTRODUCTION

The term 'figure of merit (FoM)' that combines several circuit or signal parameters in a certain formula is helpful to have a reasonable comparison between several designs. For biomedical band-pass filter (BPF) designs that have a low center frequency (audio range and below) and a power consumption less than 1 μW [1]-[5], the FoM defined by

$$\mathrm{FoM} = \frac{P \cdot V_{\mathrm{DD}}}{N \cdot f_C \cdot \mathrm{DR}}, \qquad (1)$$

has been introduced in [2] and used since then in [3]-[5], where P, V_{DD}, N, f_c, and DR are power consumption, supply voltage, order, center frequency and dynamic range of the filter, respectively. It is quite straightforward that the cost (numerator) over the performance (denominator) should be as low as possible. This suggests that to enhance the FoM, a filter circuit that contains the least amount of current branches and can operate from a very low V_{DD} is required. Computing (1) by using the concept of minimum possible energy per cycle and per pole [7] (derived from a 1st-order G_m-C low-pass filter in which the G_m cell operates with 100% efficiency) gives a lower limit at room temperature of $\mathrm{FoM} = 3.31 \cdot V_{\mathrm{DD}} \times 10^{-20}$ JV.

A FoM plot versus V_{DD} from selected compact low-power BPF designs collected over 2003 to 2011 is shown in Fig. 1. Within 8 years, the FoM has improved by slightly more than two orders of magnitude. It is interesting to see that the BPFs of [4] and [5] provide almost the same FoMs (0.89×10^{-13} and 1×10^{-13}, respectively) despite different techniques. In [4], a simple cascade topology (which has also been used in [1]) formed by a compact G_m-C biquad structure adapted from [6] was employed while the BPF of [5] uses

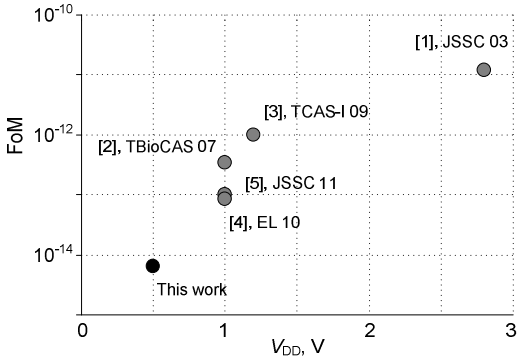

Figure 1. Figure of merit comparison of G_m-C band-pass filters collected over 2003-2011.

conventional differential pair transconductors to simulate a ladder passive LC prototype. Compared to the fundamental limit for V_{DD} = 1V, we can see that the FoM of [4] is still more than 6 orders of magnitude away from the fundamental limit.

In this paper, we develop further to achieve more than one order of magnitude FoM improvement with respect to [4]. This can be done by inventing a 2nd-order filter topology that is able to operate from a lower supply voltage and can be cascaded without the expense of a voltage buffer and be fit into a power-efficient single branch circuit structure that uses a single transistor as the transconductance element. In the next section, the proposed design including the details of the filter topology selection, transistor level architectures, bias point considerations, and noise analysis will be presented. Sec. III presents post-layout simulation results and a comparison to the previously established designs. Discussion and conclusions will be given in the last section.

II. PROPOSED DESIGN

A. Cascadable 2nd-order G_m-C Topology

Fig. 2a shows the 2nd-order BPF topology used in [1] and [4]. Capacitor C_1 with transconductor G_{m1} and C_2 with G_{m2} form the high-pass and low-pass cutoff sections, respectively. For higher order realization, a cascade connection of this circuit is required. Unfortunately, to prevent any loading effect, a voltage follower is needed to be inserted in front of

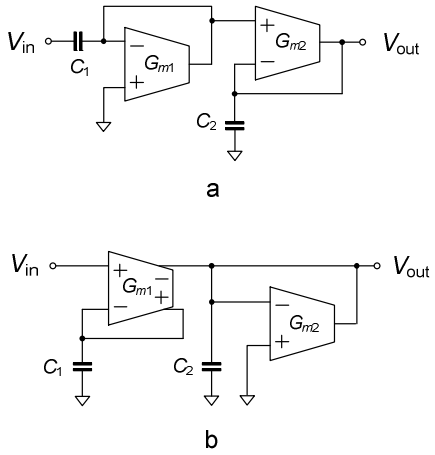

Figure 2. 2nd-order BPFs. (a) Topology of [1]. (b) Topology used in this. work

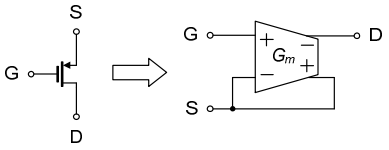

Figure 3. Single transistor and its macro-model.

the input stage [1] [4]. This leads to more chip area and power consumption.

Using a differential output G_m cell in the input stage can avoid the loading problem mentioned above. Fig. 2b shows the proposed 2nd-order G_m-C BPF topology that provides a transfer function of

$$H_{BP}(s)=\frac{-s\dfrac{G_{m1}}{C_2}}{s^2+s\left(\dfrac{G_{m2}}{C_2}+\dfrac{G_{m1}}{C_1}\right)+\dfrac{G_{m1}G_{m2}}{C_1C_2}}. \qquad (1)$$

For $G_{m1}=G_{m2}$ we have,

$$\omega_o=\frac{G_m}{\sqrt{C_1C_2}},\quad Q=\frac{\sqrt{C_1C_2}}{C_1+C_2},\quad K=\frac{C_1}{(C_2+C_1)}, \qquad (2)$$

where parameters ω_o, Q and K stand for the center frequency, the quality factor and the mid-band gain, respectively. As this structure has a high-impedance input port, the cascade connection for higher order realization does not need an additional buffer circuit. Moreover, at transistor level, the proposed structure can be formed within a compact single branch transistor-capacitor network and, as a consequence, an adjustable center frequency from the adjustable bias current is achieved.

B. Using All Terminals of a Single MOSFET

For a MOSFET that is properly biased in weak inversion saturation, a differential G_m cell connected in negative feedback fashion as shown in Fig. 3 can be obtained from the small signal operation of the transistor. Comparing Fig. 3 with Fig. 2b shows that each transistor in the proposed filter topology (Fig. 2b) can be replaced by a single transistor. For G_{m1}, the bulk terminal is connected to the source terminal to avoid the body effect and for this reason a pMOS device is preferred in an n-well CMOS process. In this case all terminals are used and, fortunately, forming a signal path vertically by a single branch structure is possible.

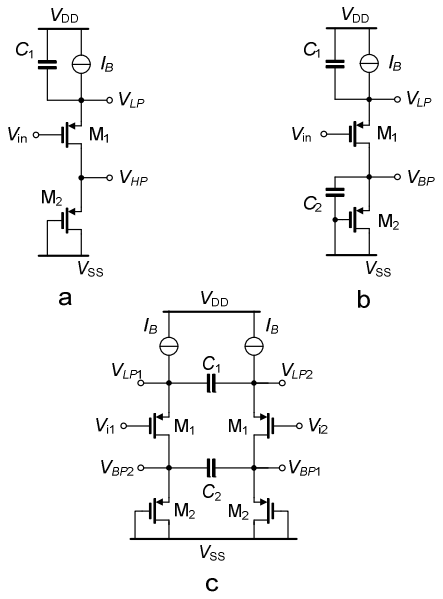

Figure 4. Single branch filter circuits. (a) 1st-order BP and HP filters. (b) 1st-order LP and 2nd-order BP filters. (c) Differential structure of the 1st-order LP and 2nd-order BP filters.

C. 2nd-order BPF on a Single Branch Bias Current

Fig. 4 shows possible realizations of single-branch G_m-C filters; low-pass (Figs. 4a and 4b), high-pass (Fig. 4a) and band-pass filter (Fig. 4b) transfer function can thus be realized. The proposed filter (Fig. 2b) can be made compact and power efficient by the circuit shown in Fig. 4b while M_1 and M_2 are acting as G_{m1} and G_{m2}, respectively. Note that the equivalent operation of the proposed macro-model and the circuit is valid only for the small signal condition. As a consequence, a differential structure as shown in Fig. 4c is required to maximize the filter's dynamic range. In this case bias current I_B defines the transconductances

$$g_{m1}=\frac{G_{m1}}{2}=g_{m2}=\frac{G_{m2}}{2}=\frac{I_B}{nU_T}, \qquad (3)$$

where n and U_T represent the sub-threshold slope factor and the thermal voltage, respectively. According to (2), ω_o is now adjustable by I_B.

D. Supply Voltage Requirement and Current Consumption

The proposed differential 4th order BPF is formed by a cascade connection of the circuit cell depicted in Fig. 4c. A total current consumption of $4I_B$ is found. In summary, the

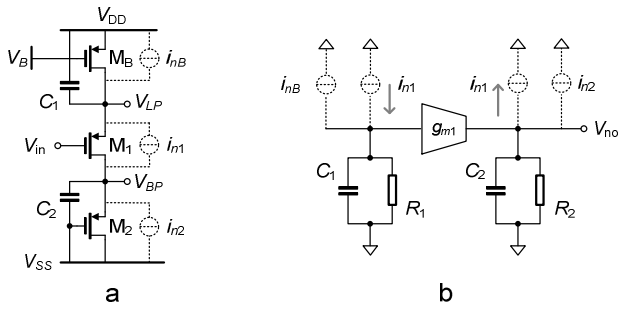

Figure 5. BPF with noise sources. (a) Transistor circuit. (b) equivalent model.

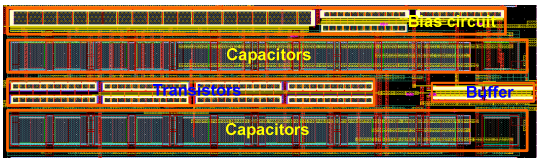

Figure 6. Chip Layout of the proposed BPF.

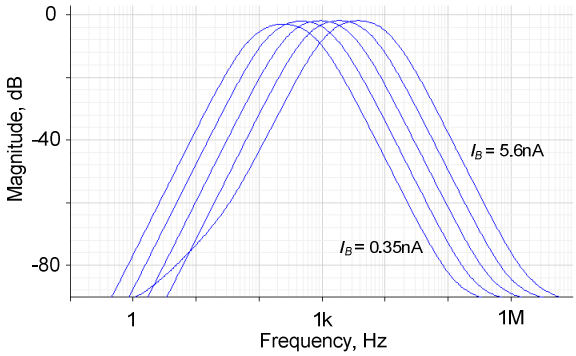

Figure 7. Magnitude response of the proposed BPF.

current consumption equals $0.5I_B$ and I_B per filter's order for single-ended and differential structures, respectively.

To arrange proper bias points in weak inversion saturation, V_{DD} and common mode level V_{CM} should be considered. For the stacked circuit shown in Fig. 4, the supply voltage required must be at least $V_{DD} = V_{SG} + 2V_{SDsat}$ (assuming that I_B requires one V_{SDsat}). For deep sub-threshold operation of the transistor in our 0.18µm technology with a nominal threshold voltage of $V_{tp} \cong -0.42$V, $V_{DD} = 0.5$V is sufficient to provide room for linear signal swing (a few tens mV limited by the exponential behavior of the transistors) and to keep all transistors in weak inversion saturation. To maintain the same signal swing range for all cascaded stages, V_{CM} of every stage should be equal to $V_{CM} = V_{SS}+V_{SG2}$.

E. Noise

Fig. 5a shows a single branch 2nd-order BPF circuit and its noise sources. In practice, I_B can be formed by a single transistor with its biased gate terminal M_B. Assuming each transistor is sized large enough and its drain current is low enough to keep the $1/f$ noise corner frequency lower than the frequency of interest, the transistor's weak inversion noise behavior will be dominated by its shot noise. Equivalent current noises i_{nB}, i_{n1} and i_{n2} will have the same power spectral density of $2qI_B$.

Fig. 5b illustrates a simplified equivalent model for the noise calculation that assumes the drain-source conductance of each transistor is negligible when compared to its g_m. First noise current i_{nb} and i_{n1} are combined and flow through the low-pass network comprising C_1 and R_1 ($= g_{m1}^{-1}$). The resulting noise voltage will be converted into an output current noise by g_{m1} and will combine with $-i_{n1}$ and i_{n2} and together flow through another low-pass network, C_2 and R_2 ($= g_{m2}^{-1}$). Subsequently, output voltage noise v_{no} appears at the output port. Note that the current noise of M_1 appears at both the input and the output ports of g_{m1} (i_{n1} and $-i_{n1}$, respectively), leading to two current sources that are correlated and will cancel each other to a certain extent. Following the aforementioned mechanism, an average output noise power can be found that equal

$$\overline{v_{on}^2} \cong \frac{2nkT}{C_1 + C_2} \quad . \tag{4}$$

For a differential version (Fig. 4c), this value will double.

III. Post-Layout Simulations

A cascaded version of the circuit in Fig. 3c forming a 4th-order band-pass filter has been designed and simulated in 0.18-µm AMS CMOS technology with a nominal threshold voltage of $V_{tp} \cong -0.42$ V. The chip layout of the filter is shown in Fig. 6. Including the filter core (pMOS transistors and dual MIM capacitors $C_1 = 10C_2 = 9$ pF), bias circuit (formed by simple scaled current mirror circuits) and source follower buffers to drive off chip loads, the chip occupies 64µm×225µm. The following results are obtained from post-layout simulations under the condition of $V_{DD} = 0.5$ V for the BPF and bias circuits, $V_{DD} = 1.8$ V for the buffers and the common mode level set to 0.15 V.

Fig. 7 shows the simulated magnitude of the frequency response of the proposed filter for I_B ranging from 0.35 nA to 5.6 nA. The f_c moves almost linearly for 4 octaves, starting from 250 Hz to 4 kHz, according to the values of I_B. $K \cong -2$ dB. Observing the lowest f_c that associates with $I_B = 0.35$ nA, we can see that K starts decreasing. At this point, the diode connected M_2 is forced to leave the weak inversion saturation by its drain-source voltage being reduced by I_B. It affects the magnitude response and gives a lower limit to the filter's adjustability. The upper limit is defined by V_{DD}. When I_B goes high, the gate-source voltages of all transistors will go up and for $I_B = 5.6$ nA the source voltage of M_1 and V_{DD} start forcing M_B out of its saturation region. This implies that we can widen the tuning range by supplying more V_{DD}.

Monte-Carlo simulations with 100 runs for the case of $I_B = 1.4$ nA which corresponds with $f_c = 1$ kHz are also given for two cases:

1. A transient simulation when a sinusoidal input voltage with frequency and amplitude of 1 kHz and 23 mV, respectively, is applied. The total harmonic

distortion (THD) has been calculated and plotted in Fig. 8. With a resulting standard deviation, σ, of 0.004 %, a THD of 1.1 % is obtained.

2. The integrated input referred noise (IRN) is plotted in Fig 9. A σ of 18.7 nV_{rms} (0.05 %) is obtained. An average noise voltage less than 40 μV_{rms} is obtained.

According to the THD and IRN obtained from these two simulations, the proposed filter's DR equals 52.2 dB.

Other filter parameters were tested, summarized and compared to those of previously reported BPFs. The results are shown in Table 1. The main distinct features of our design are the 0.5 V V_{DD} and the FoM of 0.063×10^{-13} which is more than an order of magnitude better than that of [4], the lowest number reported until recently. The BPF of [4] and ours are comparable in circuit complexity and process technology but the pMOS 2nd-order circuit cell of [4] cannot be connected in cascade without considerable loading effect and the circuit itself requires a higher V_{DD} of $2V_{SG}+V_{SDsat}$. It is also interesting to see that the 7th-order BPF of [5] consumes extremely little power of 60 pW which is almost 45 times smaller than that of our design, but it does not provide the best FoM since its f_c is only 2 Hz.

IV. Conclusions and Discussion

A smart choice of a filter topology and a very compact circuit that operates from a very low supply voltage are the keys to the design of a BPF that achieves a good FoM. Post-layout simulations of the proposed BPF filter, designed according to the keys mentioned above, show a great FoM improvement with respect to other existing designs. Following the time line of Fig. 1, a three orders of magnitude FoM improvement has been achieved during this last decade.

As it is widely known that for a smaller process technology, smaller parasitic capacitances and better flicker noise performance can be expected, the process technology and active chip area, however, are not included in (1). This makes the use of this FoM questionable in our opinion. The FoM should be redefined in such a way that it covers the chip area and the process technology. For instance in [8], a FoM that covers the relevant parameters of low-pass filters plus chip area and threshold has been used giving a more reasonable estimation.

Hopefully, in the near future, a new BPF's FoM will be introduced as well as new design techniques that can enhance further the relevant filter performance to get closer to the fundamental limit of the FoM.

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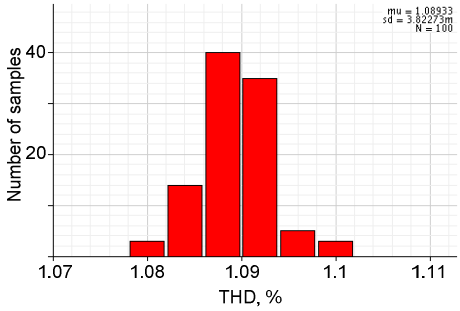

Figure 8. 100 runs Monte-Carlo simulation of THD

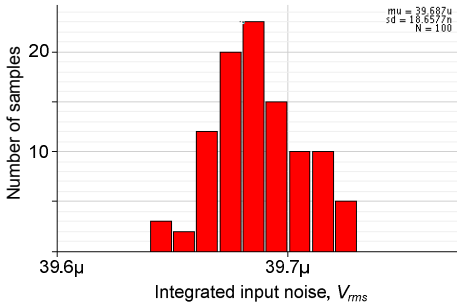

Figure 9. 100 runs Monte-Carlo simulation of noise

TABLE I. Performance Summary and Comparison

Filter parameters	[1] 2003	[2] 2007	[3] 2009	[4] 2010	[5] 2011	This work*
Tech. [µm]	1.5	0.35	0.18	0.18	0.35	0.18
order	4	6	8	4	7	4
f_c [Hz]	141	671	3.5k	732	2	1k
P [nW]	230	68	875	14.4	0.06	2.6
V_{DD} [V]	2.8	1	1.2	1	1	0.5
DR [dB]	67.5	49	37	55	43	52.2
IRN [μV_{rms}]	776	50	NA	50	51	40
THD [%]	5	NA	NA	1	0.3	1.1
FoM [10^{-13}]	119	3.4	10.1	0.89	1	0.063

*simulated