A Modular Transconductance Reduction Technique for Very Low-Frequency G_m-C Filters

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Abstract—**This paper presents a modular technique for transconductance reduction of a sub-threshold transconductor. This technique employs an ordinary differential pair circuit as a module to build a linear attenuator and to be the main transconductor. By applying the linear attenuation, the input linear range expansion and transconductance reduction are simultaneously achieved by sacrificing around 33% of its dynamic range compared to the ordinary differential pair transconductor. A 2nd-order G_m-C low-pass as an application of the proposed transconductor has been designed and simulated using 0.18-µm AMS technology. Compared to existing designs, post-layout simulation results show that, with a smaller active area (including bias circuitry, transconductors and capacitors), this design provides greater dynamic range, wider tuning range and lower power consumption.**

I. Introduction

Influenced by the requirements for very small size and very low-power consumption of portable and implantable medical devices, sub-threshold G_m-C filters have been widely used for filtering low frequency biomedical signals [1]. Conducting a very low-current in sub-threshold operation indeed results in a very low transconductance of a single transistor that helps in designing a very low-cutoff frequency G_m-C filter. Unfortunately, generating very low bias currents on chip cannot be achieved reliably because of poor matching of transistors operating in weak inversion [2]. This gives a lower limit of the reliable cutoff frequency achieved from conventional techniques and leads to the need for the transconductance reduction technique for the design of a G_m-C filter with a cutoff frequency below that limit [3] (note that generating a reliable bias circuit is also a topic of interest nowadays [4]).

In this paper, we investigate transconductance reduction techniques and we propose a more reliable realization method. The resulting circuit can be formed by compact identical circuit cells and provides both linear range expansion and transconductance reduction which makes it practically suitable for very low-frequency, large dynamic range, low-power, tunable G_m-C filters. In Sec. II, a review of existing techniques for transconductance reduction is given. The proposed technique with relevant performance analyses will be presented in Sec. III. An application to the design of linear tunable cutoff frequency low-pass filter (LPF) is shown in Sec. IV. Sec. V provides simulation results and a performance comparison between the proposed circuit and a previously reported design. The conclusion is finally given in the last section.

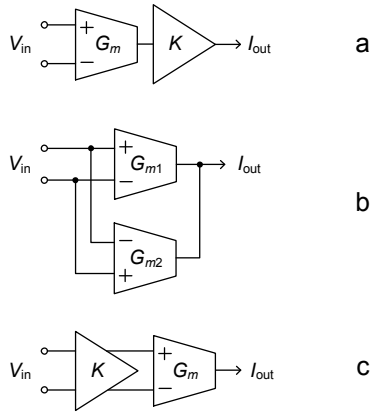

Figure 1. Tranconductance reduction techniques.
(a) Current attenuation (b) Current cancellation (c) Voltage attenuation

II. Review of Transconductance Reduction Techniques

In this work, we classify the transconductance reduction technique into three categories: 1) *current attenuation*: Fig. 1a, 2) *current cancellation*: Fig. 1b and 3) *voltage attenuation*: Fig. 1c. In most of the cases, each G_m cell is built from an ordinary differential pair circuit such as the one shown in Fig. 2, For sub-threshold operation (weak inversion saturation), the transconductor of Fig. 2 provides a nonlinear transfer according to

$$I_{\text{out}} = I_B \tanh\left(\frac{V_{i+} - V_{i-}}{2nU_T}\right), \tag{1}$$

where n and U_T are the sub-threshold slope factor and the thermal voltage, respectively. This circuit cell is considered the main source of distortion for the following reasons.

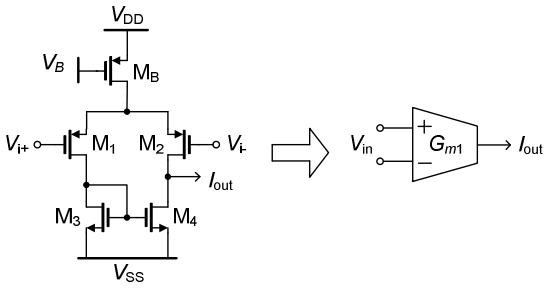

Figure 2. Single-ended nonlinear transconductor.

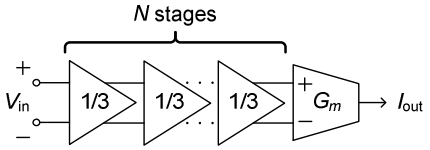

Figure 3. Low-G_m transconductor using voltage attenuation.

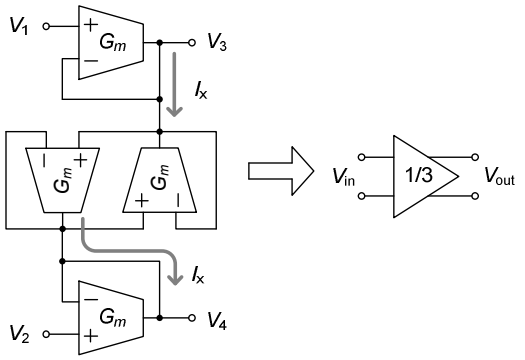

Figure 4. Nonlinear G_m network implementing a linear voltage attenuator.

In the case of Fig. 1a, input voltage V_{in} is applied to the G_m cell and will be subsequently converted into a current before being attenuated by current attenuator K which can be formed by current mirror circuits [5]. Harmonics components are mainly generated from the G_m cell and since the K provides linear current scaling, the ratios of fundamental and harmonic components are maintained. Hence, in this case, the overall transconductance is reduced successfully to $G_{mt} = K \cdot G_m$ but the harmonic distortion is unfortunately preserved. Moreover, additional noise contributed by K is unavoidable, which degrades the circuit dynamic range even more.

The current cancellation shown in Fig. 1b provides the transconductance reduction by creating an extra current generated by G_{m2} flowing in the opposite direction to become subtracted from the main output current of G_{m1}. Effectively, the overall transconductance is reduced to $G_{mt} = G_{m1} - G_{m2}$, which theoretically can be made extremely small. In practice, the subtraction mechanism is limited by transistor mismatch and again, the distortion remains [6] and more noise is added.

To extend the input linear range of the transconductor as well as its transconductance reduction, the voltage attenuation technique shown in Fig. 1c is employed. Voltage attenuator K can be made linear by a capacitive dividing network [7] [8]. The obtained overall transconductance in this case equals $K \cdot G_m$ as was also the case when employing current attenuation but now the linear range is wider without additional noise contribution. However, DC offset and operating point voltages are needed to be minimized and defined, respectively. For these reasons, a double-poly process [7] and additional circuit element [8] are required. Recently, a linear attenuator using active circuitry has been proposed [9], by which the problems mentioned above have been solved but the attenuation circuit produces noise and relies on an accurate matching between current source and current sink circuits which cannot be accomplished readily in weak inversion.

In the next section, elaborating further on the voltage attenuation method, we present an improved version of the transconductor in [9], which relaxes the design of bias circuits involved and provides modularity to the overall design.

III. Proposed Wide-Linear Range, Low-G_M Transconductor

A. Concept

Fig. 3 shows a macro-model of the proposed transconductor. It is composed of an N-stage cascade connection of one-third linear attenuators and an ordinary nonlinear subthreshold transconductor, G_m (Fig. 2). By doing so, input voltage V_{in} will be attenuated by a factor of 3^N appearing at the input port of G_m. Since the amplitude of the voltage appearing at the input port of the nonlinear element becomes smaller, effectively this mechanism leads to a linear input range extension as well as a transconductance reduction by a factor of 3^N.

The linear attenuation can be realized by the network shown in Fig. 4. Assuming the voltage to current relationship of each transconductor is a strictly monotonic increasing nonlinear odd-symmetry function, i.e.

$$I_{\text{out}} = f\left(V_+ - V_-\right) = -f\left(V_- - V_+\right), \tag{2}$$

we have

$$I_x = f\left(V_1 - V_3\right) = f\left(V_3 - V_4\right) = f\left(V_4 - V_2\right). \tag{3}$$

A linear relationship between input and output voltages is thus found

$$V_{\text{out}} = V_3 - V_4 = \frac{V_1 - V_2}{3} = \frac{V_{\text{in}}}{3}. \tag{4}$$

This linear attenuation can be built from a network of any nonlinear transconductors that comply with (2). In practice, both hyperbolic sine and hyperbolic tangent sub-threshold tranconductors are applicable to this concept.

B. Noise and Dynamic Range

Although the input linear range is enlarged, unfortunately this also holds for the input referred noise. Considering the

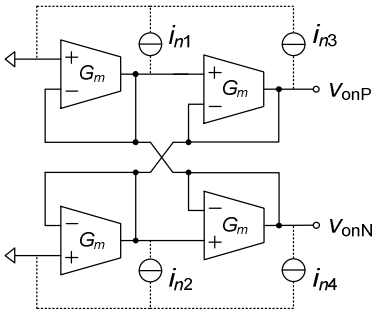

Figure 5. Linear attenuator with noise sources.

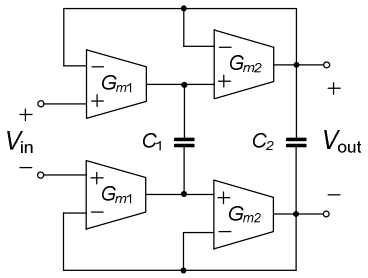

Figure 6. psuedo differential LPF.

attenuator circuit shown in Fig. 5 and that each transconductor has its own output noise current with a power spectral density of $S_{in}(f)$, the power spectral density of the output noise voltage can be found to be

$$S_{vno}(f) = S_{vonP}(f) + S_{vonN}(f) = \frac{S_{in1}(f) + S_{in2}(f) + S_{in3}(f) + S_{in4}(f)}{3^2 G_m^2} = \frac{4}{9}\frac{S_{in}(f)}{G_m^2}, \quad (5)$$

and for N cascade stages, we have

$$S_{vtotal}(f) = \sum_{j=0}^{N-1} \frac{S_{vno}(f)}{3^{2j}}. \quad (6)$$

In contrast to the case of a cascade of voltage amplifiers, the majority of noise in this case is generated from the last stage instead of the first one. The noise in (6) appears at the input of the main transconductor and will finally be converted into an output noise current in addition to the noise generated from the main transconductor itself. Then the output noise current spectral density becomes

$$S_{inout}(f) = S_{in}(f) + \frac{4}{9}\left(S_{in}(f) + \frac{S_{in}(f)}{9} + \frac{S_{in}(f)}{81} + \cdots \right) \cong 1.5 S_{in}(f). \quad (7)$$

This leads to slightly more than 33% dynamic range (DR) degradation compared to the basic transconductor,

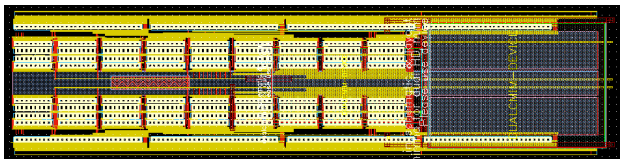

Figure 7. Chip layout of the 2nd-order LPF.

$$\mathrm{DR}_{\mathrm{proposed}} \cong \frac{\mathrm{DR}_{\mathrm{basic}}}{1.5}. \quad (8)$$

C. Current Consumption and Circuit Complexity

The transconductance reduction in this case is obtained not only by sacrificing the DR but also by adding more power consumption and more circuit complexity. Since each transconductor operates in class A and consumes a bias current I_B, a $(4N+1)I_B$ total current consumption is found.

For complexity, we count the circuit elements G_m and obtain a total number of elements of $(4N+1)$. Apparently, both the current and complexity increase by the same factor of $4N+1$ to obtain $K = 3^N$ transconductance reduction.

Now it is clear that to save the chip area occupied by on chip capacitors using this technique, we need to sacrifice DR and power. Moreover, if N is large enough the area occupied by the transconductor can be dominant. For this reason, in practice, the minimum N can be determined by the minimum current that can be reproduced reliably on chip and the area consumes by the capacitors.

IV. Filter Design and Post-Layout Simulation

A. Butterworth 2nd-order LPF

In this work, a pseudo differential 2nd-order LPF that provides a transfer function of

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{G_{m1}G_{m2}}{C_1 C_2} \cdot \frac{1}{s^2 + s\frac{G_{m2}}{C_2} + \frac{G_{m1}G_{m2}}{C_1 C_2}}, \quad (9)$$

shown in Fig. 6 is employed for two reasons; 1) a differential structure widens the signal swing and 2) unity gain feedback maintains good linearity in the pass-band [10] [11].

Setting $G_{m1} = G_{m2} = G_m$, which can be done by biasing them with the same bias current I_B, we then have a cutoff frequency $\omega_H = G_m / \sqrt{C_1 C_2}$ and quality factor $Q = \sqrt{C_1 / C_2}$. Targeting a frequency range up to 100 Hz, a total on chip capacitor of 78 pF can be used ($C_1 = 2C_2 = 52$ pF) and the entire filter circuit is fully integratable.

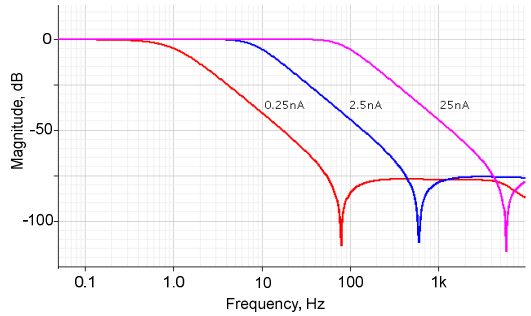

Figure 8. Frequency response of the 2nd-order LPF.

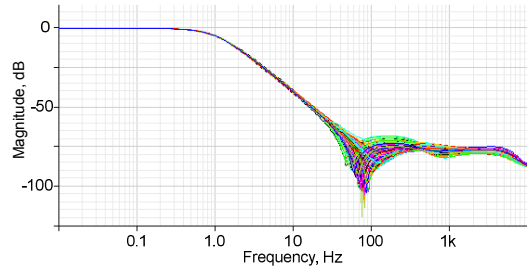

Figure 9. Effect of mismatch on the magnitude response of the filter.

TABLE I. PERFORMANCE SUMMARY

I_B (nA)	f_{-3dB} (Hz)	*IRN (μV_{rms})	V_p@1%THD, (f_{-3dB})	DR (dB)
0.25	0.73	177.4	0.54V	66.7
2.5	7.8	243.6	0.75V	66.8
25	76	266.2	0.61V	64.2

* Integrated from 10 mHz to 10 kHz.

TABLE II. PERFORMANCE COMPARISON

Ref.	Tech. (µm)	Area $(mm)^2$	Freq. (Hz)	Total Cap.	DR (dB)	V_{DD} (V)	*P_{max} (W)
†[11]	0.35	0.336	1.5-15	105pF	60	3.3	>2µ
This work	0.18	0.034	0.73-76	78 pF	64	1	0.9µ

*Tested at the highest frequency, †measured results

B. Post-Layout Simulation

The LPF has been design using AMS 0.18-µm CMOS technology. In this process, dual MIM capacitors are available and they are employed in this design. The proposed tranconductors with $N = 2$ (attenuating factor of 9) are chosen. The layout of the LPF including its bias circuit is illustrated in Fig. 7. It occupies an area of 97 µm×400 µm.

Supply voltage V_{DD} and the common mode level are set to 1 V and 0.5 V, respectively. The total current consumption depends on the filter cutoff frequencies and can be found as $I_{tot} = 4\times(4N+1)I_B = 36I_B$. Fig. 8 shows the simulated magnitude response of the LPF for different I_B s adjusted from 0.25 nA to 25 nA. This results in a power consumption of 9 nW, 90 nW and 900 nW, respectively.

Using the same condition of Fig. 8, other performances have been tested and summarized in Table I. An almost linear adjustability of the cutoff frequency, f_{-3dB}, is obtained. A sinusoidal input signal was applied for linearity testing at f_{-3dB} in each case. Calculated from the input amplitudes (V_p) that correspond to 1% total harmonic distortion (THD) and from the input referred noise (IRN), DR of higher than 64 dB is achieved for all cases.

Fig. 9 shows a 100 runs Monte-Carlo simulation of the frequency response to illustrate the robustness of the circuit in case of transistor mismatch for I_B = 0.25 nA. The pass-band gain and cutoff frequency are quite robust as they are regulated by the high loop gain of the filter in this frequency range. As the loop gain decreases at the frequency beyond f_{-3dB}, the magnitude responses start spreading.

Table II shows a performance comparison between the proposed filter and the design of [11]. It can be seen that the proposed filter supersedes the filter of [11] in terms of supply voltage, tuning range, DR, area and power consumption.

V. CONCLUSIONS

A transconductance reduction technique and a design of a second order LPF have been presented. Post-layout simulations provide results that are consistent with the theory. In comparison to a previously reported design, this filter provides greater tuning range and DR, occupies less chip area and consumes less power. For this reason, this technique is suitable for fully integrated very low frequency filters.

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REFERENCES

[1] Y. Li, C. C. Y. Poon, and Y. T. Zhang, "Analog integrated circuits design for processing physiological signals," *IEEE Reviews in Biomed. Eng.*, vol.3, no., pp.93-105, 2010.

[2] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp.1353 - 1363 , 2003.

[3] I. Pachnis, A. Demosthenous, and N. Donaldson, "Comparison of transconductance reduction techniques for the design of a very large time-constant CMOS integrator," *Proc. IEEE ICECS,* pp. 37-40, 2006.

[4] X. Zhang and A. B. Apsel "A low power, process-and-temperature-compensated ring oscillator with addition-based current source", *IEEE Trans. Circuits Syst. I, Reg. Papers*, no. 7, pp. 868-878, 2011.

[5] M. Steyaert, P. Kinget, and W. C. Sansen, "Full integration of extremely large time constant in CMOS," *IEE Electron. Lett.*, vol 27, no. 10, pp. 790-791, 1991.

[6] P. Garde, "Transconductance cancellation for operational amplifier," *IEEE J. Solid-State Circuits*, ol. 12, pp. 310-311, June 1977.

[7] A. Mourabit, G. Lu and P. Pittet, "Wide-linear-range subthreshold OTA for low-power, low-voltage, and low-frequency applications", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, p.1481 , 2005.

[8] C. Salthouse and R. Sarpeshkar, "A practical micropower programmable bandpass filter for use in bionic ears," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 63-70, 2003.

[9] C. Sawigun, D. Pal, and A. Demosthenous, "A wide-input linear range sub-threshold transconductor for sub-Hz filtering," *Proc. IEEE ISCAS*, pp.1567-1570, 2010.

[10] A. Tajalli and Y. Leblebici, "Low-power and widely tunable linearized biquadratic low-pass transconductor-*C* filter," *IEEE Tran. on Circuits Syts. II, Express Briefs*, vol. 58, no. 3, pp. 159-163, March, 2011.

[11] P. Bruschi, N. Nizza, F. Pieri, M. Schipani, and D. Cardisciani, "A Fully integrated single ended 1.5-15-Hz lowpass filter with linear tunning law," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1522–1528, 2007.