# Instantaneously companding baseband SC low-pass filter and ADC for 802.11a/g WLAN receiver

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***Abstract*—To handle the 12dB peak-to-average-power ratio (PAPR) of OFDM signals in a 802.11a/g WLAN receiver baseband, an instantaneously companding system consisting of a $5^{th}$-order low pass SC filter and a 10-bit pipeline ADC is presented. The filter cut-off and clock frequencies are 10MHz and 100MHz respectively and the ADC sampling frequency is 25MS/s. The filter provides the compressed output directly to the ADC and the signal expansion is done in the digital domain, which eliminates the need of an analog expansion amplifier. For a 12dB increase in dynamic range, it is estimated that the filter consumes 3.7 times less power than a conventional filter while the dynamic range required from the ADC is reduced by 12dB due to companding by a factor of 4. The filter and the ADC are designed to be implemented in a 1.2V, IBM 0.13$\mu$m CMOS process and the total power consumption is 75mW.**

## I. Introduction

In wireless local-area network (WLAN) receivers, the baseband typically consists of analog channel-select filters, analog-to-digital converters (ADC), the DSP unit and automatic gain control (AGC) circuits. The channel-select filter is used to reject out of band signals before analog-to-digital (A/D) conversion. This relaxes the dynamic range (and therefore resolution) and speed requirements of the A/D converter (ADC), which would otherwise have to oversample the entire input signal containing large interferers. The AGC is an essential function in wireless receivers and is commonly used to set the receiver internal gains during the preamble/midamble of the data frame so that the signal level in the receiver is optimal to provide the minimum SNDR required by the specifications.

However, the IEEE 802.11a/g WLAN receiver [1] presents two limitations to the use of AGC. First, the standard puts a stringent AGC settling time requirement ($<5.6\mu$s). Since the filter needs extra settling time, the AGC is inserted between the filter and the ADC in the receiver baseband. Secondly, since the AGC operation is based on the measure of average signal power, the high peak-to-average-power ratio (PAPR) of OFDM signals requires headroom of at least 12dB in the dynamic range of the filter and the ADC. To handle the PAPR in the receiver baseband, a companding system consisting of a $5^{th}$-order Chebychev, ladder type, SC low-pass filter and a 9.2 ENOB pipeline ADC is described in this paper which provides gain switching based on the instantaneous value of the signal and thus reduces power dissipation for a given dynamic range.

Companding compresses the high dynamic range input signal, processes it in a lower dynamic range system and then expands the signal at the output [2]. A companding system consists of a gain element at the input to compress the signal, a gain element at the output to expand the signal and, finally, a mechanism to update the state variables of the system [2]. In [3], the companding switched-capacitor (SC) integrator was introduced, which can be used to implement a companding SC filter. It is estimated that companding by a factor of 4 would save 12dB in dynamic range of the filter resulting in a 4 times improvement in power consumption as compared to a conventional filter. In [4] [5], system level methodologies were presented to design a companding SC filter for a WLAN receiver. Since a companding SC filter needs an expansion stage to recover the signal at the output, the analog expansion amplifier consumes extra power, which reduces the power savings achieved by companding. Since the filter is followed by an ADC, this expansion can be moved to the digital domain, thereby removing the need for the expansion amplifier and saving power. Also, it further reduces the dynamic range requirements of the ADC by 12dB, leading to additional power savings.

This paper is organized as follows. Section II describes the WLAN receiver system and its link budget. Section III explains the design of the last stage of the companding filter and the interfacing between the filter and the ADC. Section IV describes the circuit design of the filter and the ADC. Section V presents simulation results and finally, section VI gives the conclusions.

## II. WLAN Analog Baseband Signal Chain

A direct conversion architecture is assumed for the WLAN receiver. As shown in Fig. 1, the receiver consists of a bandpass filter, low-noise amplifier (LNA), mixers, gain amplifiers, low-pass channel-select filters and ADCs followed by the DSP unit. The RF portions of the receiver are assumed to have the following gains: $-3$dB for the (off-chip) bandpass filter, 0 or $+20$dB (selectable) for the LNA and $+10$dB for the mixers. The entire receiver has a noise figure of 9dB. After downconversion, an amplifier provides a gain of 10dB and is followed by a first order anti-aliasing filter (AAF). A $5^{th}$ order, Chebyshev, ladder type, companding SC low pass filter [4] [5] with a cut-off frequency of 10MHz and a sampling frequency of 100MHz is used for channel selection. The low pass filter has a gain of 12dB in its first stage and there is no expansion stage at the output. The filter is followed by a SC amplifier, which subsamples the input and supplies the output at 25MS/s to the following ADC. The SC amplifier is also used for gain

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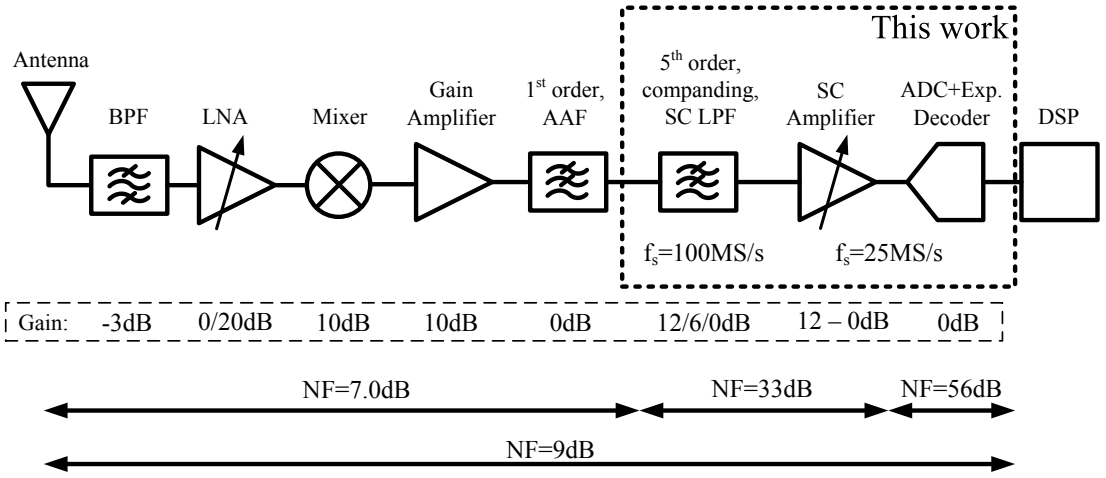


Fig. 1. WLAN receiver components and link budget

control and has a switchable gain of 12dB to 0dB in steps of 3dB. Finally, a 9.2-bit ENOB, 25MS/s, pipeline ADC is used with a decoder at the output of the ADC to expand the signal in the digital domain. The noise figure of the low-pass filter and the SC amplifier is 33dB and that of the ADC is 56dB.

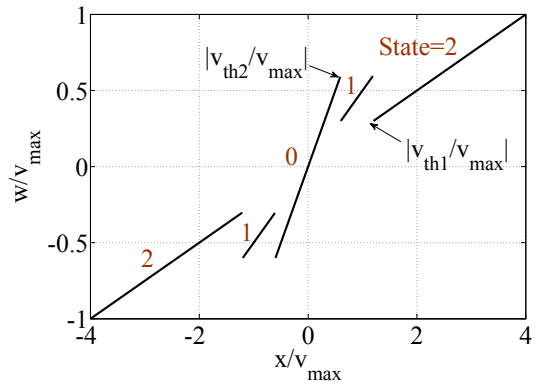


Fig. 2. Companding gain function.

## III. Companding Filter and ADC System Implementation

The companding filter is implemented using a piecewise-constant gain function $g$ and SC integrators as shown in Fig. 2 and Fig. 3(a), respectively. The compression and expansion is done in factors of 2 or 4 to make the implementation easier. Fig. 3(a) shows the companding SC discrete integrator [4] [5] modified for the last stage of the filter. The two non-overlapping clock phases are $\phi 1$ (sampling/hold phase) and $\phi 2$ (integration phase). Based on the OTA's output at the end of $\phi 2$, the sampling capacitor banks at the input are used to switch the gain by a factor of 2 in the next $\phi 2$. The charge (memory) on the integration capacitor $C_I$ is then updated. When the input gain needs to be decreased by 2, one half of the integration capacitor of value $C_I$ is disconnected and discharged to ground whereas another discharged capacitor of value $C_I/2$ is connected to the other half of the integration capacitor halving the output voltage during $\phi 1$. Another capacitor ($C_{Inc}$) of same value as $C_I$ is charged to the output voltage during $\phi 1$. When the input gain needs to be increased by 2, $C_{Inc}$ is discharged to the input of the OTA during $\phi 2$ and thus it doubles the output voltage. For each stage, the companding algorithm works on a finite-state machine (FSM) run by a controller which uses comparators and digital circuits to generate digital signals $S_{i1}$, $S_{i2}$, $S_{o1}$, $S_{o2}$, $Inc$ and $Dec$ in Fig. 3(a). Digital signals $S_{i1}$ and $S_{i2}$ are used for gain switching at the input whereas digital signals $Inc$ and $Dec$ are used to update the memory of the integrator. Digital signals $S_{o1}$ and $S_{o2}$ carry the information of expansion and they are transferred to the digital domain with an appropriate delay. These compression, memory update and digital expansion operations are synchronized due to the discrete time operation. Fig. 3(b) shows the timing diagram of various signals w.r.t. the clock signals.

The purpose of the SC amplifier is twofold. First, it sub-samples the output of the filter, which may or may not be in compressed form, at 25MS/s. In order for it not to load the last stage of the filter during the integration phase, the sampling phase of the SC amplifier has a 12% duty-cycle while the hold phase has a duty-cycle close to 50%. The clock phases are illustrated in Fig. 3(b). The sampling phase of the SC amplifier is synchronized with $\phi 1$ because in $\phi 1$ the compression takes place and thus the input to the ADC never exceeds the full-scale input voltage $V_{FS}$ for which the ADC is designed. The second purpose of the SC amplifier is to provide gain control by switching its gain from 12dB to 0dB in steps of 3dB depending on the average RMS of the input signal power. This is achieved by changing the value of sampling capacitor by switching between parallel capacitors.

The SC amplifier is followed by a 9.2 ENOB, 25MS/s, pipeline ADC with a $V_{FS}$ of 1.4V. Since the output of the SC amplifier is discrete-time, the ADC does not need a sample and hold stage. The ADC has a digital expanding decoder at its output to do the expansion. After expansion, the $V_{FS}$ becomes 5.6V. The expansion is done in factors of 2 (see Fig. 2), which

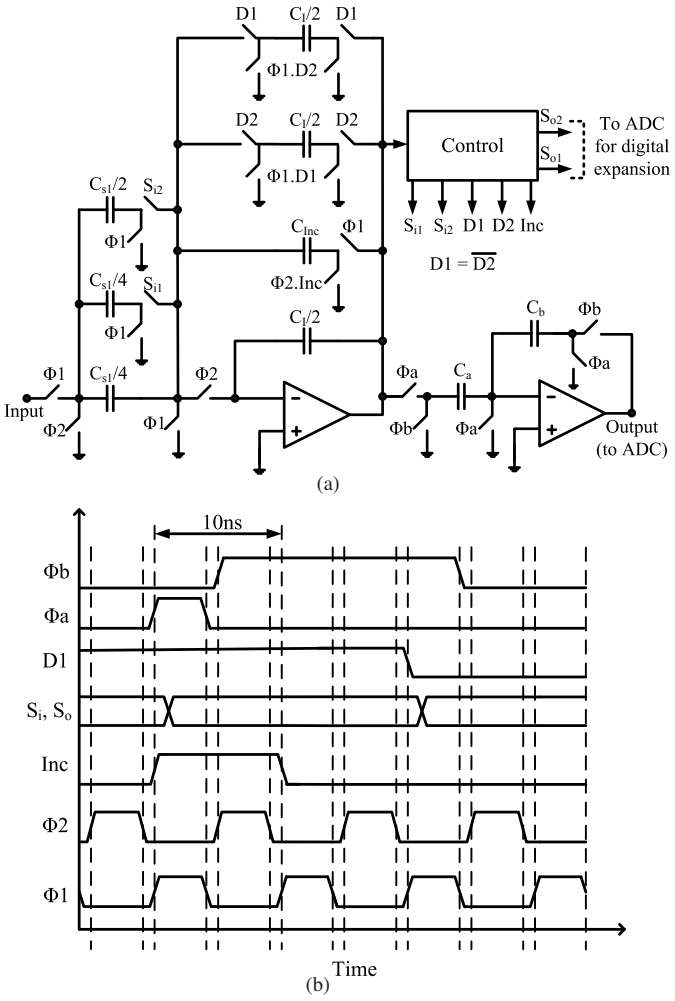


Fig. 3. (a) Interfacing between the last stage of the filter and the ADC, (b) Timing diagram for the control signals.

is achieved by shifting 1 bit and 2 bits to the left in the output 10-bit codeword of the ADC corresponding to the expansion by factors of 2 and 4, respectively. This operation results in a 12-bit output of which 2 bits are defined as companding bits. Adding 2 MSBs of binary value 0 to the original 10-bit codeword of the ADC creates a DC offset in the signal. When the operation of expansion is carried out by shifting the bits to the left, this DC offset becomes companding state dependent and has to be eliminated in the final 12-bit signal. Thus, companding state dependent DC offset cancellation bits are added to the MSBs of the 12-bit codeword after expansion as shown in Table I.

## IV. Circuit Implementation

The baseband system is designed to be implemented in a differential structure in IBM 1.2V, 0.13$\mu$m CMOS technology. The filter is implemented using 2-stage Miller compensated OTAs with a low-frequency loop gain of 60dB, closed-loop unity gain-bandwidth (UGBW) of 300MHz and slew rate of 300V/$\mu$s. The switches in the filter are implemented as CMOS transmission gates using voltage boosted clocks.

TABLE I
Summary of expanding decoder algorithm

| State ($S_{o1}, S_{o2}$) | 0 (0,0) | 1 (0,1) | 2 (1,1) |
|---|---|---|---|
| No. of bits shifted to the left | 0 | 1 | 2 |
| MSB offset compensation | 011 (2.1V) | 010 (1.4V) | 000 (0V) |

The ADC is implemented using a 1.5-bit residue stage [6] configuration, which consists of a 2-bit sub-ADC, a digital-to-analog converter (DAC) for reference voltage selection and a multiplying DAC (MDAC). Bootstrapped switches [6] and bottom-plate sampling are used to reduce distortion. The MDAC is implemented using a 2-stage Miller compensated OTA. The first stage is implemented as a folded-cascode with gain boosting and the second stage is a class AB amplifier. 30% power is saved by switching off the current in the second stage of the OTA during the sampling phase when the OTA is not being used. The MDAC has a loop gain of 88dB and achieves 16-bit linearity for a $1.4V_{pp-diff}$ input signal. The simulated closed-loop UGBW of the MDAC amplifier is 300MHz. This allows for settling within 12-bit accuracy at 25MS/s.

Scaling down the size of capacitors and OTA along the pipeline chain of the ADC is used to reduce its power consumption. The MDAC stages in the ADC are divided into three groups as shown in Fig. 4. Two scaling factors $k_1$ and $k_2$ are defined as the ratio of the scaling of the Group 2 and Group 3, respectively, with respect to Group 1.

The input referred thermal noise of the ADC is proportional to $\sum_{i=0}^{8} \frac{\beta_i}{C_{ci}A_i^2}$[7], where $\beta_i$ is the feedback factor and $C_{ci}$ is the compensation capacitor of the $i^{th}$ stage and $A_i$ the accumulated gain of the ADC upto the $i^{th}$ stage. The settling time for the $i^{th}$ stage of the ADC is given by

$$t_{si} = (N_i)\ln 2 \times \tau_i \tag{1}$$

where $N_i$ and and $\tau_i$ are settling accuracy and time constant of the $i^{th}$ stage. $\tau_i$ is given by $C_{ci}/\beta_i g_{mi}$, where $g_{mi}$ is the input transconductance of the OTA of the $i^{th}$ stage. From Eq. 1, it follows that the current consumption in the $i^{th}$ stage is proportional to $C_{ci}/\beta_i N_i$. So, we define a Figure of Merit (FOM), which gives power consumption a 30% larger weightage than the noise power as follows:

$$\text{FOM} = \frac{7}{3\overline{P_{n,in}} + 4\overline{P_{total}}} \tag{2}$$

where $\overline{P_{n,in}}$ is the normalized input referred thermal noise power and $\overline{P_{total}}$ is the normalized overall power consumption. Item coefficients can be set dependent on different applications. Fig. 5 shows the relationship between FOM and factors $k_1$ and $k_2$. From Fig. 5, $k_1 = 0.5$ and $k_2 = 0.2$ are chosen,

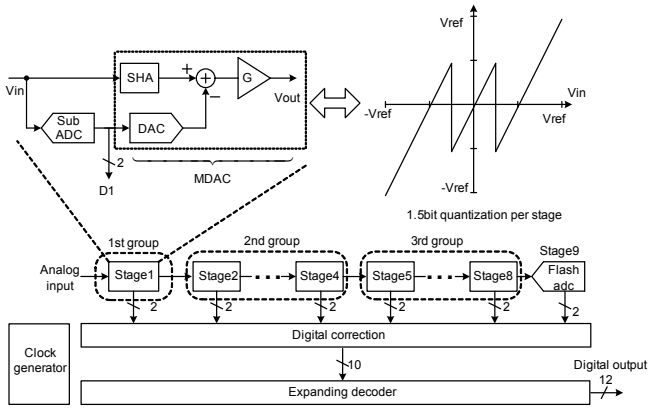


Fig. 4. Expanding ADC including pipeline ADC core and back-end expanding decoder

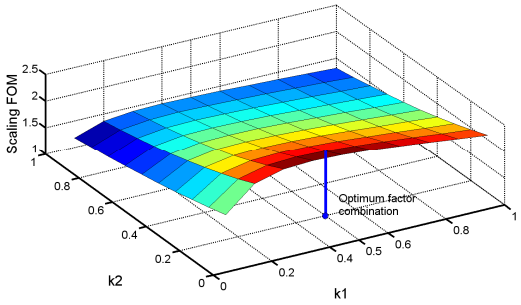


Fig. 5. Stage downscaling FOM dependent on group scaling factor $k_1$ and $k_2$

finally resulting in a large FOM and easy design configuration.

Since a companding system is an internally nonlinear system, its performance is affected by any spurious signals arising from within the system. In our case, the OTAs DC offset gives rise to distortion and should be eliminated. In the companding SC filter, the DC offset of the OTAs is eliminated in both phases. We use a continuous-time auto-zeroed (AZ) amplifier using a feedforward technique [8], which results in a residual offset of 500$\mu$V under worst case process and mismatch conditions. Correlated double sampling [8] is also used to make the integration phase offset free. The AZ amplifier consumes 40$\mu$W from 1.2V. The DC offset arising from the SC amplifier and the ADC should be removed by doing ADC calibration before doing the digital expansion of the signal and is not dealt with in this paper. The total power consumed by filter is 47mW and by the ADC including the SC amplifier is 28mW.

## V. Simulation Results

Fig. 6 shows the plots of signal to noise-plus-distortion ratio (SNDR) vs. the desired input signal power in dBm for a single-tone (at 2.34MHz) test in the presence of interferers for both cases, with and without companding. The interferers at various stages of the filter are low enough not to trigger companding when the desired signal is weak. The SC amplifier and the pipeline ADC achieve 60.3dB SNDR, 78dB SFDR at the

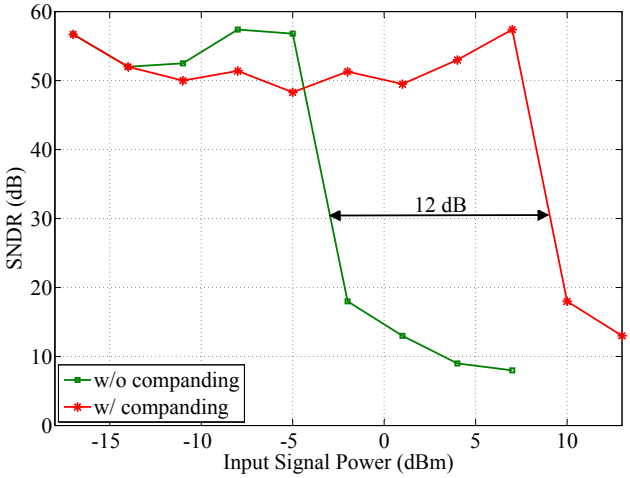


Fig. 6. Signal to noise-plus-distortion ratio (SNDR) from a single-tone (2.34MHz) test without companding (green) and with companding (red) vs. input signal power in dBm.

Nyquist frequency (12.5MHz) and at full-scale input amplitude (1.4V). Therefore, the SNDR of 50dB is mainly limited by the filter. The plot in Fig. 6 shows a 12dB improvement in the dynamic range due to companding by a factor of 4.

## VI. Conclusion

An instantaneously companding system consisting of a 5$^{\text{th}}$-order low pass SC filter and a 10-bit pipeline ADC is presented to handle PAPR in a 802.11a/g WLAN receiver baseband section. For a 12dB increase in dynamic range, it is estimated that the filter consumes 3.7 times less power than a conventional filter while the dynamic range required from the ADC is reduced by 12dB due to companding by a factor of 4. The total power consumption is 75mW and the filter and the ADC achieve an SNDR of 50dB in the higher end of the dynamic range when companding takes place.

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