A 24nW, 0.65-V, 74-dB SNDR, 83-dB DR, Class-AB Current-Mode Sample and Hold Circuit

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***Abstract*— An ultra low-power, high linearity, wide swing, current sample-and-hold circuit is presented. The proposed circuit employs negative feedback, provides very low switching error and allows for class-AB operation. Sub-threshold CMOS devices are employed to realize all circuit building blocks which leads to ultra low power consumption and large dynamic range. Operating from a 0.65V supply, simulation results using TSMC 0.13µm CMOS model parameters confirm that the proposed circuit consumes 24nW static power and for 20kS/s sampling rate, a dynamic range and a signal to noise plus distortion ratio larger than 70dB are achieved.**

INTRODUCTION

Processing electrical signals in the voltage domain using CMOS circuits is encountering the problem of signal swing reduction. This results from CMOS process scaling that forces the supply voltage, and thereby the maximum signal swing, to go down [1]. To recover the signal dynamic range, current mode signal processing has become attractive since the nonlinear behavior of the devices, i.e. the square and exponential laws for strong and weak inversion behaviors, respectively, provide a compressive voltage swing. A wide range of current signal swings can thus obtained from a low supply voltage [2].

In the area of biomedical electronics that focuses on the design of implantable devices, minimizing power and area consumption are major requirements. To operate circuits at very low current consumption and limited supply voltage, the CMOS devices will be forced into their weak inversion region, which creates a design difficulty in terms of noise and mismatch [3]. Therefore, a suitable circuit technique that can satisfy the requirements and overcome the design difficulty is needed.

In this paper, we consider an analog sampled-data technique called 'switched current (SI)' which provides low sensitivity to device mismatch and does not require any linear capacitor [2]. We can thus obtain a small silicon area. Moreover, we also focus on how to design the circuit to consume very low current, provide high accuracy and large signal to noise ratio (SNR). Hence in Sec. II, the SI memory cell is re-examined from the feedback point of view. By doing so, the implicit feedback mechanism of the memory cell is revealed. As a consequence, based on a comprehensive understanding of the negative feedback mechanism, the design of a high performance ultra low power class-AB fully differential current sample and hold (CSH) circuit is presented in Sec. III. The entire circuit comprises two transconductance stages in order to enhance the circuit's loop gain. The first stage is realized using a simple class-A differential pair to perform high gain voltage amplification. For the second stage, a class-AB sinh transconductor is employed to handle a large input/output signal swing. Based on this closed-loop differential structure, very low distortion, very large signal swing, and ultra low power consumption are obtained. In Sec. IV, the performance verification of the design by simulation results using Cadence RF Spectre and 0.13µm CMOS model parameters is presented. From a 0.65V supply, the CSH circuit consumes 24nW static power and provides a maximum signal to noise plus distortion ratio (SNDR) of 74.3dB for a 40nA, 1.25kHz, sinusoidal input current sampled at a 20kS/s clock rate. Finally, a conclusion will be given in the last section.

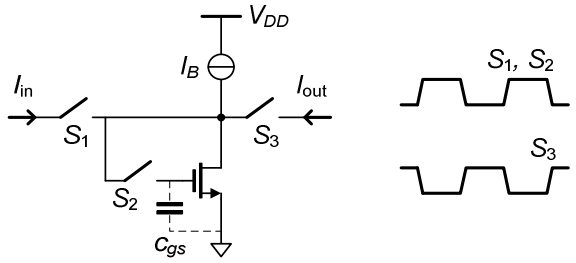

Figure 1. 2nd generation SI memory cell

II. REVIEW OF FEEDBACK MECHANISM AND PERFORMANCE ENHANCEMENT OF A CURRENT SAMPLE AND HOLD CIRCUIT

Fig. 1 shows a 2nd generation SI memory cell which is the most compact current sample and hold (CSH) circuit [2]. It comprises one transistor, biased by constant current I_B, and switches S_1-S_3, controlled by two non-overlapping clock phases.

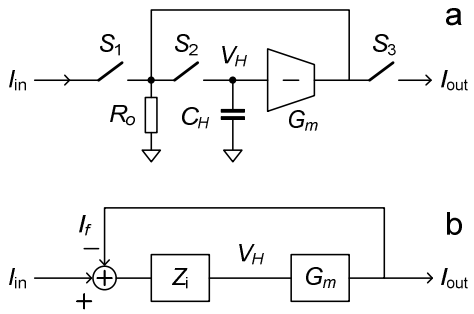

Figure 2. 2nd generation SI memory cell a) small signal equivalent circuit b) feedback block diagram

Including channel length modulation, the circuit in Fig. 1 can be modeled as shown in Fig. 2a, where R_o and G_m represent the output resistance and transconductance gain of the transistor. During the sampling phase (S_1 and S_2 are closed and S_3 is opened), the feedback mechanism of the circuit can be described using the block diagram in Fig. 2b. As one can see, the error current resulting from I_{in}-I_f, (where I_{in} and I_f represent the input and feedback currents, respectively) will flow into Z_i, thereby creating voltage V_H which is the input voltage of transconductor G_m. Finally, V_H will be converted into I_f by G_m again. From the block diagram, the loop gain (LG) of the system can be obviously found to be $G_m Z_i = G_m R_o / (1 + sC_H R_o)$. It is widely known that a large LG leads to high accuracy and low sensitivity to disturbances. To enhance the LG of the CSH circuit, two different approaches have been developed including increasing R_o by exploiting cascoded transistors [2] and increasing G_m by cascading G_m stages [4-8].

When the charge injection effect of MOS switches is considered, only the latter approach is promising since the former approach does not help fixing the voltage swing at the sampling node. This enhancement technique can be described through the circuit in Fig. 3. In Fig. 3a, a voltage amplifier A_i is inserted in front of the G_m. This results in a higher effective tranconductance $G_{mt} = A_v G_m$, which can be made very large. By doing so, the error current is forced to be very small by the very large LG resulting in a very small variation of V_H. Therefore the signal-dependent charge injection can be neglected. To realize voltage amplifier A_i, another G_m stage is used and there will be two high impedance nodes, created by parasitic resistances and capacitances in the negative feedback loop, which may lead to stability problems. Pole splitting can be applied to stabilize the system by changing the location of the holding capacitor C_H (which is used as a miller capacitor in the sampling phase) and the polarities of amplifiers A_i and G_m as shown in Fig. 3b [5, 6].

To get rid of the charge injection error, a fully differential structure, shown in Fig. 4, is required. In this case the signal–independent charge injection error can be considered a common-mode error and will be cancelled out. As a result, a high linearity CSH circuit is obtained [4, 7, 8].

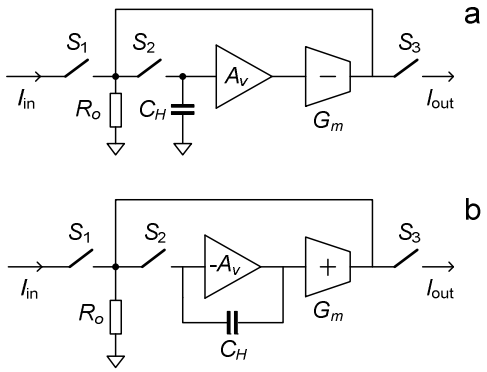

Figure 3. CSH circuit with LG enhancement with a) grounded holding capacitor and b) miller holding capacitor

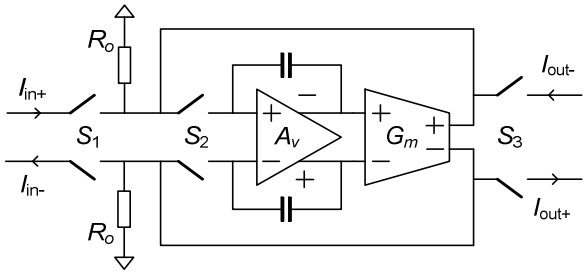

Figure 4. Fully differential CSH circuit

III. Proposed Class-AB Sample and Hold Circuit

A. Circuit Description

To serve the requirements for ultra low-power biomedical applications, the proposed CSH circuit is designed using weak inversion MOSFETs. Considering the circuit in Fig. 4 in practical detail, a macro-model of the circuit including parasitic elements is shown in Fig. 5. To stabilize the internal voltage swings to a certain common-mode voltage level, common-mode feedback (CMFB) circuits are required. Very high resistors R_1 and R_2 represent the output resistances of transconductors G_{m2} and G_{m1}, respectively. C_1 and C_2 are parasitic capacitances of G_{m1} and G_{m2}, respectively. In the sampling phase, switches S_1 and S_2 are closed and S_3 are opened and a balanced differential input current I_{ind}, defined by $I_{ind} = I_{in+} - I_{in-}$ and $I_{in+} = -I_{in-}$, is applied to the input. Due to the negative feedback mechanism, the differential input voltage of G_{m1} is forced to be very small and all the input currents become feedback currents flowing into the output terminals of G_{m2} so that a large voltage swing (which is dependent on the amplitude of the input current) occurs at the input terminals of G_{m2} instead of G_{m1}. So for the whole sampling period, the voltages across switches S_2 are almost constant and at the end of the sampling phase (S_2 and S_1 are turned off and S_3 is turned on) the charge injection from the switches is almost independent from the input signal amplitude (almost constant) and will be cancelled out providing an accurate differential output current, I_{od}.

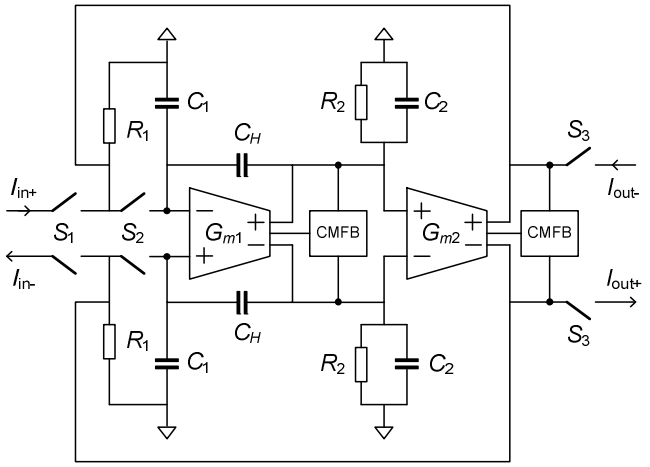

Figure 5. Fully differential CSH circuit including parasitic elements and CMFB circuits

As can be seen from Figs. 4 and 5, what we need from the first stage is a high voltage gain. G_{m2} determines the range of I_{ind} that the CSH circuit can handle. Based on above considerations, we employ the circuits in Fig. 6 to realize the CSH circuit. Fig. 6a shows a simple PMOS differential pair with its tail current I_B and loaded by transistors M_2 biased by V_{B-} (supplied from a CMFB circuit). For being operated in weak inversion saturation, the small signal transconductance gain of this circuit can be found to be $G_{m1} = I_B/2nU_T$. R_2 and C_1 approximately are $r_{ds1}//r_{ds2}$ and C_{sg1}, respectively.

In order to obtain a high current swing, the class-AB circuit in Fig. 6c is employed to realize G_{m2}. Since the input voltage of this circuit is not forced to be small but to handle the large current swing, the large signal characteristic of the circuit is of interest. From the exponential behavior of weak inversion saturation devices we can find the voltage to current relationship of this circuit as [9]

$$I_{\text{od}} = I_{\text{out+}} - I_{\text{out-}} = 4I_B \sinh\left(\frac{V_{o+} - V_{o-}}{nU_T}\right) = 4I_B \sinh\left(\frac{V_{od}}{nU_T}\right). \quad (1)$$

Equation (1) implies that a very high current drivability is obtainable. Passive elements C_2 and R_1 are approximately given by $3C_{sg4}$ and $r_{ds2}//r_{ds4}$, respectively.

The circuit in Fig. 6b is used as CMFB circuit to detect the common-mode (CM) signal at the high impedance nodes, to compare this CM voltage to a reference voltage, V_{ref}, and to feed back the error signal to control the bias currents of G_{m1} and G_{m2} via V_{B-} and V_{B+}, respectively.

B. Stability Considerations

From Fig. 5 and assuming all the circuit elements are linear, breaking the loop at the input of G_{m2}, the LG can be found as

$$LG \cong \frac{G_{m1}G_{m2}R_1R_2\left(1 - \dfrac{sC_H}{G_{m1}}\right)}{s^2R_1R_2\left(C_1C_2 + C_HC_1 + C_HC_2\right) + sG_{m1}R_1R_2C_H + 1}, \quad (2)$$

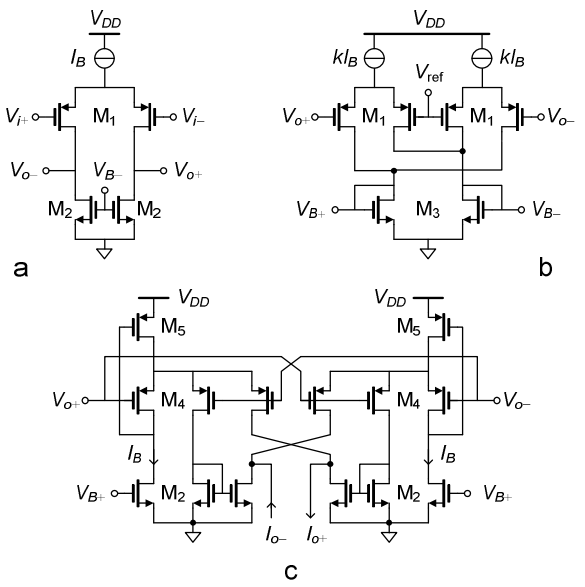

Figure 6. Sub-circuits a) simple differential pair b) CMFB circuit and c) class-AB sinh tranconductor

which is in the form of a generic two stage amplifier and the open-loop unity gain frequency, poles and RHP zero can be approximated to be $\omega_u \cong G_{m2}/C_H$, $\omega_{p1} \cong -\left(G_{m1}R_1R_2C_H\right)^{-1}$, $\omega_{p2} \cong -G_{m1}/\left(C_1 + C_2\right)$, and $\omega_{z1} \cong G_{m1}/C_H$, respectively [10].

To keep the circuit stable, the small signal transconductance of the circuit in Fig. 6c is taken into account. It is found from (1) and equals $G_{m2} = 4I_B/nU_T$. We may thus need to control the bias currents of G_{m1} and G_{m2} and C_H to achieve sufficient phase margin. It should be noted that this design is intended for large signal operation and that the pole and zero locations move according to the input signal amplitude. The dynamic behavior of the pole-zero locations can be only described properly using the circuit's dynamic eigenvalues [11] and the circuit stability can be optimized for a large certain range of input signals.

C. Effect of Switching Error and Offset

Resulting from the mismatch between the set of switches S_2 and C_H, the charge injection error not can be completely removed. This residue error will be combined with the effective input offset of G_{m2} degrading the linearity of the CSH circuit. To analyze the circuit distortion, we model the offset error as

$$V_E = V_{\text{offset}} + V_{CFT+} - V_{CFT-}, \quad (3)$$

where V_{offset} is the input offset of G_{m2} combined with the output offset of the first stage and V_{CFT+} and V_{CFT-} are error voltages induced by charge injection and clock-feedthrough effects [12, 13] appearing on the non-inverting and inverting terminals of G_{m2}, respectively. Considering the output current in the hold phase, including the effect of V_E, we have

$$I_{out} = \varepsilon_1 I_{in} + \varepsilon_2 \cosh\left(\sinh^{-1}\left(I_{in}/2I_B\right)\right), \quad (4)$$

where $\varepsilon_1 = 4I_B \cosh\left(V_E/nU_T\right)$ and $\varepsilon_2 = 4I_B \sinh\left(V_E/nU_T\right)$.

Using a 4th order Taylor's expansion, undesired components are dominating at the 2nd and the 4th harmonics and the 2nd and 4th harmonic distortions are found to be

$$HD_2 = \frac{\varepsilon_2}{\varepsilon_1}\frac{1}{16}\frac{\hat{I}_{in}}{I_B^2}\left(1-\frac{1}{64}\left(\frac{\hat{I}_{in}}{I_B}\right)^2\right) \quad (5)$$

and

$$HD_4 = \frac{\varepsilon_2}{\varepsilon_1}\frac{1}{4096}\frac{\hat{I}_{in}^3}{I_B^4}, \quad (6)$$

where $\hat{I}_{in}$ is the amplitude of the input signal. From (5) and (6), the distortions can be kept low for a small input current and can be minimized by careful layout of the differential pair and the class-AB sinh circuits and/or using a large C_H.

IV. Simulation Results

The CSH circuit has been designed and simulated in Cadence/RF Spectre using TSMC 0.13µm CMOS process parameters. Transistor sizes are shown in Table 1. V_{DD} =0.65V, V_{ref} =0.15V and C_H =0.6pF. Biasing currents I_1=30nA and I_2=0.1nA are set for G_{m1} and G_{m2}, respectively. All switches are realized by NMOSTs with a threshold voltage of $V_{tn} \cong 0.3$V and driven by clock signals switching between V_{DD} and ground. The dimensions of the switches are all identical and chosen to be as small as the process allows to minimize charge-injection and clock-feedthrough effects (W = 0.15µm and L = 0.13µm). The quiescent power of the entire circuit equals 23.8nW.

Noise and linearity performances are verified using periodic steady state (PSS) and periodic noise (PNOISE) analyses for a 1.25kHz input signal with its amplitude varying from 20pA to 74nA and a 20kS/s sampling rate. The total harmonic distortion (THD), SNR and SNDR are plotted and shown in Fig. 7. From this plot, a dynamic range (DR) (measured up to a THD of 1%) of 83.2 dB is obtained and an SNDR of 74.3dB can be achieved at a 40nA input amplitude. This leads to an effective number of bits (ENOB) of 12 and a figure of merit (FoM), that embraces the effects of distortion, sampling speed, and power consumption, of 0.51nW/MHz ($\text{FoM} = P/f_s 2^{\text{ENOB}}$, where P represents the average power consumption and f_s is the sampling rate) which is more than an order of magnitude better than of a recently proposed CSH circuit (FoM = 30nW/MHz) [13].

Conclusion

Theory and design of a sub-threshold class-AB CSH circuit have been presented. The proposed CSH circuit operates from a very low supply voltage, consumes ultra low quiescent power and provides very high DR and SNDR. This verifies that the proposed CSH circuit can be considered a very good candidate for ultra low-power sampled-data filter and data converter design.

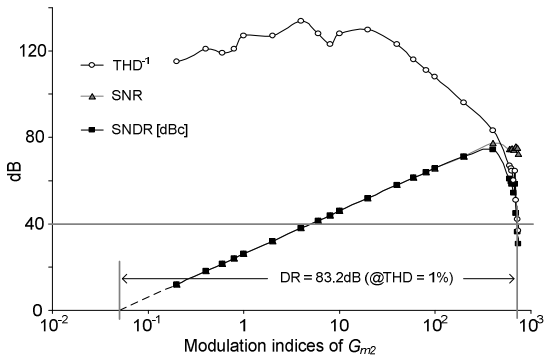

Figure 7. THD, SNR and SNDR as function of the modulation index ($\hat{I}_{in}/I_B$) of the class-AB transconductor

TABLE I. Transistor dimensions

MOSFET	M_1	M_2	M_3	M_4	M_5
W/L, [µm/ µm]	5/2	4/2	0.4/2	0.25/2	0.5/1

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