A low power UWB-LNA using Active Dual Loop Negative feedback in CMOS 0.13µm

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***Abstract*— A low noise amplifier for UWB and broadband applications is presented. The active dual loop negative feedback architecture dissevers the severe tradeoff existing between the input impedance, gain and noise figure, and produces a flat S_{11} across the entire band. The LNA is composed of a voltage amplifying negative feedback amplifier with a trans-conductance amplifier forming a shunt-shunt feedback around it, thereby tailoring the input impedance with respect to the gain settings of the first amplifier.**

The values of the resistive feedback elements have been chosen such that they fulfill the requirements of gain, input impedance, noise figure and linearity. The design has been carried out in TSMC 0.13um CMOS Technology. From circuit simulations, the average gain of the LNA across 2-7GHz is 13dB. The noise figure is below 4dB with a minimum of 2.9dB. S_{11} is below -15dB for the entire frequency band. The design employs a DC-current re-use scheme to reduce the power consumption. The LNA draws 5.6mA from a 1.2V supply.

I. INTRODUCTION

A low-noise amplifier (LNA) is a critical component in ultra-wideband (UWB) and broadband receivers and cognitive radios. Recent publications have reported ways to obtain wideband input noise and impedance matching and gain, through filter-matching techniques [1], indirect dual feedback [2], distributed amplifiers [3], resistive feedback [4] and using a common-gate input stage [5].

This paper investigates the use of active double loop negative feedback in order to obtain a flat S_{11} and high gain over a wide bandwidth, while ensuring low power consumption. By using two loops an attempt has been made to alleviate the stark trade-off existing between noise, input matching and gain of an LNA. Negative feedback provides the ability to tailor port impedances for optimal noise and impedance matching and simultaneously reduces distortion by a factor of the loop gain. Negative feedback also ensures gain stability over process and supply variations.

The paper is organized as follows: The conceptualization of the LNA is demonstrated in section II. Section III explains all the aspects taken into account during circuit design. Simulation results and conclusions are presented in section IV & V.

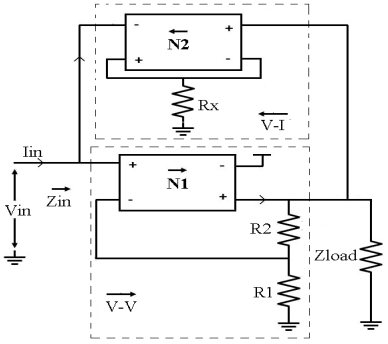

Fig. 1 Double loop negative feedback power-to-voltage LNA

II. LNA TOPOLOGY

The two feedback loops in the proposed LNA comprise a voltage-sense voltage-feedback (V-V) loop which sets the output gain and an active voltage-sense current-feedback (V-I) loop which sets the input impedance with respect to the gain settings determined by the first loop. The conceptual diagram with Nullors N1 and N2 is depicted in Fig.1. For the V-V loop it holds:

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{R_1} \tag{1}$$

For the active V-I loop:

$$\frac{I_{in}}{V_{out}} = \frac{1}{R_x} \tag{2}$$

In (2), I_{in} is the output current of N2 and V_{out} is the output voltage of N1, which is indeed the input to N2. R_2 and R_1 are the feedback and input resistances forming the V-V loop and R_x defines the trans-conductance of the V-I loop. Solving (1) and (2), we can obtain an expression for the input impedance $Z_{in,}$ as follows:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{R_1 R_x}{R_2 + R_1} \tag{3}$$

After selecting the ratio of R_2 and R_1 to set the Gain[1], R_x can then be chosen to design for the input impedance to be matched to the 50Ω source. The load impedance is assumed to be 50Ω. For the power gain it holds:

$$|S_{21}|^2 = \frac{P_{out}}{P_{in}} = \frac{{V_{out}}^2}{Z_{Load} V_{in} I_{in}} \tag{4}$$

[1]A trade-off between noise and distortion exists with the value of R_1 and R_2

The resistors R_2, R_1 and R_x contribute noise and all the noise sources shifted across the two loops and referred to the input, give an expression for the input referred noise. The total noise Voltage spectral density at the input is given by:

$$S_{vn,\,eq} = 4KTR_s + S_{vn1} + \left(\frac{R_2R_1}{R_2+R_1} + R_s\right)^2 . S_{in1} + 4KT\left(\frac{R_2R_1}{R_2+R_1}\right) S_{vn2}\left(\frac{R_s}{R_x}\right)^2 + S_{in2}R_S^2 + \frac{4KT}{R_x}R_S^2 + S_{vL}\left[\left(\frac{R_s}{R_x}\right)^2 + \left(\frac{R_1}{R_2+R_1}\right)^2\right] \quad (5)$$

S_{vn1}, S_{in1} and S_{vn2}, S_{in2} are the input referred power of the voltage and current noise sources of the input stage of N1 and N2, respectively. From (5), it can be seen that the load contribution to noise is present. The output impedance of N1 is pulled to zero by negative feedback hence the current noise contribution of the load is cancelled out. The noise voltage source though, is transformed to the input via the transfer of the entire LNA. S_{vL} is the input referred power of the noise voltage of the next stage, which is modeled here by a 50 Ω resistor representing the input impedance.

III. NULLOR DESIGN

The circuit diagram, with both nullors implemented is depicted in Fig. 2. For N1, we have designed a two stage amplifier using the DC current re-use technique. The first stage, transistor M1, has a narrow band-pass response, which peaks at the resonance frequency of the series L_d C_2 load. The second stage, transistor M2, is a common source amplifier with bridged T-coil peaking bandwidth enhancement [6], to ensure gain over a wide bandwidth. N2 is a degenerated common source amplifier, involving R_x and transistor M3. The effective trans-conductance – G_m approaches $1/R_x$, for large values of g_m. This occurs, provided the device M3 is still in saturation.

A. Input Stage , Noise due to Active Feedback

The input stage, transistor M1, should have a high gain in order to suppress the noise contribution of subsequent stages. A high g_m ensures this, as well as reduction in the input referred noise voltage due to its own channel noise. Its input referred current source diminishes with increase in f_T of the device. Hence, though g_m increases with the aspect ratio to a certain extent, the f_T of the device consequently decreases. The g_m/g_{ds} ratio and the Q-factor of the inter-stage network determine its frequency response. The transistor is biased for cancellation of its g_{m3} component (discussed in section III C); the aspect ratio has thus been chosen keeping in mind these considerations.

Fig. 3 shows the noise sources of transistor M3. The channel noise current $I_{n,d}$ can be represented by two equivalent sources $I_{n,d1}$ and $I_{n,d2}$. If $I_{n,d1}$ flows entirely through the transistor, then it completely cancels out the effect of $I_{n,d2}$, effectively ruling out noise contribution of channel noise and only the noise contribution of $I_{n,Rx}$ is seen at the output. Thus, increasing R_x reduces noise, and so does increasing the g_m. The aspect ratio of M3 has to be chosen such that the effect of C_{gs} does not become pronounced.

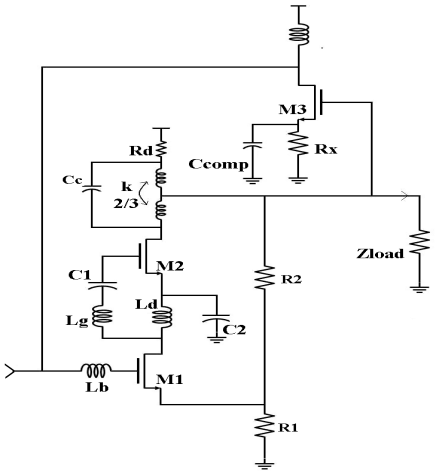

Fig. 2 Signal Diagram of the proposed LNA (Bias not Shown)

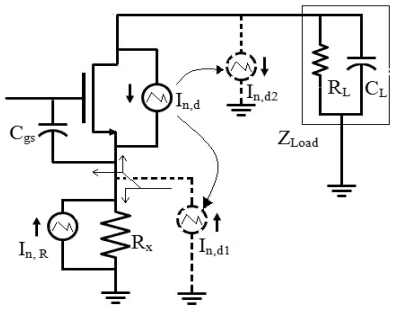

Fig. 3 Noise sources in M3 of Nullor N2.

B. The Interstage Network and DC-Reuse Technique

The inter-stage network is formed using Ld, C2, Lg and C1 and performs a current-reuse function to achieve high power gain. The lower frequency edge of the band-pass response of the LNA is determined by the Ld-C2 resonance frequency, above which the inductance Ld forms a high impedance path and acts as an AC signal block. Lg and C1 are used to perform a series-resonance with Cgs of M2, in the low impedance path. The series resonance has a narrow band characteristic and has a resonant frequency. This is used to enhance the gain at the higher end of the desired band. A high gm/gds ratio is maintained for M1 to provide high gain at the lower side of the band. The lower edge of the frequency band is limited by the size limit of Ld. The equivalent signal model of the inter-stage is shown in Fig. 4. Fig. 5 shows the frequency response of the network.

Lb, though not part of the inter-stage network, is used to reduce the effect of the input capacitance of N1. Though it resonates with the capacitance at a particular frequency, it proves useful in improving the S_{11} over a large bandwidth. It also helps in shaping the noise response as it can be used to control the frequency at which noise match occurs.

C. Linearity

Distortion is classified into weak distortion and clipping distortion. The low noise amplifier in a receiver typically

operates well below its 1dB compression point, thus the scope for clipping distortion is largely reduced. The trans-conductance source (g_m) and output conductance (g_d) are the two main sources of non-linearity. When the drain voltage swing is low, trans-conductance is the dominant source of non-linearity. A simple analysis of g_m distortion can be made considering the 1st, 2nd and 3rd order terms of trans-conductance non-linearity, for a two-tone input signal. Assuming equal amplitude for both tones: $a\cos(\omega_1 t)$ and $a\cos(\omega_2 t)$.

$$g_{m1} V_{gs} = g_{m1} .a \{\cos(\omega_1 t) + \cos(\omega_2 t)\} \quad (6)$$

$$g_{m2} V_{gs}^2 = g_{m2} .a^2 + g_{m2} \{ \frac{a^2}{2} \cos(2\omega_1 t) + \frac{a^2}{2} \cos(2\omega_2 t)\} + g_{m2} .a^2 \{\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\} \quad (7)$$

$$g_{m3} V_{gs}^3 = g_{m3} a^3 \{ \frac{9}{4} \cos(\omega_1 t) + \frac{9}{4} \cos(\omega_2 t)\} + g_{m3} .a^3 \{ \frac{1}{4} \cos(3\omega_1 t) + \frac{1}{4} \cos(3\omega_2 t)\} + g_{m3} .a^3 . \frac{3}{4} \{\cos(2\omega_1+\omega_2)t + \cos(2\omega_1-\omega_2)t + \cos(2\omega_2+\omega_1)t + \cos(2\omega_1 t - \omega_2 t)\} \quad (8)$$

From (7) it can be seen that the second order term generates harmonic distortion components at $2\omega_1$ and $2\omega_2$ and the IM2 components. It is interesting to note that the second order term generates a DC component, making the bias RF dependent! From (8), the 3rd order inter-modulation distortion component at $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ are located close to the fundamental tones, and are hard to filter out.

The dependence of g_{m3} on V_{GS} is such that it changes from positive to negative when V_{GS} transitions from the moderate to the strong inversion region. There exists a zero crossing point (Fig. 6) for g_{m3} at a particular gate bias [7]. Transistor M1 is biased close to this voltage. Transistor M2 is biased at Vdd, in an attempt to minimize device size for a particular value of trans-conductance. M1 and M2 form a dual stage amplifier and thus, as the gain of the first stage increases, the overall IIP3 reduces, since the IM3 increases as a function of the third power of the input amplitude. This conflicts with the requirement for low noise.

In order to ensure low distortion, it is necessary to have high loop gain. IM2 and IM3 reduce directly by a factor of the loop gain [8]. Source degenerated M3 provides active feedback. The weak distortion contribution of which is also reduced by a factor of the loop gain introduced by the degeneration resistance. The degeneration resistance reduces IM2 by a factor of (1/1+T) and IM3 by a factor of $T/(1+T)^2$. Where T is the loop gain and (1+T) is the return factor [9].

In the presence of negative feedback, the second harmonics generated by $g_{m2}V_{gs}^2$ are fed back to the input, thus adding to the fundamental components of Vgs. These spectral components then get mixed in $g_{m2}V_{gs}^2$ and contribute to IM3. This contribution is fortunately quite small in the presence of sufficient loop gain, which suppresses the 2nd order harmonic components. Focusing on accurate design of the magnitude of the loop-gain and using the needed gate bias to stem the effect of g_{m3}, the LNA has been designed to demonstrate an IIP3 greater than -7dBm across the entire frequency range.

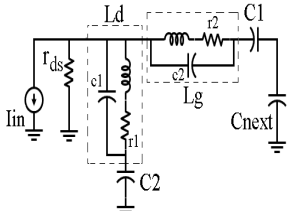

Fig. 4 The Inter-stage Network

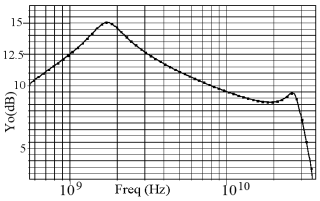

Fig. 5 First Stage AC response

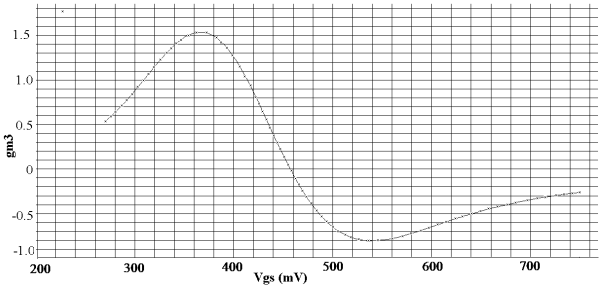

Fig. 6 Variation of g_{m3} with V_{gs} for Transistor M1

D. Bandwidth and Biasing

The LNA has a bandwidth of 2-7GHz. Each stage contributes to the LP product [8], and hence to the bandwidth. Peaking techniques are commonly used for enhancing the bandwidth of wideband amplifiers.

The bridged T-coil (BTC) peaking circuit [6] has been used in the second stage of nullor N1. The BTC is obtained by augmenting a simple T-coil circuit with a bridging capacitor and gives the largest bandwidth extension among other techniques. For a mutual coupling factor k= 2/3, the bridged T-coil circuit provides almost 2.8x improvement in the bandwidth of the second stage [10].

Since peaking circuits don't produce a flat transfer curve, the active feedback through M3, requires compensation in the form of C_{comp} (Fig. 2). The addition of C_{comp}, though degrades the noise performance as it is seen in parallel to Rx by noise current $I_{n,d1}$ (Fig. 3). Based on the discussion in III-A, reduction in degeneration impedance of the active feedback results in increased noise contribution.

The circuit has been biased in order to ensure all signal parameters are obtained. The circuit with biasing is shown in Fig. 7. Bias transistor M5 is degenerated with resistance R_{bx} to reduce its noise contribution.

IV. SIMULATION RESULTS

Simulation results for the LNA and a table of comparison, with current LNA designs is presented in this section.

Fig. 8 shows the noise figure, which across the band is less than 4dB with a minimum of 2.9dB at 2.6GHz. Fig. 9 shows the forward transmission co-efficient S_{21} and the input reflection co-efficient S_{11}. The S_{21} measured across the bandwidth of 2-7 GHz is 13 ± 1.5 dB. S_{11} is below -15dB and the stability factor (k) is greater than 1.2 for the entire frequency range. The total power consumption of the LNA

TABLE.1

COMPARISON WITH RECENTLY REPORTED STATE-OF-THE-ART WIDEBAND AMPLIFIERS

	Tech.	S_{21}[dB]	S_{11}[dB]	B[GHz]	NF(dB)	Power [mW]	IIP3[dBm]
[1]	0.18 µ SiGe (BJT)	19±2	<-9	3-10	4 - 9	30mW@3.3V	-5.5 to 3
[2]	CMOS 0.13 µ	16±1	<-10	3-12	2-4	16.8mW@1.2V	-15.6@7GHz
[3]	CMOS 0.18 µ	8±0.6	<-16	.04-6.2	4.2-6.2	9mW	3 (freq. N/A)
[4]	CMOS 0.13 µ	12	<-9	2-5.2	4.5-5.7	11.1mW@1.8V	-5.5@5GHz
This Work	CMOS 0.13µ	13±1.4	<-15	2-7	2.9-4	6.7mW@1.2V	-4.8@4GHz

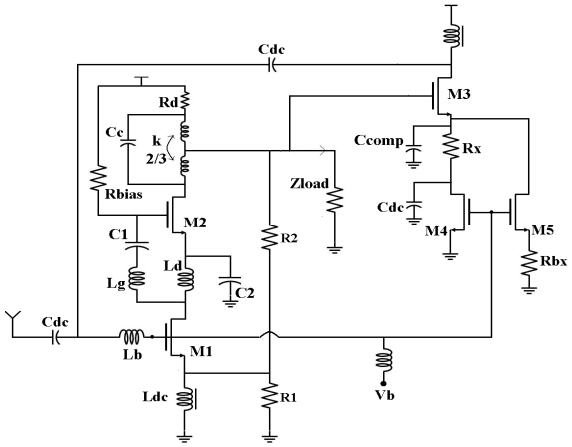

Fig. 7 Circuit Diagram of the LNA with Biasing

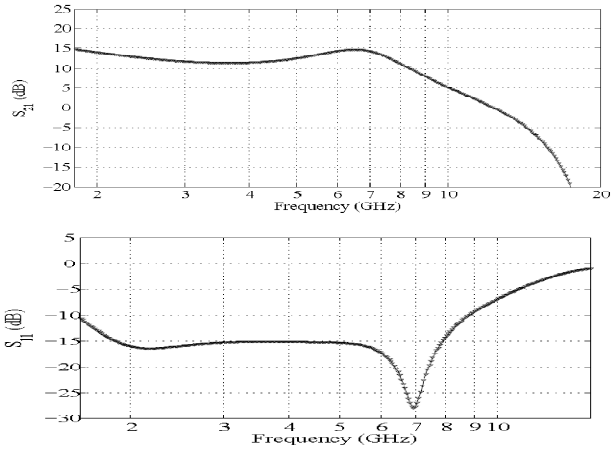

Fig. 8 S_{21} (above) and S_{11} (below) of the LNA Vs frequency

is 5.6mA from a 1.2V source.

V. CONCLUSION

An ultra-wideband, low power, active double loop negative feedback amplifier designed in 0.13µm technology has been presented. The concept of having two negative feedback loops for setting the gain and the input impedance accurately over a wide bandwidth has been justified with good simulation results. The stability factor is greater than 1.2 and the amplifier provides a flat S_{11}<-15dB over the entire band with a gain of 13dB at low current consumption of 5.6mA from a 1.2V source.

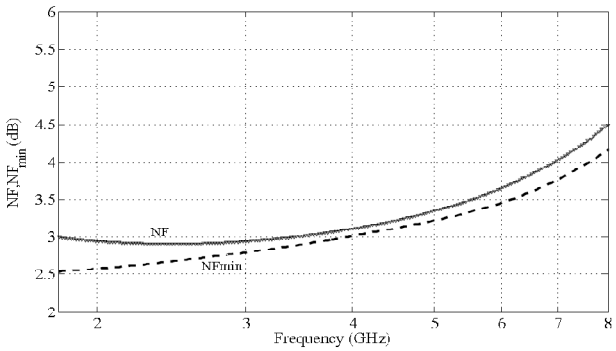

Fig. 9 Noise Figure

ACKNOWLEDGEMENT

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