A Time-Interleaved Sampling Delay Circuit for IR UWB Receivers

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***Abstract*—This paper presents a time-interleaved sampling delay circuit to be used in an autocorrelation receiver for impulse-radio UWB. It applies a 10 GHz time-interleaved sampling and readout operation for analog signal storage and reconstruction. The delay function is achieved by shifting the sampling and reading clock sequence by a particular time interval. System analysis shows the feasibility of using sampling operation in the delay without losing autocorrelation information, and gives design suggestions for the circuits. The delay circuit has been designed to be implemented in TSMC 0.13 um CMOS technology. Simulation results predict a 500 ps delay at a power consumption of 10 mW from a 1.2V power supply. Moreover, the delay range from 100 ps to 900 ps can be covered in 100 ps steps without additional power consumption.**

I. Introduction

The autocorrelation receiver (AcR) [1] is a popular receiver architecture for impulse radio (IR) ultra wideband (UWB) communication due to its simplicity, as illustrated in Fig. 1. In impulse radio, consecutive pulses are transmitted with a predefined delay τ_d between each other. The first pulse acts as a reference, whereas the second pulse is modulated with the binary information. The autocorrelation receiver correlates the incoming signal with its delayed version. Hence, the binary information in the autocorrelation of incoming pulses can be recovered from the sign of the output after integration. This modulation scheme is called *transmitted reference UWB* (TR-UWB). However, this basic architecture suffers from strong narrow band interference, and as the majority of components has to operate at UWB frequencies, the overall receiver becomes power consuming.

A *Quadrature Downcoversion Autocorrelation Receiver* (QDAR) as shown in Fig. 2, has been proposed to operate in the presence of strong narrowband interference [2]. In this receiver, the incoming UWB signal is first downconverted to lower frequencies before it is delayed. This allows the delay to operate at lower frequencies. However, the realization of an accurate and low power delay circuit is still quite challenging, and often becomes the bottleneck for the overall performance

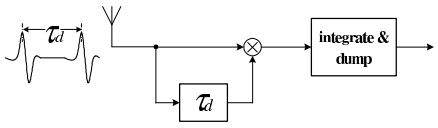


Fig. 1. An autocorrelation receiver with a typical waveform

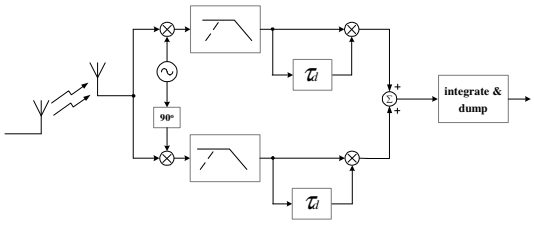
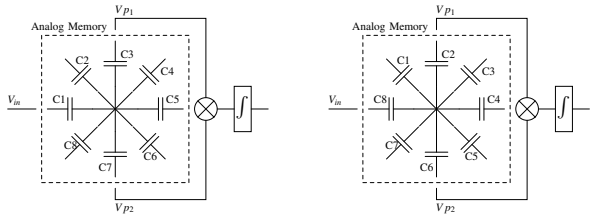


Fig. 2. Quadrature Downconversion Autocorrelation Receiver



(a) Clock Phase 1 (b) Clock Phase 2

Fig. 3. Time-Interleaved Sampling Autocorrelation Architecture Diagram

of the receiver.

In [3], Bagga et al have proposed a delay filter. This delay approximates the transfer function of an ideal delay by a gm-C filter. However, the delay time of this pure analog approach is difficult to control. A quantized analog delay was proposed in a mixed-signal approach in order to have a easy control of the delay time [4]. The power consumption of these two designs is too high to apply them successfully in real applications. Furthermore, the signals generated by these delay circuits exhibit serious distortion in waveform, which will introduce errors in the autocorrelation performed. This will degrade the performance of the receiver.

In this paper, a novel time-interleaved sampling delay architecture is proposed in order to overcome the aforementioned power consumption and distortion problems. Its conceptual diagram is shown in Fig. 3. The input signal is first sampled and stored in an analog memory array, and subsequencyly, the two signal waveforms with different delay times are reconstructed from the same analog memory. In this way, the two reconstructed signal waveforms should be identical and differ only by a shift in time. As a result, possible errors in the autocorrelation of the waveforms will be avoided.

A system level analysis of the proposed delay architecture is

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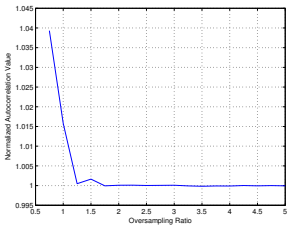
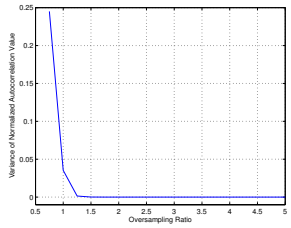


(a)



(b)

Fig. 4. Autocorrelation of Sampled Gaussian Monocycle Signal: Mean Value (a) Variance (b)

presented in Section II. Section III describes the circuit implementation of the time-interleaved sampling delay. Simulation results are given in Section IV. Finally, conclusions are drawn in Section V.

II. System Analysis

The principle of the proposed delay architecture can be explained using Fig. 3. In Fig. 3(a), the input signal waveform is sampled on C1, and at the same time the previously sampled signal voltage on C3 and C7 are correlated. After one clock cycle, the capacitor array rotates by one capacitor, the input signal is sampled by C8, and the voltage on C2 and C6 are correlated, as in Fig. 3(b). In this way, by rotating the capacitor array, the time-interleaved sampling operation is applied to the input signal, and two delayed versions of the input signal with different delay time are generated.

To evaluate the delay performance, the effect of the sampling operation on the autocorrelation information delivered by this delay architecture is considered. From the analysis it will be found that the sampling clock frequency and jitter performance are of great importance to the delay circuit.

A. Sampling Frequency

Compared to the original analog waveform, the autocorrelation of the sampled signal is somehow depending on the initial sampling instance. Fig. 4 shows a Monte Carlo simulation result of the mean and variance of the autocorrelation for a sampled gaussian monocycle input signal as a function of the sampling frequency in Matlab in case of random initial sampling .

From this simulation it follows that, if the sampling frequency is higher than two times the signal bandwidth, then the loss in autocorrelation for the sampled signal can be neglected. Thus, oversampling is suggested in order to reduce the loss in autocorrelation.

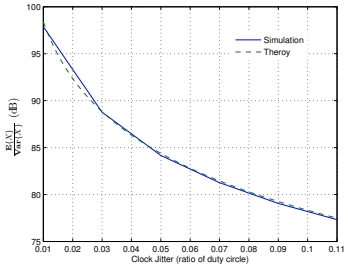


Fig. 5. Output Signal to Noise Ratio vs Clock Jitter

B. Clock Jitter

In this sampling system, clock jitter will introduce noise into the output, further degrading the detection sensitivity. Considering the noise introduced by jitter only, the SNR at the output of the integrator is:

$$\mathbf{SNR} = \frac{W_p f_s}{2\alpha\sigma^2 + \beta\sigma^4} \tag{1}$$

where W_p is the pulse energy, f_s is the sampling frequency, σ^2 is the square of the edge-to-edge clock jitter J_{ee} and α and β are coefficients related to the shape of the pulses. From (1), it is suggested that oversampling can improve the SNR.

Fig. 5 shows the analytical result and Matlab Monte Carlo simulation result of output SNR with different jitter , which are well matched. Hence, if the desired noise performance and sampling frequency is known from design requirements, requirements for the maximum clock jitter can be found. Similar analyses for other sources of imperfection have been done, and the conclusion can be drawn, namely that oversampling is a good way to improve the autocorrelation performance.

In conclusion, oversampling in this delay architecture should be applied in order to achieve good overall performance, and the clock performance is quite critical in this architecture. Here, a 10 GHz time-interleaved sampling delay circuit with ten analog memory elements is chosen. Its design will be discussed in the following section.

III. Time-Interleaved Sampling Delay Circuit

The circuit implementation of the time-interleaved sampling delay element is composed of two main blocks, namely the analog memory array and the multiphase clock generator. The circuit details will be discussed below.

A. Analog Memory Array

The core part of this delay circuit is the analog memory array, which takes care of the signal storage and reconstruction. It comprises ten analog memory cells in parallel. In order to achieve high speed and low power consumption, the sampling capacitors in the analog memory cells should be small. For this reason, parasitic gate capacitances of MOS transistors are used as sampling capacitors. A single analog memory cell is shown in Fig. 6.

M_2 is the sampling switch, controlled by the sampling clock Clk_s. M_3 is the readout switch, controlled by clock Clk_r. M_1 is

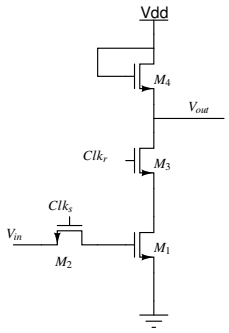


Fig. 6. A Single Analog Memory Cell

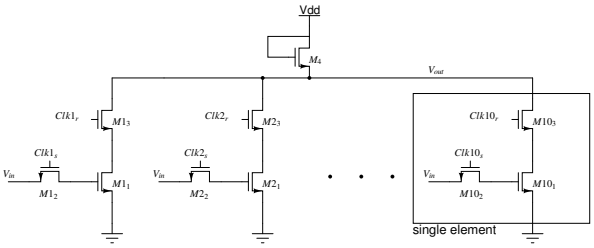


Fig. 7. Analog Memory Array

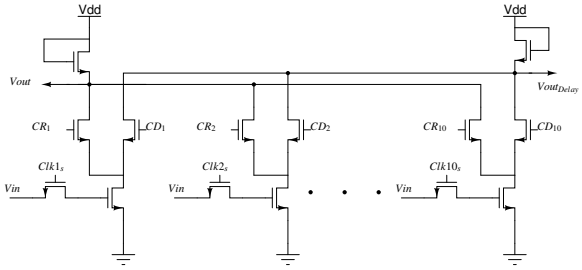


Fig. 8. Analog Memory Array with Two Outputs

a common source stage and also provides a sample capacitor using its parasitic gate capacitor C_{gg}. M_4 is a diode connected common load, and converts the current originating from M_1 back into a voltage.

The circuit for one analog memory array is shown in Fig. 7. Ten analog memory cells are connected in parallel with the same common load M_4. For the time-interleaved readout scheme, the power consumption of the analog memory array is the same as that of a single cell. So the power consumption of this architecture does not change with the delay time nor with the number of elements used.

Furthermore, two analog memory arrays can also share the same sampling capacitors, resulting in an analog memory array circuit with two outputs with different delays, as shown in Fig. 8. The delay time of the two different outputs is defined by the time difference between the readout clocks CR_n and CD_n.

B. Clock Generation

The rotating operation described for the circuit of Fig. 3 is achieved by applying multiphase clock to the switches in the analog memory array. The waveform for the ten sampling clocks are shown in Fig. 9. Each clock Clk_n is about 100

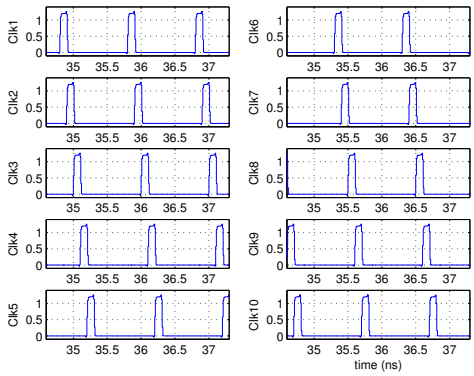


Fig. 9. Transient Waveform for 10 Sampling Clocks

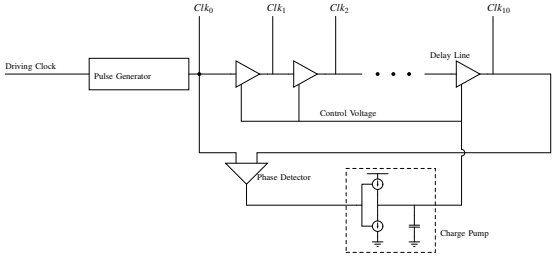


Fig. 10. Clock Generation Schematic

ps delayed with respect to its previous clock Clk_{n-1}. The clocks for the readout switches are the same clocks used for the sampling switches, albeit with a different sequence.

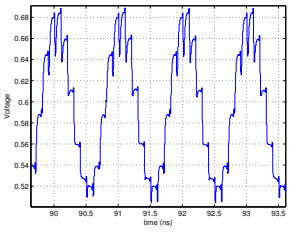
The clock generator is an important block, as it determines the delay accuracy and correlation performance of the entire delay circuit. Fig. 10 demonstrates a delay-locked loop (DLL) based multiphase clock generator [5]. In this scheme, Clk_0 and Clk_{10} are well aligned by controlling the control voltage of the delay cells. The driving clock signal, originating from an oscillator, has a clock period of 1 ns. The driving clock is fed into the pulse generator where a pulse signal Clk_0, is generated, with a clock period of 1ns and a duty cycle of 100ps. By a cascade of voltage controlled delay cells, all multiphase clocks will be generated.

IV. Simulation Results

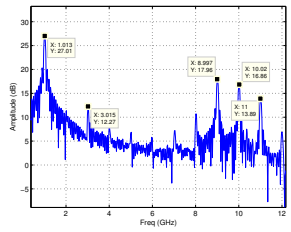
All simulations are done for a 1.2V power supply in TSMC $0.13\mu m$ technology using Cadence.

Fig. 11 shows the transient waveform and its spectrum of one output of the analog memory array with a 1-GHz sinusoidal input signal. The glitches originate from the switching activity in the circuits. Although the glitches are quite large in the waveform, the signal at low frequency is not affected. As a consequence, the presence of the glitches will only give an fixed offset to the autocorrelation, which does not affect the detection of the information.

Fig. 12 shows the input and single output signal waveform. The delay time is about 500 ps. Fig. 13 shows the output waveform of the two outputs of the analog memory array. There is a 500 ps delay between two output waveforms,



(a)



(b)

Fig. 11. Transient Output Waveform (a) and Spectrum (b) for Sinusoidal Input

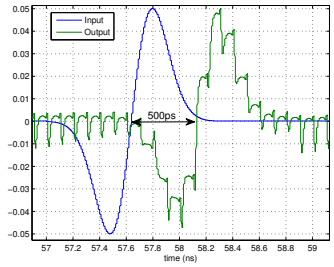


Fig. 12. Input and Output Waveforms of Analog Memory Array

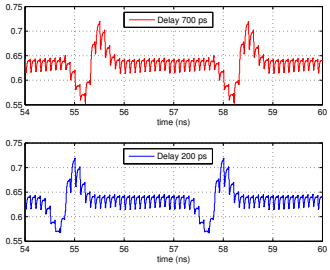


Fig. 13. Outputs with Different Delay Time

and they have almost the same shape. The delay function is successfully realized.

The results of Monte Carlo simulations of the output waveform where the components are varied over process parameters are shown in Fig. 14. From this figure, it can be observed that mismatch in the circuits does not considerably affect the timing of the output nor the shape of the waveform, and as such the autocorrelation is preserved. Thus this design is not very sensitive to component mismatch.

Other simulation results are listed in Table I. The total power

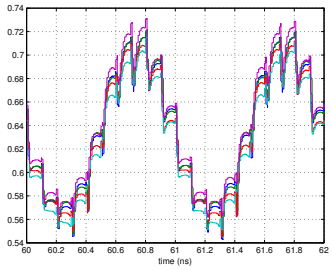


Fig. 14. Output Waveform Monte Carlo Simulation

TABLE I
COMPARISON BETWEEN THIS WORK AND PREVIOUS WORK

	[3]	[4]	this work(simulated in TSMC 0.13μm)
Power W	70 mA @ 1.6 V	36.7 mA @ 1.6 V	8.33 mA @ 1.2 V
Delay Time τ_d	720 ps	550 ps	500 ps
W and τ_d	not available	$W \propto \tau_d$	W is constant

consumption including the clock generation is about 10 mW. For different delay times from 100 ps to 900 ps in 100 ps steps, the power consumption stays the same as that for a 500 ps delay.

V. CONCLUSION

In this paper, a time-interleaved sampling delay has been proposed. The influence of the delay element on the AcR has been analyzed, and circuit techniques to implement the delay have been proposed. From simulation results, this delay element shows low power consumption and good delay accuracy. Thus the time-interleaved sampling delay architecture fulfills the requirements of the delay element in an AcR. A comparison between this design and previous designs is also listed in Table I.

This delay has the apparent advantage of a lower power consumption when delay time is comparable with other designs. A delay range from 100 ps to 900 ps can be covered without extra power consumption. The flexibility of this delay allows for multiple outputs with different delay timing, which makes the receiver robust to distortion introduced by the delay. Thus, this delay outperforms previous designs in power consumption and functionality.

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