Nanopower Sampled Data Wavelet Filter Design using Switched Gain Cell Technique

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***Abstract*—In order to realize a nano-power wavelet filter for biomedical applications, this paper applies the Singular Value Decomposition approximation to transform the time domain 1st-derivative of a Gaussian (gauss1) wavelet base into a 5th-order z-domain transfer function. Consequently, to realize the approximated transfer function in CMOS technology employing circuitry that operates from a low supply voltage, a sampled data circuit technique, coined '*Switched Gain Cell*, (SGC),' is introduced. Using the SGC technique, standard MOS switches, simple subthreshold (nonlinear) transconductors and their associated parasitic capacitances suffice to constitute the filter, while the scale of the filter can be controlled by the clock frequency. This renders the filter architecture to be simple, modular, and area efficient. Simulation results, using 0.13µm CMOS model parameters, show that the wavelet filter implements the gauss1 wavelet base well, operates from a 1V supply and consumes less than 0.47 µW quiescent power.**

I. INTRODUCTION

The wavelet transform (WT) is a useful tool for multi-resolution signal analysis and has been widely used in biomedical applications [1]. To perform the WT, software-based approaches combined with digital hardware have been employed [2] albeit at heavy computational cost and occupying a large chip area.

To meet the requirement for ultra low power real time signal processing, an analog wavelet filter (WF) performing the WT has been introduced employing the dynamic translinear or log domain circuit principle using bipolar transistors or MOSFETs in weak inversion [3]. As many biomedical signals manifest themselves at very low frequencies and thus require very large time constants, for an acceptable (integratable) capacitor value, the bias currents of the WF elementary building blocks, viz., the log domain integrators, need to be very low (in the pA range) and, as a consequence, are very difficult to generate precisely.

Trying to circumvent the pA current requirement, a G_m-C WF using very low gain triode MOS transconductors has been reported [4]. Although the problem of low bias currents indeed can be overcome by keeping the MOS transistors in their triode region, to provide accurate transconductance, a sophisticated bias generator and highly accurate transistor sizing are required as well as very long transistors to keep them in strong inversion at minute currents.

Recently, a sampled data WF using the switched current (SI) technique has been reported [5]. As a SI circuit relies on matching rather than on the presence of linear elements, an SI WF is expected to fit into standard digital CMOS technology and to be precisely controlled by the clock sampling frequency only [6]. At first glance from [5], the aforementioned problems (tradeoff between capacitor size and bias current) seem to be elegantly solved, but unfortunately, for low voltage low power designs, SI circuits suffer from the imperfections of CMOS switches; driven by a low voltage clock amplitude, the on resistances of the switches are large and cause distortion [7]. Furthermore, transient glitches are induced by the sudden change of operating voltages of the memory transistor [8]. Moreover, the realization of a multiple gain (output) SI accumulator, the elementary building block of SI filters, relies on the precision of transistor sizing and bias current scaling. These requirements are very difficult to meet simultaneously in circuits operating at very low current densities [9].

In this paper, a circuit technique employing weak inversion MOSFETs operating at very low current densities, coined as '*Switched Gain Cell*, SGC,' is introduced. Evolved from the SI technique, the SGC technique maintains the advantages of the SI technique (that does not require linear capacitors and transistor linearization) but eliminates the need for high precision transistor sizing and allows for electronic adjustability. Furthermore, by the SGC topology itself, the switching error induced by the switch can be simply compensated by using the technique recently reported in [10]. The SGC technique is then applied to a 5th-order gauss1 (1st derivative of the Gaussian function) WF. The WF is designed to be implemented in 0.13µm CMOS IC technology and to operate from a 1V single supply. The WF can be scaled by altering the clock frequency.

The conversion of a gauss1 impulse response in the time domain into a z-domain transfer function using the SVD approximation [11], in conjunction with the Schwarz form for state-space matrices [12], is presented in Section II. The result is a ladder filter structure that can be directly realized

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by the SGC circuit introduced in Section III. Simulation results of the SGC WF are presented in Section IV. Finally, the entire work will be summarized in Section V.

II. SAMPLED-DATA WAVELET FILTER

To synthesize a sampled-data WF, the wavelet base, defined in the time domain, first has to be converted into a z-domain transfer function and subsequently an appropriate state-space description (filter topology) has to be selected, employing delay cells as elementary building blocks. In this work, the gauss1, defined by $f(t) = -2t \cdot e^{-t^2}$, shifted by τ = 1.7, is employed as a wavelet base.

We first consider the following discrete time state space matrices

$$\begin{bmatrix} x_{(k+1)} \\ y_{(k)} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} x_{(k)} \\ u_{(k)} \end{bmatrix}, \tag{1}$$

where $u_{(k)}$, $y_{(k)}$ and $x_{(k)}$ and $x_{(k+1)}$ are the input, output and the present and advanced states of the system, respectively. A, B, C and D are the state, input, output, and direct matrices of the state space description, respectively. The impulse response of a state space system can be found from

$$h = \left[\cdots \quad 0 \quad 0 \quad 0 \quad \boxed{D} \quad CB \quad CAB \quad CA^2B \quad \cdots \right]^T. \tag{2}$$

The boxed entry denotes the instance at t = 0. To perform the SVD approximation, (2) has to be put into the form of a Hankel (H) matrix [11], such that

$$H = \begin{bmatrix} CB & CAB & CA^2B & \cdots \\ CAB & CA^2B & & \\ CA^2B & & \ddots & \\ \vdots & & & \end{bmatrix} = O \cdot K. \tag{3}$$

As can be seen from (3), the columns of H are shifted versions of the impulse response and the H matrix is a result of a multiplication of matrices O and K, where O is the observability matrix and K is the controllability matrix, respectively defined by

$$O = \left[C^T \quad A^T C^T \quad A^{T^2} C^T \quad \cdots \right]^T \text{ and}$$
$$K = \left[B \quad AB \quad A^2B \quad \cdots \right]. \tag{4}$$

Now, we can perform a singular-value decomposition (SVD) on the H matrix by applying $H = U \cdot \sum \cdot V^H$, where matrix $\sum$ is a diagonal matrix with the singular values arranged in decreasing order. The columns of U are the left singular vectors and the columns of V are the right singular vectors. In order to find a suitable compromise between the order of the system (and therefore the WF complexity, power consumption and chip area) and the accuracy of the approximation, matrix $\sum$ is truncated to a rank 5, resulting in a 5th order system. The O and K matrices can be calculated from the SVD respectively as $O = \hat{U} \cdot \hat{\Sigma}^{1/2}$ and $K = \hat{\Sigma}^{1/2} \cdot \hat{V}^T$, where, $\hat{U}$, $\hat{\Sigma}$, and $\hat{V}$ are the rank 5 approximations of the original U, $\sum$, and V matrices, respectively.

Next, we need to extract the A matrix of the state space description by dividing the O or C matrix in two separate parts and again dividing them to extract the A matrix. For example, we choose the O matrix as

$$O = \left[\overbrace{C \quad CA \quad CA^2 \quad \cdots \quad CA^{n-1}}^{O_x} \quad CA^n \right]^T = \left[C \quad \overbrace{CA \quad CA^2 \quad \cdots \quad CA^{n-1} \quad CA^n}^{O_y} \right]^T \tag{5}$$

We then have $O_x \cdot A = O_y$ and $A = O_x^+ \cdot O_y$, where O_x^+ indicates the pseudo-inverse of O_x. The B and C matrices can be simply found from the first row and first column of the O and K matrices, respectively. As the WF itself is a band-pass filter that does not have any direct transfer from input to output, we can set $D = [0]$.

Unfortunately, all matrices obtained from this approximation (except matrix D) are fully dense (i.e., have no zero entries), which means there is a high connectivity between the various blocks in the filter which adds to the complexity and induces additional noise and power consumption. To reduce the complexity of the filter topology, we convert the matrices into a Schwarz form [12] which yields a more compact filter structure as shown below.

$$A = \begin{bmatrix} -0.5229 & -0.3571 & 0 & 0 & 0 \\ 0.3571 & 0 & -0.1998 & 0 & 0 \\ 0 & 0.1998 & 0 & -0.1478 & 0 \\ 0 & 0 & 0.1478 & 0 & -0.0974 \\ 0 & 0 & 0 & 0.0974 & 0 \end{bmatrix} \tag{6}$$

$$B = [1 \quad 0 \quad 0 \quad 0 \quad 0]' \tag{7}$$

$$C = [0.1654 \quad 0.5111 \quad 0.589 \quad 2.68 \quad -0.5701]. \tag{8}$$

The sampled data WF structure and its impulse response obtained from the resulting state space description for a sampling frequency of 10 Hz are shown in Figs. 1a and 1b respectively. Compared to the ideal continuous-time gauss1 impulse response, this approximation provides a mean square error of only 0.41 %.

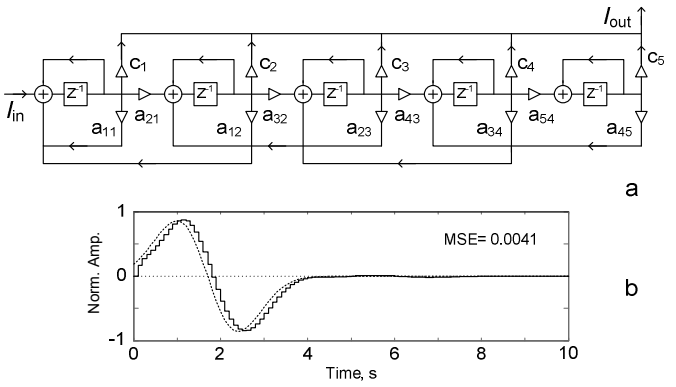

Figure 1. a) z-domain block diagram and b) Normalized impulse response

III. SWITCHED GAIN CELL TECHNIQUE

The basic idea of the SGC technique is shown in Fig. 2. Fig. 2a shows a transconductor-based current amplifier or current gain cell. In the case that the voltage-current relation of each transconductor is a monotonic function, described by

$$I_o = I_B f\left(V_+ - V_-\right) = I_B f\left(V_{\mathrm{id}}\right), \tag{9}$$

where I_B is a transconductor bias current, applying (9) to the circuit in Fig. 2a, we obtain

$$I_{\mathrm{out}} = I_{B2} f\left(V_{\mathrm{idB}}\right) = f\left(f^{-1}\left(\frac{I_{\mathrm{in}}}{I_{B1}}\right)\right) = \frac{I_{B2}}{I_{B1}} I_{\mathrm{in}}. \tag{10}$$

From (10), we can see that a current gain is obtained by a ratio of bias currents of identical transconductors A and B that can be either linear or nonlinear [14]. A half delay cell or track-and-hold circuit, the basic element of a sampled data filter, can be achieved by inserting switch S_1 as shown in Fig. 2b. When switch S_1 is closed, the voltage at the inverting node of transconductor A is connected to the non-inverting node of transconductor B and then it will be converted into I_{out} by (9) again. After opening S_1, the voltage at the non-inverting node of transconductor B is sustained by the parasitic capacitance at the noninverting node and the output current is held until the next clock phase. It should be noted here that the concept of a transconductor-based tuneable track-and-hold cell using linear transconductors has been previously reported under the name '*Switched Transconductor*' circuit [15]. As is evident from the circuit mechanism, there is no transconductor nor current being switched, but a gain cell, so we decided to give the more appropriate name '*Switched Gain Cell*' to this circuit.

Charge injection and clock feedthrough effects in MOS switches also affect the performance of the the SGC circuit. To reduce the switching error, the technique reported in [10] is applied to the SGC circuit, as shown in Fig. 3. Switch S_2, which is identical to S_1, is inserted at the inverting node of transconductor B. Therefore, the switching error voltage at the non-inverting node is almost completely cancelled by the error voltage created by S_2 at the inverting node.

The multiple outputs accumulator can be realized as shown in Fig. 4a. Two half-delay cells are cascaded and the output current is fed to the input summing node. All transconductors are identical and their gains can be adjusted by their bias currents. Therefore, contrary to SI circuits, the problem of transistor sizing does no longer play a role.

All transconductors in the SGC circuits can be replaced by a simple *tanh* transconductor. See Figure 4b. Biasing this circuit in weak inversion with a very low bias current I_B (nA range), its voltage to current relationship, that complies with (10), can be found to be $I_o = I_B \tanh(V_{\mathrm{id}}/2nV_T)$, where n is the sub-threshold slope factor [16]. In the z-domain block diagram of Fig. 1a, we can substitute the delay elements and the gain blocks, by the SGC integrator of Fig. 4a, to realize the current-mode WF. The resulting WF is shown in Fig. 5. The bias currents of each transconductor are set according to the coefficients in the state space matrices derived in Sec. II.

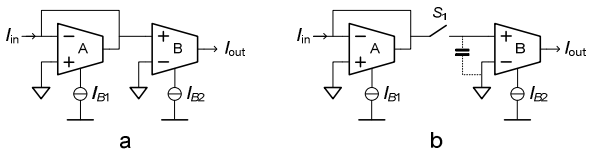

Figure 2. a) Current gain cell b) SGC memory cell

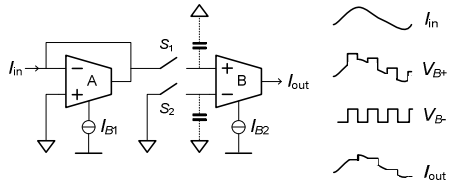

Figure 3. SGC memory cell with switching error compensation

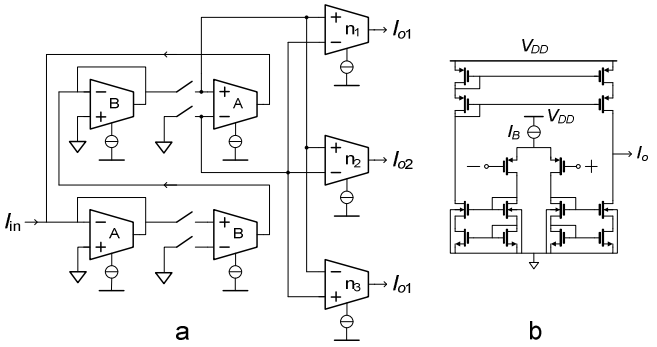

Figure 4. a) Multiple output SGC integrator b) Transconductor circuit

IV. SIMULATION RESULTS

The concept of the SGC circuit technique and the feasibility of using SGC circuits in WF filter design has been verified by Cadence simulations using RF spectre and 0.13 µm CMOS model parameters. The *tanh* transconductor of Fig. 4b was employed and the dimensions were set as 10µm/10µm and 3µm/3µm for the PMOS differential pair and all transistors in the cascode current mirrors, respectively. Table I shows the values of the bias currents of each transconductor in Fig.5. From a supply voltage of 1V, the filter consumes 467nW of static power.

The impulse responses of the WF of Fig. 5 using ideal linear transconductors and the *tanh* transconductors are illustrated by the gray and black lines, respectively, in Fig. 6. Due to channel-length modulation in the transistors in the transconductors, the waveforms are slightly different, both in magnitude and time. However, this minor error can be counteracted by slightly increasing the bias currents of G_A and G_B.

The wavelet (impulse response) can be scaled by adjusting the clock frequency. As shown in Fig. 9, when the clock frequency is adjusted from 0.25kHz to 2.5kHz, the scale of the wavelet is changed while its waveform is preserved. This paves the way to multi-resolution analysis using identical circuits to implement the scales.

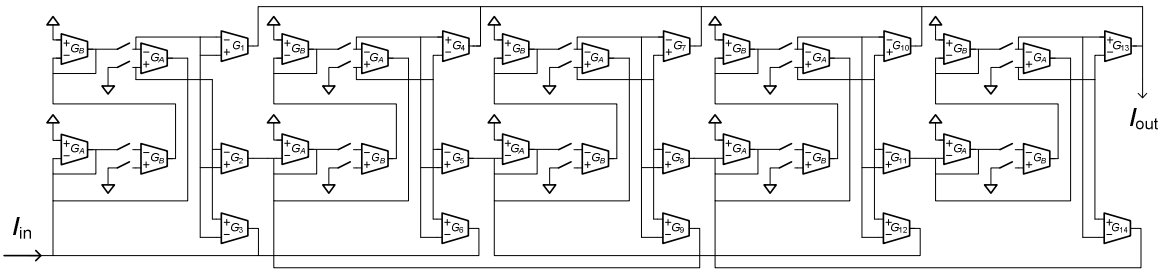

Figure 5. SGC wavelet filter

TABLE I. TRANSCONDUCTOR BIAS CURRENTS

TRANSCONDUCTOR	G_A , G_B	G_1	G_4	G_7	G_{10}	G_{13}	G_3	G_2, G_6	G_5, G_9	G_8, G_{12}	G_{11}, G_{14}
BIAS CURRENT (nA)	10	1.7	5	6	26.8	5.7	5.3	3.6	2	1.5	1

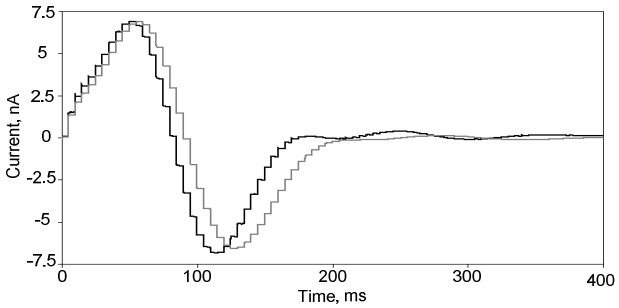

Figure 6. Impulse responses of the wavelet filters

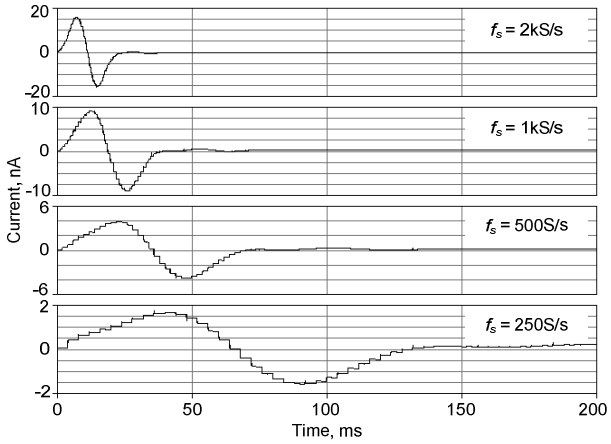

Figure 7. Impulse responses obtained from changing clock frequency

V. CONCLUSION

A current-mode sampled-data wavelet filter, obtained from combining the SVD approximation method with the SGC circuit technique has been introduced. The SVD approximation provides a compact z-domain filter structure while the SGC technique allows the realization of the filter using MOSFETs in weak inversion. The simulation results confirm that the WF operates well at very low current densities and the wavelet can be adjusted by changing the switching clock speed.

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