A UWB CMOS 0.13μm Low-Noise Amplifier with Dual Loop Negative Feedback

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***Abstract*— A Low-Noise Amplifier for ultra wide band (UWB) applications is presented. The use of a dual-loop negative feedback topology is advantageous, since it allows to achieve both impedance matching and a very low noise figure, and saves a lot of chip area as no bulky inductors are needed.**

A nullor and a resistive feedback network are employed, and the values of the feedback elements involved are defined in order to fulfill the noise-figure, input impedance and power-gain requirements for an UWB receiver. To ensure circuit stability, frequency compensation is done by means of a phantom zero and the addition of a transistor connected between input and output, thus realizing a *multipath* structure.

The design targets UMC 0.13μm CMOS IC technology and operation from a 1.2-volt supply. From circuit simulations, the power gain of the LNA amounts to 17dB, and the bandwidth spans up to 12GHz. S_{11} is below -10dB up to 10GHz and the noise figure is below 3dB up to 8GHz, and below 4dB@10GHz. The power consumption equals 14mA.

Compared to competitive solutions, using resonating load stages or LC ladder networks, this chip will be much smaller and cheaper; it will use standard CMOS technology, and achieve very low noise, high gain and wide band matching at reasonable power consumption.

I. Introduction

Ultra wide band (UWB) is one of the most promising approaches to radio communication due to its inherent ability of transmitting data over a wide frequency spectrum with high speed and low power. With these advantages, UWB can be used for imaging systems, vehicular and ground-penetrating radars and wireless communication systems. Especially for Personal Area Networks, it can provide wireless link connection at home and in the office instead of heavy cables with data rates of a few hundred megabits up to a few gigabits.

UWB communication poses big challenges for low-noise amplifier (LNA) design. Since the LNA is the first active component close to the antenna, it must provide sufficient low noise behavior not only at one frequency but over the whole UWB frequency band from 3.1 to 10.6GHz. The targeted noise figure is around 3dB, which is quite a challenging value compared to previously reported works. Power gain is another important parameter; S_{21} should be larger than 15dB[1].

Wideband impedance matching is another critical issue: the LNA has to be matched to 100Ω, the characteristic impedance of the antenna [1], so S_{11} should be below -10dB over the entire frequency band. At the same time, we need to ensure that the matching network will not destroy the noise performance and waste chip area. Some LNA designs by other UWB groups in the world [2] employ LC ladder networks. However, an inductor is a costly component since it consumes most of the chip area and also introduces large parasitic resistances that will increase noise. Power consumption is another consideration: our goal is to limit the current consumption to less than 15mA. The IC technology we target is UMC (United Microelectronic Corporation) 0.13μm CMOS.

[1]In a usually matched system, the transducer power gain equals $|S_{21}|^2$

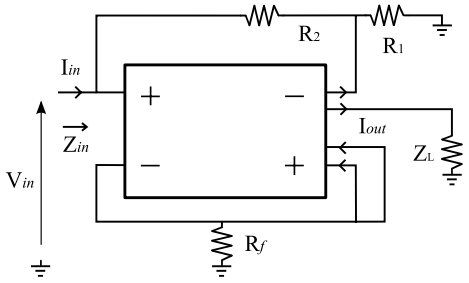

Fig. 1. Dual loop indirect negative feedback power-to-current amplifier (basic configuration).

Since our design is based on negative feedback, it will benefit from technology advancements, leading to a larger loop gain and hence a larger bandwidth and a lower power consumption.

The paper is organized as follows: in Section II, we will discuss the dual-loop feedback topology chosen for the LNA and will define the feedback network according to our specifications. In Section III a nullor implementation with optimized performance and relevant simulation results will be presented. A comparison between our work and previously reported wideband amplifiers will be given in Section IV.

II. LNA Topology

To achieve accurate input impedance matching, two feedback loops are used: a voltage-to-current (V-I) feedback loop and an indirect current-to-current (I-I) feedback loop, as shown in Fig. 1.

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The reason why this topology is called "indirect feedback" is because the I-I feedback does not sense the output directly, but in an indirect way, by means of a replica of the output current: the final circuit has got two inputs and four current outputs. Of the two negative outputs, one is fed back to the input, while the other is fed to the load; the two positive outputs are put in parallel and fed back to the input after being converted to a voltage.

For the V-I loop, it holds:

$$\frac{I_{out}}{V_{in}} = -\frac{1}{2R_f} \tag{1}$$

For the I-I loop, the current gain can be expressed as:

$$\frac{I_{out}}{I_{in}} = -\frac{R_1 + R_2}{R_1 + 2R_f} \tag{2}$$

where R_f represents the V-I feedback resistor and R_1, R_2 are the current divider resistors. Hence, the input impedance can be defined as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{I_{out}}{I_{in}}\frac{V_{in}}{I_{out}} = \frac{R_1 + R_2}{R_1 + 2R_f} \cdot 2R_f \tag{3}$$

By proper selection of the feedback resistors, appropriate values for input impedance, power gain and noise figure can be designed. In fact, under the condition of sufficient input impedance match, it can be derived:

$$|S_{21}|^2 = \frac{P_{out}}{P_{in}} = \frac{I_{out}}{I_{in}}\frac{I_{out}}{V_{in}}Z_L = \frac{R_1 + R_2}{R_1 + 2R_f}\frac{1}{2R_f}Z_L \tag{4}$$

Z_L being the load impedance, usually equal to 50Ω. The resistors in the two feedback loops will contribute noise and have influence on the noise transfer. After shifting and combining all the noise sources, we arrive at the following expression for the total noise voltage power spectral density:

$$\begin{aligned} S_{v_n,eq} &= 4kTR_{n,s} + |R_s + R_f|^2 S_{i_n} + |1 + \frac{R_s}{R_2}|^2 S_{v_n} \\ &\quad + 4kT\frac{R_s^2}{R_2} + 4kTR_f \end{aligned} \tag{5}$$

where S_{v_n} and S_{i_n} are the equivalent power of the voltage and current noise sources of the first stage of the nullor; $R_{n,s}$ is the noise resistance of the UWB antenna, approximately equal to antenna resistance R_s, 100Ω in our case, instead of the usual value of 50Ω. As it can be seen from Equation 5, if the value of R_f is decreased and the value of R_2 increased, the total noise power spectral density will be reduced. So in order to achieve low noise, R_f must be chosen as small as possible and R_2 as large as possible. However, some practical limitations arise. For instance, if R_f is too small, for the same input signal, more current needs to be delivered, which is likely to cause clipping distortion as the available current from the supply is limited. Based on simulation results $R_f = 5\Omega$, $R_2 = 910\Omega$ and $R_1 = 90\Omega$ have been found to offer a good compromise. The resulting values for power gain and noise figure will be shown in Section IV.

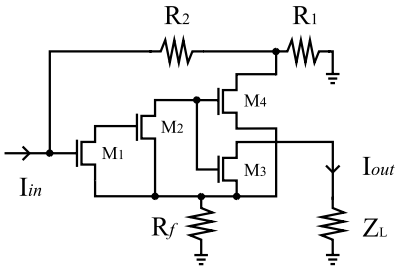

Fig. 2. Dual loop indirect negative feedback power-to-current amplifier (circuit diagram, biasing not included).

III. Nullor Design

The nullor is the critical part in our design, since parameters such as bandwidth, noise figure, distortion, will all depend on how good the nullor implementation is. For proper design of the first stage of the nullor, its noise performance is of prime importance. Furthermore, a high gain is required to suppress noise from other stages. Generally, a nullor comprises at least two stages (an input stage and an output stage), but in order to increase the loop gain and bandwidth, we can add more intermediate stages. Each stage will add gain and a dominant pole, so if more than three stages are used, frequency compensation will become very difficult, compromising the stability of the circuit.

Fig. 2 shows the circuit diagram of the nullor, which is composed by three stages, described in subsections *A* and *B*: the input stage realized by transistor M_1, the intermediate stage (transistor M_2) and the double output stage (transistors M_3 and M_4). In order to get a large gain, all stages are realized through common-source (CS) transistors. Additional stages used to obtain frequency compensation will be described later in subsections *C* and *D*.

A. Input Stage

The noise contribution of the active part of the LNA is minimized by optimizing the input stage of the nullor, i.e. defining geometry and bias current of its input transistor. Since the noise figure of the LNA reduces when the drain bias current I_d of the first stage increases, in order to minimize the noise, I_d should be chosen as large as possible. Trading off noise figure for power consumption, we choose 4mA for the drain current of the first stage (transistor M_1). Since the gain of a transistor is proportional to its g_m, which, in strong inversion, in turn is proportional to W/L, W being the width of the transistor and L its length, we choose the minimum feature size 0.12μm for L. In weak inversion, the g_m of the transistor no longer depends on its width and as the parasitic capacitances still do, the gain of the transistor reduces again for increasing widths. As a consequence, the NF increases again. As a compromise, we choose W=100μm.

B. Intermediate and Output Stage

For the two indirect output stages (transistor M_3 and M_4), like for the input stage, in order to have a large gain, we use

CS stages. The width of each transistor equals $W = 100\mu$m; their bias current equals 3.5mA. To increase the loop gain, we add one intermediate CS stage, transistor M_2, whose width W is equal to 100μm and bias current equal to 3mA.

C. Frequency Compensation

Employing phantom zeros is an efficient way to do frequency compensation [3]: their characteristic property is that, though implementing a zero in the loop gain, they are not present in the system transfer function. Phantom zeros are mostly placed near the band edge. Hence, their influence on noise and distortion is only noticeable beyond the band of interest. The zero is either realized in the feedback network, or at the input or at the output. For three stages, in order to do proper frequency compensation, two phantoms zero are required or one phantom zero and an additional frequency compensation measure. From hand calculations and circuit simulations, employing a phantom zero at the input or at the output proves to be ineffective. Since the LNA has two feedback loops, we thus have to implement any phantom zero in both loops. As the feedback element of the V-I loop is a resistor (R_f), we can only implement one phantom zero in the feedback path, by means of a series inductor. For the other (current) feedback loop, we implement the (same) phantom zero by means of a capacitor in parallel with R_2. Final values for these two components are set from simulations to: C_{comp}=50fF, L_{comp}=65pH.

D. Multipath Structure

Since, in general, two frequency compensation measures are required to compensate a third-order feedback system, next to the phantom zero, we need an additional measure. To this end, pole splitting, pole-zero cancelation or resistive broadbanding can be used [3]. Another technique, which turned to be very adequate for the proposed double-loop negative feedback power-to-current amplifier, is by adding an additional transistor connected between input and output, as in Fig. 3 (transistors M_5 and M_6, one transistor each feedback loop). We now obtain a *multipath* structure, composed by the parallel connection of the three-stage path discussed so far, and the additional common-gate stages, whose frequency responses have a dominant pole which lies at a much higher frequency than the dominant poles of the three stage path.

The parallel of the two signal paths operates as follows. At low frequencies the loop gain is delivered by the parallel of the two paths: as the gain of the three stage path is much larger, the loop gain is still mainly determined by this one. On the contrary, the additional stage is effective at higher frequencies, where the multipath transistor takes over, increasing the phase margin, thus ensuring stability.

IV. Simulation Results

The final circuit diagram including biasing scheme, first-order models for the bondpad (bp), bondwires (bw) and antenna, is shown in Fig. 4. Biasing is realized employing three additional coupling capacitors, C_c, a biasing shunt resistor

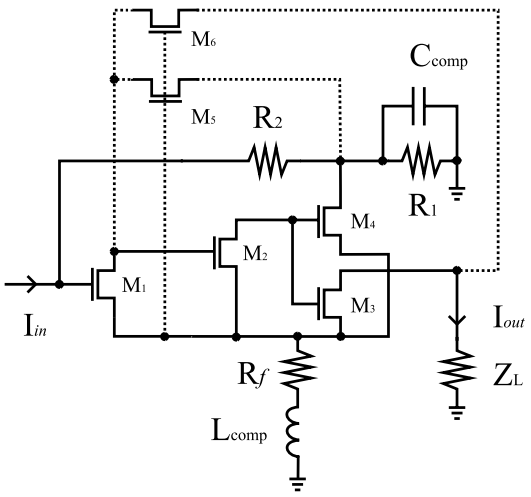

Fig. 3. Amplifier signal diagram employing phantom zeros and multipath structure.

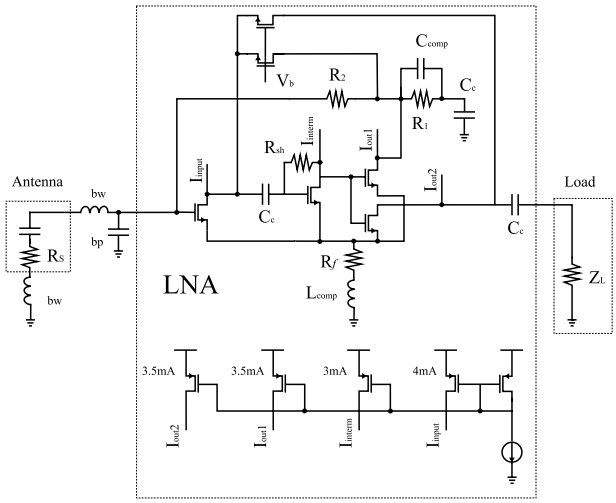

Fig. 4. Final circuit with biasing.

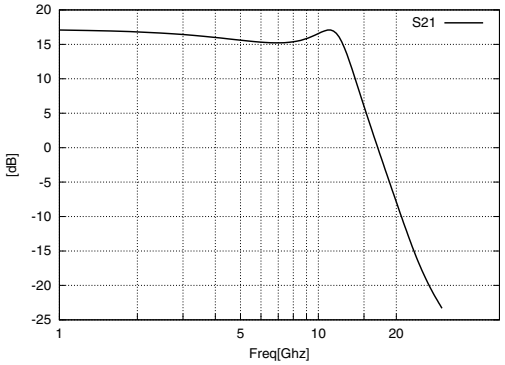

Fig. 5. Forward transmission coefficient S_{21}.

TABLE I
COMPARISON WITH RECENTLY REPORTED STATE-OF-THE-ART UWB LNA

	Tech.	S_{11}[dB]	S_{21}[dB]	B[GHz]	NF_{min}[dB]	Power[mW]	$IIP3$[dBm]
This work	0.13 CMOS	< -10	17	3-12	2@5GHz	16.8	-15.6@7GHz
[2]	0.18 SiGe	< 9.6	21	2.2-8	2.5@5GHz	30	-1@5GHz
[4]	0.13 CMOS	-	16.5	2.2-10.6	2@5GHz	9	-5.1@8GHz
[5]	0.18 SiGe	< -9.9	9.3	2.6-11.7	4@6GHz	9	-15@6GHz
[6]	0.25 SiGe	-	10	4-6	4.5@5GHz	3.5	-10@5GHz
[7]	0.18 SiGe	-	20.3	0.1-13.6	1.8@6GHz	26	2.1@6GHz
[8],[9]	0.18 CMOS	-	8.5	2.8-10.8	4.4@10GHz	4.5	8.3@10GHz

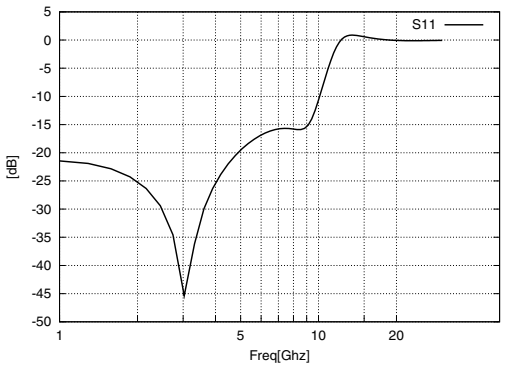

Fig. 6. Input reflection coefficient S_{11}.

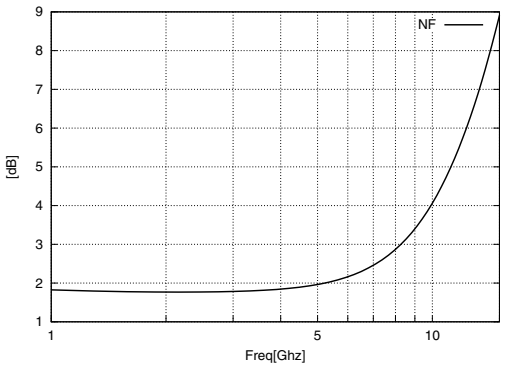

Fig. 7. Noise Figure.

R_{sh}, a voltage source V_b and a simple current mirror with multiple current outputs, fed to the four transistors in the third-order path; the two multipath transistors are biased at $I_{\rm out1} - I_{\rm interm}$ each. The total bias current through the input stage equals $I_{\rm input} + 2(I_{\rm out1} - I_{\rm interm})$.

From circuit simulations, the following results are obtained: the bandwidth spans up to 12GHz, $S_{21} = 17$dB, $S_{11} < -10$dB up to 10GHz, NF<3dB up to 8GHz and NF<4dB at 10GHz and IIP3=-15.6dBm . Figures 5, 6 and 7 show the forward transmission coefficient, S_{21}, the input reflection coefficient, S_{11} and the noise figure, NF, as a function of frequency. In Tab. I, a comparison with previous UWB LNA designs is made. We can state that our work is one of the most advanced LNA solutions for UWB applications due to its wide-band features.

V. CONCLUSION

An ultrawideband dual-loop negative-feedback low-noise amplifier to be implemented in UMC 0.13μm CMOS technology has been presented. Its power gain equals 17dB over a bandwidth up to 12GHz with a noise figure smaller than 4dB. S_{11} is below -10dB from very low frequencies up to 10GHz. Since the supply voltage is 1.2V and the total current consumption is 14mA, the power consumption equals 16.8mW.

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