Companding Baseband Switched Capacitor Filters and ADCs for WLAN Applications

(Invited Paper)

Vaibhav Maheshwari, Wouter A. Serdijn, John R. Long
Electronics Research Laboratory, Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology, Mekelweg 4, 2628 CD, Delft, The Netherlands
Emails: {v.maheshwari, w.a.serdijn, j.r.long}@ewi.tudelft.nl

***Abstract*— In this paper, system level design techniques for companding baseband switched capacitor (SC) filters for WLAN applications are presented. With companding, no AGC is required in front of the filter. A filter prototype is designed for 802.11g receiver and simulation results show that, with careful design of the opamps, a total harmonic distortion of less than 0.5% can be achieved. A new type of companding ADCs along with the algorithm to achieve companding in ADCs is proposed. It is shown that companding by a factor of 4 reduces the power consumption of the SC filter by a factor close to 4 times for a given dynamic range whereas it directly results in 12 dB reduction in the dynamic range requirement of the following ADC.**

I. Introduction

Low power and low cost designs are essential for the success of future portable wireless applications. With the advancement in CMOS technology and the demand for higher integration, it is imperative to design precision analog blocks that can coexist with digital ones on the same die at low supply voltages. Analog baseband filters are one of the key components used in wireless receivers for channel selection, i.e. to reject out of band signals before analog-to-digital (A/D) conversion. This relaxes the dynamic range (and therefore resolution) and speed requirements of the A/D converter (ADC), which would otherwise have to oversample the entire input signal containing large interferers. These analog filters have to maintain a minimum Signal to Noise plus Distortion Ratio (SNDR) required by the specifications and on top of that they have to incorporate the often high dynamic range of the input signal to be processed. Thus, filters with very high dynamic range and high selectivity need to be designed, which necessitates high power consumption and large chip area [1].

A common way to relax the dynamic range requirements of the analog filter is to use AGC (Automatic Gain Control) in front of the filter. AGC works on the principle of adapting the receiver to the strength of the signal being received. However, since most wireless receivers are subject to the presence of interferers during minimum desired signal reception, it limits the allowable AGC gain in front of the filter. Therefore, the AGC operation is distributed throughout the filter, further amplifying the signal as interferers are attenuated [1]. This helps in reducing the power consumption of the later stages of the filter but the power consumption of the former stages is still high. Also, in digital communication systems, the AGC settings of the receiver are set during the preamble or the midamble of the data frame. Once the gain settings are set, they are not disturbed for the rest of the frame even though the signal reception might change. This mandates extra leeway in the dynamic range of the filter, which in turn implies that finer AGC gain settings should be used. This may lead to a longer settling time of the AGC loop, which in many applications is not acceptable. For instance, in WLAN 802.11a/g systems using OFDM modulation the settling time for the AGC loop is quite small ($< 6\ \mu$s) [2]. Thus, only coarse gain settings can be used and that too mainly after the filter and before the ADC [3]. Moreover, OFDM systems have a high peak-to-average power ratio (PAPR), which further increases the dynamic range requirements. Significant power dissipation savings can be obtained if gain settings could be changed dynamically while the filter is in service. To this end, some techniques have been reported in literature [1][4][5].

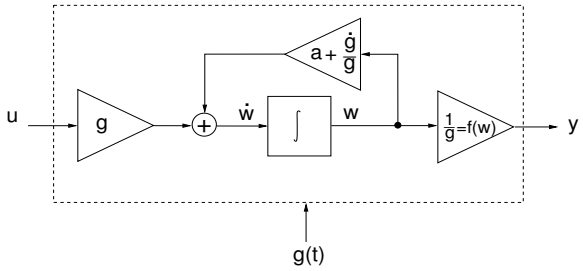


Fig. 1. Companding lossy integrator.

In [4], it is shown that companding can be used to achieve high dynamic range analog filters with low power consumption. Two possible SC implementations of companding filters are discussed in [5]. In this paper, we present system level design techniques for companding baseband SC filters with simulation results for WLAN 802.11g receiver. We also extend the concept of companding to ADCs, where with the help of digital post-processing, significant improvement in dynamic range of the combined companding baseband filter and ADC can be achieved. The following sections deal with the details.

II. Companding Switched Capacitor Filter Implementation

Companding systems generally include an input gain element, a signal processor and an output gain element. The input gain element compresses the high dynamic range input signal, which is then processed by the low dynamic range signal processor followed by expansion using the output gain element. In order for the output of the signal processor not to be disturbed by dynamic modifications of the gain at the input end, one must control the system's state variables accordingly [6]. Fig. 1 shows the block diagram of a companding lossy integrator (lossless for $a = 0$, where $a \leq 0$ is a fixed feedback gain factor) [4]. Here, the state variable $w(t)$ is defined as

$$w(t) = g(t)x(t). \tag{1}$$

where $x(t)$ is the output of the integrator without companding, i.e. when $g(t) = 1$. Since integrators are the main building blocks and power horses of analog filters, the gain function $g(t)$ can be used to achieve compression at the output of each integrator and thus it would

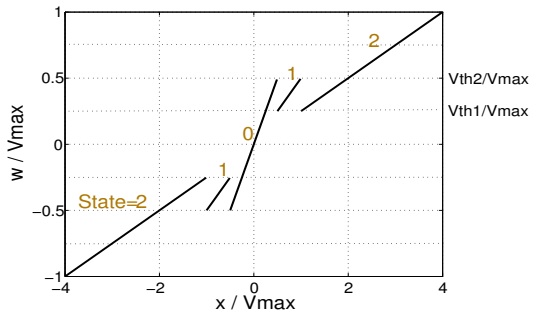


Fig. 2. Mapping from x to w.

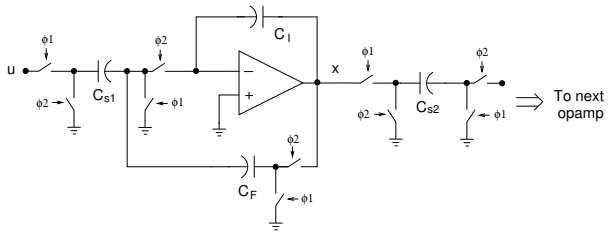
help reduce the required dynamic range and power consumption of the filter. A practical implementation of companding filters can be achieved by using a piecewise-constant gain function g and SC integrators [5]. In this case, the $\dot{g}/g$ term in the feedback block of the integrator shown in Fig. 1 can be implemented by state variable updating given by the relation [4]:

$$w(t_k^+) = w(t_k^-)\,\frac{g_k}{g_{k-1}}. \tag{2}$$

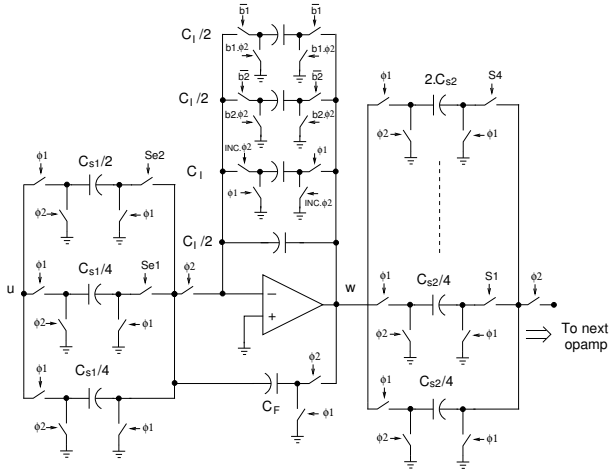
In the above equation, k is used as an index to represent different values of g that appear in time, t_k is the time instant at which the value of g changes and $w(t_k^-)$ and $w(t_k^+)$ denote the limit of $w(t)$ as time t approaches t_k from left and from right respectively. Fig. 2 shows an example of x to w mapping used in this paper, in which the consecutive values of g (1, 1/2, 1/4) differ by a factor of 2 [5]. We define three states 0, 1 and 2 by the variable *State* corresponding to the values 1, 1/2 and 1/4 of g respectively. In such a case, the updating of state variable w amounts to either doubling it or halving it whenever there is a change in g. Comparators are employed to detect the crossings of w through the thresholds (V_{th1} and V_{th2} in Fig. 2, where $V_{th1} < V_{th2}/2$ to avoid instability) and change g accordingly. Note that in Fig. 2, threshold V_{th2} is lower than the maximum allowable value V_{max} that could saturate the output of the opamps. The choice of these thresholds should be made carefully as will be explained later.

A companding filter using a piecewise-constant function g can be easily implemented using SC integrators. Fig. 3(a) shows the parasitic insensitive SC Lossy Discrete Integrator (Lossy DI). Let ϕ_1 and ϕ_2 be the two non-overlapping clock phases. The input signal is sampled in phase ϕ_1 during which the output of the opamp remains constant. During phase ϕ_2, the charge from the sampling capacitor C_{S1} is transferred to the integrating capacitor C_I. Fig. 3(b) shows the Lossy DI along with state variable update circuitry used to double and half the output voltage depending on whether g increases or decreases by a factor of 2 respectively [5]. An array of capacitors is used at the input and the output for gain scaling. The integrator in Fig. 3(b) is shown as the first stage of the filter. The capacitor array at the output of one stage is combined with the array at the input of the following stage to form a single array, which is controlled using the logic signals S_1, S_2, S_3 and S_4 derived from both the stages.

Since the output of the opamp is held fixed in ϕ_1, the comparison of the state variable w is done in ϕ_1 and the signals b_1, b_2, *INC*, $Se1$, $Se2$, S_1, S_2, S_3 and S_4 are switched after ϕ_1 ends but before the integrating phase ϕ_2 starts. This is possible since non-overlapping clocks are used and complete switching is accomplished between the two phases ϕ_1 and ϕ_2. In this way, the circuit is prepared for



(a)

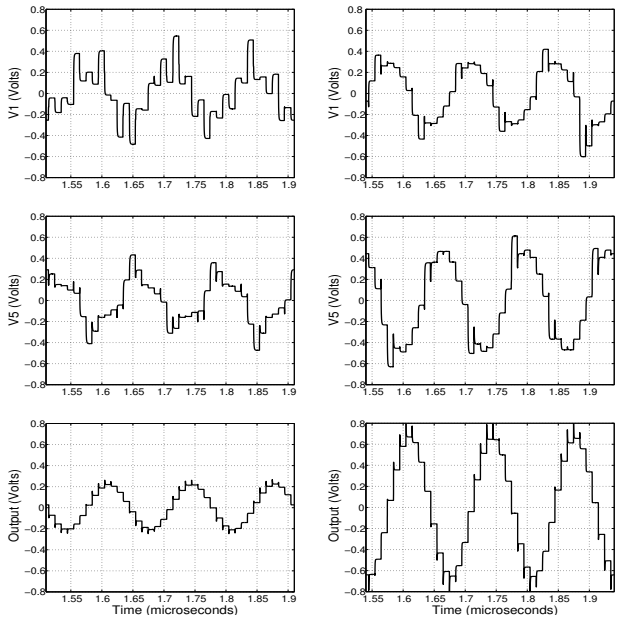


(b)

Fig. 3. Example of (a) SC Lossy Discrete Integrator, (b) Companding SC Lossy Discrete Integrator.

the following ϕ_2 and not the next ϕ_2 as presented in [5]. This is done to avoid any loss in the dynamic range due to voltage jumps in consecutive cycles of ϕ_1. This is explained as follows. In SC filters, when a signal with a high amplitude and at a frequency close to the filter cut-off frequency is applied to the input, the jumps between the output voltages of the opamps in consecutive cycles of ϕ_1 can be very high, especially in *State* 0 when there is no compression. For example, the output voltage of the opamp can be less than but close to V_{th2} in one cycle of ϕ_1. In the next cycle of ϕ_1, it can jump to a much larger voltage before a decision to compress the signal is made. Therefore, threshold V_{th2} should be made lower than V_{max} to accomodate such a signal step. If, after comparison in ϕ_1, the compression is made in the next cycle of ϕ_2, the output of the opamp would jump to an even larger value. To this end, an even lower threshold V_{th2} should be chosen. Although the signal is allowed to go beyond threshold V_{th2} in the final *State* 2 as shown in Fig. 2, part of the dynamic range may be compromised because noise puts a lower limit to the minimum value of V_{th2} that can be used. Since the filter noise is fixed based on the minimum required sensitivity, it should be ensured that V_{th2} is high enough such that compression caused by either the interferer or the desired signal does not bring down the desired signal to below signal sensitivity levels. Thus, the minimum value of V_{th2} may put a limit on the maximum amplitude of the signal that the companding filter can accomodate without saturating any of the opamps.

An alternative solution could be to increase the oversampling ratio



(a) (b)

Fig. 4. Waveforms at the output of first, last and expansion stage of the companding filter when (a) $G_{RF} = 25$ dB and (b) $G_{RF} = 0$ dB.

of the SC filter so that the signal is sampled faster and thus, the voltage jumps would be smaller. Also, having a higher oversampling ratio eases the anti-aliasing requirements of the prefilter. However, a faster clock increases the power consumption and also makes the design of switches challenging to achieve low distortion, especially at high input frequencies. A higher clock frequency can also make the value of the sampling capacitors (C_{S1} and C_{S2} in Fig. 3(a)) very small making it unrealistic to realize the array of capacitors in Fig. 3(b) on chip. So, there is a trade-off between the oversampling ratio and the dynamic range of the companding filter after the threshold V_{th2} cannot be further lowered. Even if a higher sampling ratio is allowed, as a design strategy, the value of V_{th2} should be chosen as close to its minimum value so that the voltage jumps in the characteristic of Fig. 2 do not affect the slew rate requirements of the opamps.

III. WLAN Receiver Design and Simulation Results

WLAN applications require the receiver to accomodate a wide range of input signal [2]. In order to ease the linearity requirements of the RF front-end, two switchable gain modes of 0 dB and 25 dB are assumed in the RF front-end. The baseband filter is implemented as a fifth-order, 0.1 dB in-band ripple Chebyshev low pass ladder filter using SC integrators. The cut-off frequency is fixed at 10 MHz. The oversampling ratio of the SC filter is chosen as 10 so that the sampling clock frequency is 100 MHz. Since, for more than 90 MHz offset from the carrier frequency the signals at the antenna will be out-of-band, they will get attenuated in the RF front-end. Thus, a single order baseband prefilter is sufficient to achieve anti-aliasing requirements for the following SC filter. We chose the fixed gain of the prefilter as 18 dB such that neither strong in-band signals nor interferers saturate the output of the prefilter. Similarly, the fixed gain of the first stage of the SC filter is chosen as 12 dB taking into

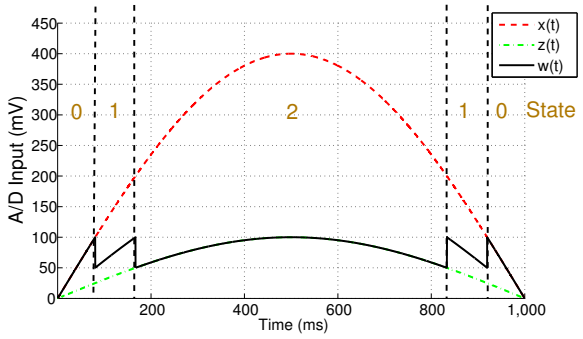


Fig. 5. Waveforms $x(t)$, $w(t)$ and $z(t)$

account the extra dynamic range achieved with companding.The filter is implemented in differential structure using ideal opamps with DC gain of 80 dB, gain-bandwidth product of 700 MHz and slew rate of 100 V/μs. The switches are implemented as CMOS transmission gates using 1.2 V, 0.13 μm CMOS technology with boosted clocks. The total harmonic distortion is 0.2% due to the non-idealities of the switches alone. Fig. 4 shows the differential output of the filter at the first stage, last stage and after expansion when it is excited by a sinusoidal input at a frequency of 7.5 MHz in the presence of two in-band interferers at 25 MHz and 50 MHz [2]. Fig. 4(a) is for the case when RF front-end gain, G_{RF}, is set to 25 dB and Fig. 4(b) for the case when it is 0 dB. In both cases, the desired signal is applied at maximum power.

IV. Companding A/D Converters

Further power savings can be obtained by removing the expansion gain stage at the output of the companding filter and directly feeding the compressed, low dynamic range output signal to the ADC. The signal expansion can be done in the digital domain using digital post-processing. Also, in this case, only a coarse AGC before the ADC is required. Such a scheme is presented in this section.

The dynamic range of the ADC DR_{ADC} is calculated as:

$$DR_{ADC} = SNR_{DEM} + DR_{SIG} + DM \quad (3)$$

where SNR_{DEM} is the SNR requirement of the demodulator that follows the ADC and DR_{SIG} is the signal dynamic range in front of the ADC which is determined by the receiver structure and gain control scheme. A design margin (DM) of 4 to 10 dB is commonly applied in the design of ADCs for wireless receivers to accommodate sudden variations in the received signal strength. Companding can significantly reduce DR_{ADC}. Let $x(t)$ be the uncompressed sinusoidal input signal to the ADC and $w(t)$ be the compressed signal given by equation (1), where $g(t)$ is the time varying gain ($0 < g \leq 1$). Let g_{min} be the minimum gain used during one half cycle of the signal, i.e. $g_{min} = g(t)$ when $|w(t)|$ reaches its peak in each half cycle. We consider a hypothetical signal $z(t)$ defined by $z(t) = x(t).g_{min}$ during each half cycle. Let the maximum voltage that $w(t)$ and $z(t)$ can take be V_{FS} – the full-scale voltage of the ADC used. Ideally, the ADC should receive the input signal $z(t)$ but instead now it receives $w(t)$. The ADC digitizes the signal $w(t)$ and the output is mapped to the correct bits that would have been obtained from $z(t)$ if it were digitized by the same ADC. The algorithm is explained as follows.

Let $W(n)$, $Z(n)$, $g(n)$ be the values of $w(t)$, $z(t)$ and $g(t)$ at time $t = nT$ respectively, where T is the sampling period of the N-bits ADC. We define another gain term $g_i(n) = g(n)/g_{min}$. The

size of the least significant bit (LSB) is denoted by $\Delta = V_{FS}/2^N$. Let $W_d(n)$, $Z_d(n)$ and $\widehat{Z}_d(n)$ denote the quantized voltages of $W(n)$, $Z(n)$ and $W_d(n)/g_i(n)$ respectively. We have the following equations:

$$W(n) = W_d(n) + \epsilon_1(n),\ -\frac{\Delta}{2} \leq \epsilon_1(n) < \frac{\Delta}{2} \quad (4)$$

$$\begin{aligned} Z(n) &= \frac{W(n)}{g_i(n)} \\ &= \frac{W_d(n)}{g_i(n)} + \frac{\epsilon_1(n)}{g_i(n)} \\ &= \widehat{Z}_d(n) + \epsilon_2(n) + \frac{\epsilon_1(n)}{g_i(n)}, |\epsilon_2(n)| \leq \frac{g_i(n)-1}{g_i(n)}\frac{\Delta}{2} \end{aligned} \quad (5)$$

where $\epsilon_1(n)$ and $\epsilon_2(n)$ are the quantization errors associated with $W(n)$ and $W_d(n)/g_i(n)$ respectively. The absolute maximum value of the sum of last two quantization error terms in (5) is bounded by $\Delta/2$. Therefore, we have

$$\widehat{Z}_d(n) = Z_d(n) \quad (6)$$

Thus, we can obtain the correct digital output corresponding to $z(t)$ signal. The above algorithm can be easily illustrated with the following example. Fig. 5 shows the waveforms $x(t)$, $w(t)$ and $z(t)$. To illustrate, we consider 3-bits ADC with threshold voltages for the positive cycle as 0, 25, 50 and 75 mV. The bits (000), (001), (010) and (011) correspond to analog voltages 12.5, 37.5, 62.5 and 87.5 mV respectively. The initial value of $State$ is 0. Using equations (4) and (5), we obtain the following mapping of output bits shown in Table I to do expansion in digital domain:

TABLE I
MAPPING OF ADC OUTPUT BITS DEPENDING ON $State$ AND g_{min}

State	$g_{min} = 1/4$	$g_{min} = 1/2$	$g_{min} = 1$
0 ($g = 1$)	(000, 001) → (000) (010, 011) → (000)	(000, 001) → (000) (010, 011) → (001)	no change
1 ($g = 1/2$)	(010, 011) → (001)	no change	—
2 ($g = 1/4$)	no change	—	—

As can be seen, the mapping is very simple and can be easily accomplished in the digital domain.

It can be estimated that companding by a factor of 4 should result in reduction in power consumption of the SC filter by 4 times for a given dynamic range [5]. However, the control circuitry, the comparators and the output expansion amplifier consume extra power and reduce the power savings achieved by companding. Since, using companding ADC with SC filter excludes the use of output expansion amplifier, and the control circuitry including the comparators consume only a fraction of the power consumption of the opamps, companding results in power reduction by at least 2 times and it can be close to 4. Additional power savings are achieved in the ADC, whose dynamic range requirement is reduced by 12 dB, without incurring any major penalty since the expansion is done in the digital domain. Besides, as estimated in [5] companding SC filter occupies lesser chip area as compared to a conventional linear filter designed for the same dynamic range.

V. CONCLUSION

In this article, companding is proposed as an alternative technique to AGC, which is normally used in front of the baseband filter in wireless receivers to reduce the power consumption. System level design techniques for companding switched capacitor filters are discussed and simulation results are presented for WLAN 802.11g receiver. An algorithm for companding ADCs is presented using which, companding switched capacitor filter can be combined with ADC to achieve significant improvements in dynamic range and power consumption.

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