

DCS1800/WCDMA ADAPTIVE VOLTAGE-CONTROLLED OSCILLATOR

Aleksandar Tasić, Wouter A. Serdijn and John R. Long

Delft University of Technology, Faculty of EEMCS
Electronics Research Laboratory
Mekelweg 4, 2628 CD Delft, The Netherlands
Phone: +31 (0)15 278 9423 Fax: +31 (0)15 278 5922
E-mail: a.tasic|w.a.serdijn|j.r.long@its.tudelft.nl

ABSTRACT

The ever-increasing demands for telecom services that require a higher cellular capacity and a higher data rate have pushed the wireless industry towards the development of wide-band, third-generation wireless systems. On the other hand, as there is a number of applications that are comfortably served by second-generation systems, for maximum functionality, reduced cost and power consumption, the integration of both second and third generation cellular systems should be the ultimate goal. Accordingly, an adaptive 2G/3G voltage-controlled oscillator (VCO) is described in this paper. For the DCS1800 operation, it achieves better than -133dBc/Hz phase noise at 3MHz offset from a 1.8GHz oscillating frequency at power consumption of 6mW as well as better than -120dBc/Hz phase noise at 3MHz offset from a 2.2GHz oscillating frequency while consuming 1.5mW for the WCDMA standard. By adapting the bias current, a phase-noise tuning range ($PNTR$) of more than 11dB can be realized, with more than a factor of four reduction in power consumption.

1. INTRODUCTION

As third-generation cellular systems are launched, there will be an increasing demand for multi-mode terminals which will allow access to different systems, providing various services. The coexistence of second and third generation cellular systems will require multi-mode, multi-band, multi-standard mobile terminals. The motivation is to share as many receiver building blocks as possible, without degrading the performance compared to single-standard receivers.

However, so far, multi-standard terminals have not progressed further than switching among different pieces of hardware, being either different circuits or entirely different front-ends. Indeed, this approach is simpler to implement, but is neither optimal in cost nor in power consumption [1]. Therefore, without adapting transceiver circuits to different operating conditions/standards, the idea of multi-standard front-ends will not pay off.

In line with this reasoning, an adaptive 2G/3G voltage-controlled oscillator, meant for a dual-standard adaptive front-end, is described in this paper. The VCO with a resonant-inductive degenerated tail-current source satisfies all the systems requirements in both the 1.8GHz DCS1800 and the 2.2GHz WCDMA frequency band. The oscillator achieves phase noise better than -133dBc/Hz at 3MHz offset from a 1.8GHz oscillating frequency and phase noise better than -120dBc/Hz at 3MHz offset from a 2.2GHz oscillating frequency at power levels of 6mW and 1.5mW, respectively. By adapting the bias current, a required phase-noise tuning range of more than 11dB is achieved, with up to four times possible reduction in power consumption.

The paper is divided into five sections. The concept of frequency adaptivity is described in Section 2. A design procedure for an 11dB phase-noise adaptive voltage-controlled oscillator is outlined in Section 3. Simulation results are presented in Section 4, while the conclusions are summarized in Section 5.

2. FREQUENCY ADAPTIVITY

The chosen quasi-tapped bipolar VCO [2], shown in Figure 1, beneficially uses the advantage of an increased voltage swing over the LC tank, while at the same time the transistors of the oscillator's active part remain far from heavy saturation. What is more, the freedom of choosing the base-biasing to be lower than the corresponding supply voltage allows for an even larger swing over the tank, fairly approaching the CMOS VCO performance in this respect. The oscillator consists of a resonating LC tank and a cross-coupled transconductance amplifier as the active part. Here, L stands for the tank inductance, C_V for the varactor capacitance, C_{SW} for the switched capacitance, C_A and C_B for the quasi-tapping capacitances and L_{RID} for the tail-current source degenerative inductance.

2.1. Frequency tuning

In order to cover both the 1.8GHz and the 2.2GHz frequency band, the LC tank is constructed with one variable (varactor) and one fixed-value capacitor that can be switched on and off by, e.g., a MOS switch. Fine frequency tuning of 250MHz around 1.85GHz and 2.15GHz, the DCS1800 and WCDMA central frequencies, is achieved by means of the variable capacitor C_V . Its minimum and maximum capacitance are 2.1pF and 3.5pF respectively, for a voltage tuning range of 2.7V. On the other hand, switching between the two bands/standards, is achieved with a 1.1pF switched capacitor. In the WCDMA mode it is disconnected from the LC tank, while in the DCS1800 mode it is inserted.

This frequency tuning scheme allows for a 600MHz over-all tuning range, from 1.7GHz to 2.3GHz. The frequency vs. voltage tuning range is shown in Figure 2.

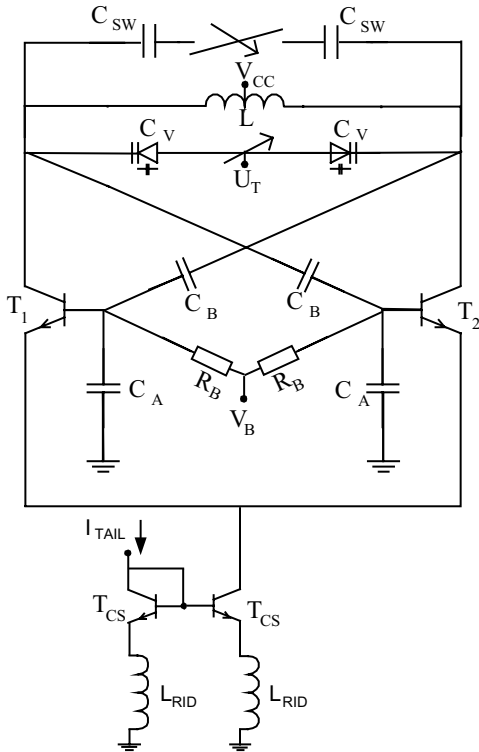


Figure 1. Quasi-tapped LC-oscillator.

3. PHASE-NOISE ADAPTIVITY

Once the noise originating from the bias circuitry in the oscillator is made negligible, the oscillator *noise performance* will depend only on the properties of the active part and the properties of the resonator.

On the other hand, as the *signal performance*, i.e., voltage swing over the LC tank, depends on the bias tail current, it will be possible to adapt the phase noise of the oscillator to different standards/specifications, through a change in a current I_{TAIL} , shown in Figure 1. This phenomenon is named *phase-noise tuning* [3], and the figure describing the oscillator's phase-noise adaptivity is named *phase-noise tuning range*.

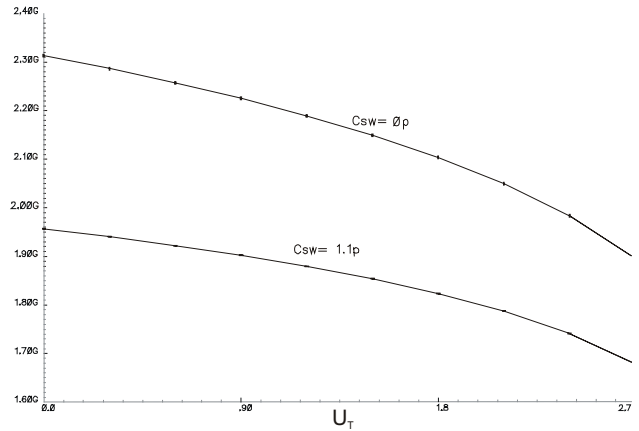


Figure 2. Frequency tuning curves for a 2.7V tuning voltage and 1.1pF switched capacitance.

However, before elaborating on the aspect of phase-noise tuning, let us first briefly describe the conditions for noise-free biasing.

3.1. Bias noise suppression

In order to avoid that the contribution of the biasing tail-current noise around even multiples of the resonant frequency to the over-all phase noise of the oscillator becomes larger than all the other contributions together [4], a low-noise biasing scheme, named *resonant inductive degeneration (RID)* [5] of the tail-current source, is employed, leading to a reduction of the noise contribution of the oscillator's tail current source to a minimum. The technique relies on *resonant-matching* of the inductor in the emitter of the biasing transistor to the transistors reactive part, being the base-emitter capacitance C_{Tb} , at twice the oscillating frequency $2f_0$. Satisfying the condition $R_{IN}g_{m,CS}=(f_T/2f_0)^2$, where f_T is the transit frequency, $g_{m,CS}$ the transconductance and $R_{IN}=2\pi f_T L_{RID}$ the input impedance of the tail-current source, the effective transfer of the equivalent input voltage-noise power to the output of the biasing transistor is reduced by a factor of $(f_T/2f_0)^2$. For the chosen current source parameters, and for the resonantly matched inductance $L_{RID}=3.4\text{nH}$, a factor of 40 tail-current

noise suppression is estimated, resulting in an 7dB phase-noise improvement.

3.2. Phase-noise tuning

So far, single-mode oscillators have been designed to satisfy the most stringent conditions, having all the performance and circuit parameters fixed. As the mobiles are exposed to such conditions only for a short period of time during operation, worst case design, i.e., over-design, appears to be rather expensive in terms of power.

On the other hand, multi-standard operation implies that there are multiple worst case conditions, i.e., one per standard. Therefore, applying a design procedure of single-standard oscillators to multi-standard, multi-mode oscillators, satisfying the most stringent conditions of the most demanding operation mode, would lead to even larger penalties in power consumption. However, this rather expensive approach is, nowadays, rather accepted among designers of oscillators [6].

Adapting oscillator to different operating conditions/standards, would solve the problem of waste of power. For example, when switching from the phase-noise demanding, DCS1800 mode to the less demanding WCDMA mode, it is not necessary any more to stay at the best phase-noise level, but rather a lower one.

The selection of appropriate oscillator parameters, in line with the design for adaptivity approach outlined above, is treated in the remainder of the subsection.

Having the noise of the biasing tail-current source eliminated, a required $PNTR$ of 11dB can be achieved between the loop-gain value of $k_{MIN}=2$, the safety start-up condition, and the value $k_{MAX}=19$, where the best phase noise is expected. The loop-gain k_{MAX} is estimated from the simplified expression [3]

$$PNTR(k_1, k_2) = \frac{\mathcal{L}_{QT}(k_1)}{\mathcal{L}_{QT}(k_2)} = \frac{k_2^2}{k_1^2} \frac{1+n(k_1/2+c)}{1+n(k_2/2+c)} \quad (1)$$

where c is a positive constant defined as $c=r_B g_{ms-up}$, with r_B and g_{ms-up} being the core transistor's base resistance and start-up ($k=1$) transconductance and \mathcal{L} being the phase noise of the oscillator. Relating the voltage swing across the bases of the oscillator's active part to the loop gain as

$$V_{S,B} = \frac{2}{\pi} \frac{I_{TAIL}}{G_{TK}} = \frac{8}{\pi} k V_T \quad (2)$$

where G_{TK} is the equivalent LC-tank conductance and V_T the thermal voltage, for the maximum value of the loop gain and the best phase noise, a voltage swing across the bases of $V_{S,B,MAX}=1.2V$ is required. On the other hand, the maximum voltage swing across the bases of the active part should not be larger than $V_{S,B,MAX}=2(V_{CC}+(V_{BE}-V_{CE,SAT})-V_B)/(n+1)$, the value up to which the effective reduction of the detrimental

effects of both hard saturation and additional current noise of the forward biased base-collector junctions of the transistors can be achieved. Here, $V_{CC}=2.7V$ is the supply voltage and V_B is the base potential of the core transistors. From this it follows that the DC base voltage that allows for the required phase-noise tuning range of $PNTR=11dB$ is between $V_B=1.8V$ ($V_{CE,SAT}=0.3V$) and $V_B=2.1V$ ($V_{CE,SAT}=0V$) as a compromise between weaker saturation and larger voltage swing.

4. SIMULATION RESULTS

Using 50GHz SiGe technology device parameters, all the simulations have been performed with the SpectreRF Cadence simulation tool. An 3nH differentially driven symmetric LC-tank inductor and an 3.4nH RID asymmetric inductor have been additionally designed. The inductors' model parameters have been derived with the aid of the GEMCAP simulator [7]. The values of other oscillator parameters are already given in the previous sections.

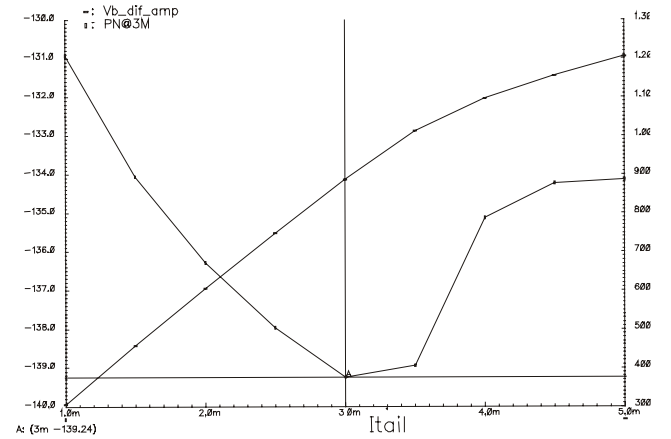


Figure 3. Phase-noise tuning range and voltage-swing tuning range at 1.8GHz. Phase noise at 3MHz offset from the oscillating frequency is considered here.

Following the design procedure outlined above, the operating range of the oscillator is determined to be between a tail current of 0.3mA and 3mA. The phase-noise tuning range and the voltage-swing tuning range, as a function of the tail current, in the 1.8GHz DCS1800 band, are shown in Figure 3. In this frequency range, the VCO achieves a figure of merit $FOM = \mathcal{L}(Aff_0)^2 V_{CC} I_{TAIL} = 186$. The 2.2GHz WCDMA phase-noise tuning range and the voltage-swing tuning range are shown in Figure 4. At this frequency, a figure of merit of 186 can be achieved as well.

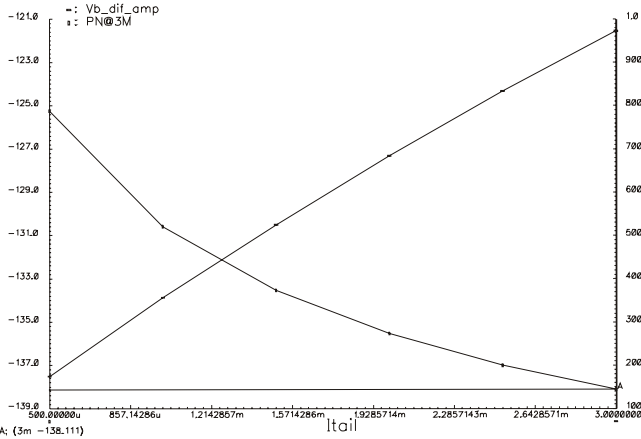


Figure 4. Phase-noise tuning range and voltage-swing tuning range at 2.2GHz. Phase noise at 3MHz offset from the oscillating frequency is considered here.

5. CONCLUSIONS

Enhancing the performance of wireless devices to cover multiple standards means that the system will have more functionality, but more performance *only* if the system can be adapted to different radio-channel conditions. What is more, being able to share the building blocks among different standards, *adaptive multi-standard front-ends* will offer the advantage of reduced complexity, chip area and over-all cost.

Accordingly, a second-third generation adaptive voltage-controlled oscillator has been described, operating in DCS1800 and WCDMA mode, satisfying all the requirements at power consumption levels of 6mW and 1.5mW, respectively.

6. REFERENCES

- [1] J. Ryyanen, K. Kivekas, J. Jussila, A. Parssinen, K. Halonen, "A dual-band RF front-end for WCDMA and GSM applications", *Proceedings CICC2000*.
- [2] A. Tasic and W. A. Serdijn, "Concept of Quasi-Capacitive Tapping of Bipolar Voltage-Controlled Oscillators", *Proceedings ICECS2002*.
- [3] A. Tasic and W. A. Serdijn, "Concept of Phase-Noise Tuning of Bipolar Voltage-Controlled Oscillators", *Proceedings ISCAS2002*.
- [4] J. J. Rael and A. Abidi, "Physical Processes of phase-noise in differential LC Osillators", *Proceedings CICC2000*.
- [5] A. Tasić, W. A. Serdijn and J. R. Long, "Resonant-Inductive Degeneration of Voltage-Controlled Oscillator's Tail-Current Source", *Proceedings ISCAS2003*.
- [6] D. Wang et. al., "A fully integrated GSM/DCS/PCS Rx VCO with fast switching auto-band selection", *Proceedings RAWCON2002*.
- [7] J. R. Long, *GEMCAP* - inductor modeling tool.