A PPM GAUSSIAN PULSE GENERATOR FOR ULTRA-WIDEBAND COMMUNICATIONS

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ABSTRACT

A Gaussian pulse generator incorporating a pulse position modulator for use in an ultra-wideband or impulse radio system is described. The pulse generator is preceded by a programmable pulse-position modulator and consists of a cascade of complex first-order systems, which, in turn, are made up of differential pairs employing partial positive feedback. The resulting PPM Gaussian pulse generator has been designed to be implemented in AMS 0.35µm CMOS IC technology. Simulations predict the correct operation of the circuit for supply voltages of 3.3V and a power consumption of 95mW. The output monocycle indeed approximates a Gaussian monocycle very well and has a pulse duration of about 230ps. Proper modulation of the pulse in time is confirmed.

Keywords - ultra-wideband, complex first-order systems, pulse position modulation, analog integrated circuits, transceiver

1. INTRODUCTION

The United States Federal Communications Commission (FCC) has officially endorsed ultra-wideband (UWB) technology for commercial wireless applications. One of the variants of UWB, called impulse radio (ir), may revolutionize the way we think in wireless technology by modulating data in time rather than in frequency, which promises enhanced data throughput with low-power consumption. Transmitted pulses of ultra-short duration with very low power spectral density, a wide fractional channel bandwidth and excellent immunity to interference from other radio systems, are typical characteristics of ir-UWB systems **[1]**.
The implementation of an active Gaussian pulse generator is the focus of this work. Gaussian pulses offer an excellent time-frequency resolution product **[2].** Pulse position modulation is used to encode the binary transmitted data **[3] [4]**.
The Gaussian pulse generator comprises a cascade of a fast triangular pulse generator and a Gaussian filter (i.e., a filter with a Gaussian impulse response) **[2]** and is described in the following two sections of this paper. It is central to the ultra-wideband transmitter design. The filter is implemented as a cascade of three complex first-order systems (CFOS), which consist of gm-C sections that employ differential pairs with partial positive feedback. The CFOS is described in Section 3. When driven by the triangular pulse generator, which is presented in Section 4, the filter provides an output signal that approximates a Gaussian monocycle. The pulse is modulated in time by means of a programmable binary pulse position modulator (PPM) that precedes the Gaussian filter. Simulation results are presented in Section 5.

2. TRANSMITTER ARCHITECTURE

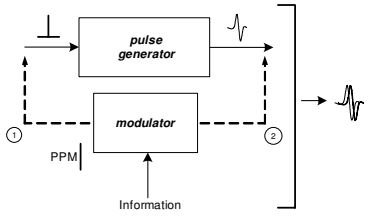

Figure 1 (1) PPM precedes the pulse generator; (2) PPM succeeds pulse generator

In principle, the pulse generator may either precede or succeed the pulse position modulation (PPM) (See Figure 1). Delay circuits that are used to implement pulse position modulation are either active on the incoming binary data or on the pulses ready for transmission. It is known that delaying continuous time signals requires a higher degree of hardware complexity as compared to delaying a binary signal. Hence, the modulator will be located in front of the pulse generator.

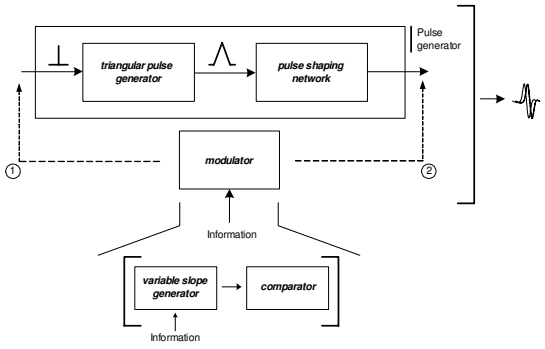

Figure 2 PPM based pulse generator. The modulator will either proceed or follow the pulse generator

Figure 2 shows the triangular pulse generator as part of the pulse generator. The triangular pulse generator is used to avoid cross talk and to approximate an impulse-like waveform to evoke the Gaussian monocycle. The pulse shaping network or Gaussian filter is implemented by using cascaded CFOS stages. The modulator is composed of a variable slope generator and a

comparator. The block scheme for the resulting UWB transmitter is depicted in Figure 3.

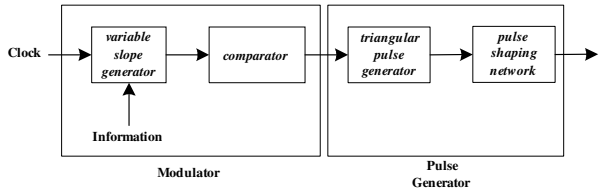

Figure 3 UWB transmitter

3. CFOS REALIZATION

A complex first-order system (CFOS) is basically an extension of an ordinary first-order to complex variables. Its structure exhibits similar characteristics as an ordinary second order system. Two real equations are used to express the behavior of a CFOS instead of one complex equation **[2]**.

$$\frac{d}{dt}x(t) = (\sigma + j\omega)x(t) + (cr + jci)u(t) \quad x(t) = xr(t) + xi(t) \tag{1}$$

where u is a real input signal, x is a complex state variable, σ, ω, cr, ci are system parameters; $\sigma \leq 0$, $\omega > 0$, ci and cr are real numbers. Furthermore, the impulse response is represented by the following equation.

$$h(t) = (cr + jci)e^{(\sigma_0 + \omega_0 j)t}U^{-1}(t) \tag{2}$$

Output voltage xr can be designed using an integrator whose input current is the sum of u/Rr, $-xi/R\omega$, and $-xr/R\sigma$, according to

$$xr = \int\left(\frac{-xr}{R\sigma C} + \frac{-xi}{R\omega C} + \frac{ur}{RrC}\right)dt \tag{3}$$

Likewise, output voltage xi too can be written as:

$$xi = \int\left(\frac{-xi}{R\omega C} + \frac{xr}{R\sigma C} + \frac{ur}{RiC}\right)dt \tag{4}$$

Subsequently, one expresses the real (xr) and imaginary outputs (xi) as follows:

$$xr = \frac{-R\sigma}{1 + R\sigma C}\left(\frac{ur}{Rr} + \frac{xi}{R\omega}\right) \tag{5}$$

$$xi = \frac{R\sigma}{1 + R\sigma C}\left(\frac{xr}{R\omega}\right) \tag{6}$$

From (5) and (6) one easily calculates the transfer function of the CFOS cell for the real and imaginary outputs, which are given as follows.

$$\frac{xr}{ur} = \frac{-R_\sigma R_\omega^2(1 + R_\sigma Cs)}{R_r(R_\omega^2 + R_\sigma^2)\left(\frac{R_\omega^2 R_\sigma^2 C^2}{R_\omega^2 + R_\sigma^2}s^2 + 2\frac{R_\omega^2 R_\sigma C}{R_\omega^2 + R_\sigma^2}s + 1\right)} \tag{7}$$

$$\frac{xi}{ur} = \frac{-R_\sigma^2 R_\omega}{R_r(R_\omega^2 + R_\sigma^2)\left(\frac{R_\omega^2 R_\sigma^2 C^2}{R_\omega^2 + R_\sigma^2}s^2 + 2\frac{R_\omega^2 R_\sigma C}{R_\omega^2 + R_\sigma^2}s + 1\right)} \tag{8}$$

As illustrated by (7) and (8), the complex first-order system does show similar characteristics of that of a second order system and this confirms the statement made earlier. One also establishes the expressions for σ, ω and cr, which are, respectively:

$$\sigma = \frac{1}{R_\sigma C}; \qquad \omega = \frac{1}{R_\omega C}; \qquad c_r = \frac{1}{R_r C} \tag{9}$$

Now going back to (2), one may validate the results obtained for σ, ω and cr. Considering the Laplace transform of the two functions shown in (10) and (11), it is unambiguous that the impulse response of the real output is equal to $c_r e^{-\sigma t}\cos(\omega t)$ and similarly, the impulse response of the imaginary output is equal to $c_r e^{-\sigma t}\sin(\omega t)$.

$$L[c_r e^{-\sigma t}\cos(\omega t)] = \frac{-c_r\sigma}{\omega^2 + \sigma^2}\frac{1 + \frac{s}{\sigma}}{\frac{s^2}{\omega^2 + \sigma^2} + 2\frac{\sigma}{\omega^2 + \sigma^2}s + 1} \tag{10}$$

$$L[c_r e^{-\sigma t}\sin(\omega t)] = -\frac{c_r\omega}{\omega^2 + \sigma^2}\frac{1}{\frac{s^2}{\omega^2 + \sigma^2} + 2\frac{\sigma}{\omega^2 + \sigma^2}s + 1} \tag{11}$$

From (2), the impulse response of a cascaded (n+1) CFOS system is given by (12).

$$h_{n+1}(t) = A(c_r + jc_i)^{n+1}\frac{t^n}{n!}e^{(\sigma + j\omega)t}U(t) \tag{12}$$

As one can deduce from the term $t^n/n!$, the more the number of stages, the better the approximation of the Gaussian envelope.

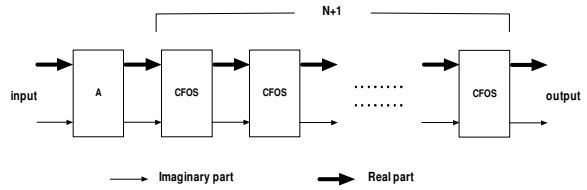

Figure 4 Cascaded CFOS

4. CIRCUIT DESIGN

4.1 Pulse generator

4.1.1 gm-C cell CFOS

To satisfy (5) and (6) and for high frequency applications, one uses small and fast transition blocks such as gm-C cells (Figure 5) **[5]**. However, due to the four cascaded transistor stages in the feedback ring, the response time of the CFOS stage becomes too large. Moreover, from simulations it follows that ten stages need to be cascaded to achieve a reasonable approximation of the Gaussian envelope. As a result, the power consumption becomes too large.

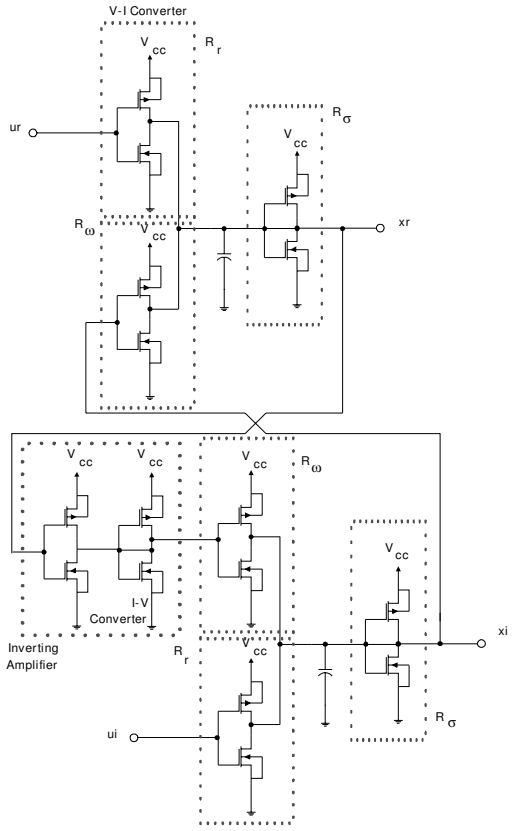

Figure 5 gm-C single stage CFOS

To solve this, a differential structure is used to get rid of the required inverters and thus enhance the response time of the CFOS.

4.1.2 Pulse shaping network

The differential pair arrangement in Figure 6 with partial positive feedback (PPF) **[**6**]** also satisfies equations (7) and (8).

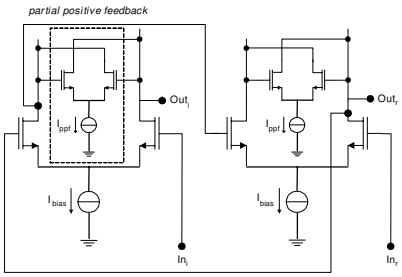

Figure 6 Differential pair with gain enhancement; single-stage CFOS

The inclusion of the PPF stage as active load enhancement not only increases the DC gain but also the unity gain frequency. The significant increase in the gain and the bandwidth is contributed to the increase in the effective transconductance of the stage.

Let n be the loop gain, then the gain of the amplifier is enhanced by a factor of $1/(1- n)$. When n tends to 1, the gain tends to infinity. If n is made too large or too small, it will either make the system unstable or have little to no effect on the performance of the amplifier at all. Thus, n should be bounded by the following equation.

$$0< n <1 \qquad (12)$$

A significant improvement in the response time is seen because of the PPF loop. One could even use PMOS pull-ups as a positive feedback load to save power.

4.1.3 Triangular pulse generator

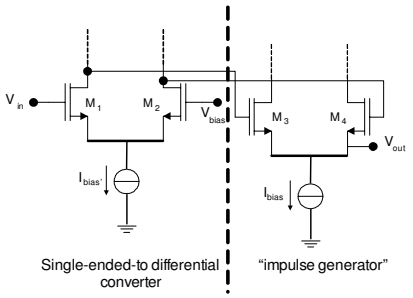

Figure 7 Triangular pulse generator

The triangular pulse generator is made up of a single-ended to differential converter, followed by an even-symmetry function. See Figure 7. The key purpose of this block is to generate an impulse-like function that is able to evoke the impulse response of the succeeding pulse shaper. This circuit is biased such that for either bit 1 or 0 the output voltage, V_{out}, remains fixed at a predetermined value. When the input voltage, V_{in}, equals 0V, then M_1 is off and M_2 conducts. Subsequently, M_3 stays in saturation and M_4 is turned off. Similarly, when V_{in} is equal to V_{CC}, M_1 and M_4 are in saturation and M_2 and M_3 are off. However, during a 0-1 or 1-0 transition, all four transistors conduct, V_{out} is lowered and a triangular pulse is being generated.

4.2 Modulator

4.2.1 Variable slope generator and comparator

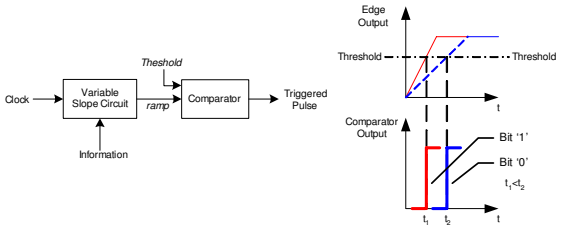

Figure 8 a) PPM modulator comprises of a variable slope circuit and a comparator

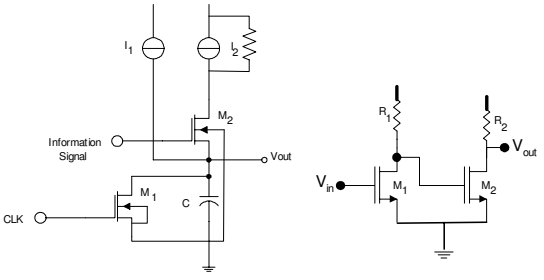

Figure 9 a) variable slope generator b) comparator

When designing a pulse position modulator, one exploits a ramp, whose slope depends on the information signal. This

signal is fed to a comparator that compares the momentary value of the ramp with a fixed threshold and generates a trigger.
The concept of having an edge with a varying slope and a comparator yields a pulse position modulator (Figure 8) **[7].**
The slope of the edge depends on the total current (I) through the capacitance and the capacitance (C) **[8] [9].** The variable slope circuit is implemented using a capacitor charged by a binary dc current. The resulting voltage is given by the following equation.

$$V_{out} = \frac{I}{C}t + V(0) \tag{13}$$

Switches S1 and S2 are implemented by simple NMOS transistors. The circuit functions in the following manner. Firstly, when the information signal is low, M_2 is open. When the clock signal is low (M_1 open), capacitor C is charged by current I_1 and thus the output edge has a slope with a definite value. Secondly, when the information signal is high, M_2 is closed. When the clock signal is low (M_1 open), capacitor C is charged by a current I_1+ I_2 and thus now the output edge has a steeper slope. Finally, S_1 is closed to reset the variable slope generator. As for the working of the comparator, when the input signal is low, M_1 is turned off, while M_2 conducts with a gate-source voltage equals to V_{CC}. This results in an output voltage V_{OUTL}, given by:

$$V_{OUTL} = V_{CC} - R2\frac{k2}{2}(V_{CC} - V_T)^2 \tag{14}$$

where V_T is the threshold voltage and *k2* is defined as the product of the transconductance coefficient and the aspect ratio of the transistor (*W/L*).
Increasing the input voltage V_{in} beyond V_T, M_1 begins to conduct and thus the gate-source voltage of M_2 decreases. The drain current of M_2 decreases and consequently, the output voltage, V_{OUT} increases. For an input voltage equal to V_{INH}, the gate-source voltage of M_2 becomes equal to its threshold voltage and thus M_2 is turned off. Finally, V_{OUT} becomes equal to V_{CC}. By increasing the input voltage even further, the gate-source voltage of M_2 decreases and so transistor M_2 continues to stay turned off allowing the output voltage to remain at V_{CC}.
For V_{INH}, it holds:

$$V_{INH} = V_T + \sqrt{\frac{2(V_{CC} - V_T)}{R1k1}} \tag{15}$$

Similarly, *k1* is the product of the transconductance coefficient and the aspect ratio of the transistor (*W/L*).
The comparator threshold thus becomes:

$$V_* = V_T + \sqrt{\frac{(V_{CC} - V_T)}{2R1k1}} \tag{16}$$

5. SIMULATION RESULTS

Given that all simulations were carried out in AMS 0.35µm CMOS technology, the smallest possible pulse width attained is 230ps before layout extraction and 300ps after layout extraction when using a cascade of three CFOS stages. See Figure 10.
The power consumption is approximately equal to 95mW at a power supply of 3.3V. By controlling currents I_1 and I_2, time delays in the order of picoseconds to nanoseconds could be achieved. Proper pulse position modulation is confirmed.

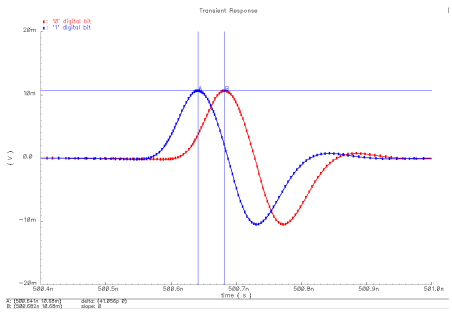

Figure 10 Pulse position modulation of 1st derivative of Gaussian monocycle

6. CONCLUSIONS

A fully programmable on-chip Gaussian pulse generator incorporating a pulse position modulator for use in an ultra-wideband or impulse radio system has been presented. Proper modulation of the information as well as an excellent approximation of the Gaussian monocycle has been achieved. The smallest possible pulse width attained was 230ps before layout extraction and roughly 300ps after layout extraction. The power consumption was approximately equal to 95mW at a power supply of 3.3V.

7. REFERENCES

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