AN ULTRA LOW-POWER DYNAMIC TRANSLINEAR CARDIAC SENSE AMPLIFIER FOR PACEMAKERS

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ABSTRACT

In this paper, a cardiac sense amplifier, i.e. the front end of a pacemaker, based on the Dynamic Translinear (DTL) circuit technique is presented. The system consists of a voltage-to-current converter, a bandpass filter, absolute value and RMS-DC converter circuits and an event detection circuit. From simulations, it is demonstrated that the DTL technique is a good alternative to conventional sense amplifiers for intra cardiac applications since they handle the required dynamic range and perform non-linear operations at low supply voltages. The circuit operates from a 2-V supply voltage and dissipates 240nW.

***Keywords* –** Cardiac signal detection, dynamic translinear circuits, analog signal processing, integrated circuits, IECG

1. INTRODUCTION

Conventional pacemaker topologies usually are divided into an analog part (comprising a sense amplifier and a heart stimulator) and a digital part (comprising a micro controller) [1]. The sense amplifier plays a fundamental role in providing information about the current state of the heart. It is designed to detect and monitor intracardiac signal events (e.g., R-waves in the ventricle). After signal sensing, the signal is fed to the digital microprocessor that decides upon the appropriate pacing therapy to be delivered by the stimulator. However, the algorithm in the microprocessor requires from the sense amplifier the accurate measurement of the heart activity even in the presence of noise and interference [2]. The diverse features of the intracardiac signals, therefore, require a large dynamic range, i.e., a large signal-to-noise-plus-interference level, for the sense amplifier.

This paper presents the applicability of DTL circuits to the design of cardiac sense amplifiers to be implemented in pacemakers. The main advantages of DTL circuits with respect to other low-power techniques are, first of all, the ability to handle a large dynamic range in a low-voltage environment. Second, the static and dynamic translinear principles can be applied to the implementation of the required transfer of functions described by (possibly non-linear) polynomial differential equations. Moreover, only transistors and capacitors are required to realize these functions. Since in conventional ultra low-power designs resistors would become too large for on-chip integration, their superfluity is a very important advantage. Others advantages are that DTL circuits present a high functional density and are theoretically process and temperature independent.

We thus implement a fully-integrated sense amplifier with a large dynamic range by means of DTL circuits.

Section 2 treats the required functionality of the sense amplifier. Next, Section 3 provides an overview of the static translinear (STL) and dynamic translinear (DTL) principles. The circuit designs are subsequently described in Sections 4 to 7. Some results provided by simulations are shown in Section 8. Finally, Section 9 presents the conclusions.

2. DESIGN SPECIFICATIONS AND CIRCUIT DESCRIPTION

In Fig.1 a suitable block diagram of a sense amplifier for cardiac signal detection is given. The system consists of a V-I (voltage-to-current) converter, a bandpass filter, absolute value [3] and RMS-DC converter circuits [4,5], and a comparator circuit [3]. Additionally, an EMI filter is implemented off-chip for electromagnetic interference cancellation (not shown). It is a 2^{nd} order bandpass filter to suppress dc and signals beyond 1kHz. The V-I converter is required as the input and output quantities of the EMI filter are voltages and translinear circuits are inherently current-mode as will be treated in Section 3. The bandpass filter is used to specifically select intra-cardiac signals, in our case being the QRS complex or R-wave, and to minimize the effect of the overlapping myocardial interference signals and low frequency breathing artifacts. The center frequency of the bandpass filter is located at 25 Hz. The reason to use an absolute value circuit is to be independent from the electrode position in the heart. Accommodation to changes in the average input signal level is realized using the RMS-DC converter. This circuit implements two functions, a squarer-divider and a lowpass filter. At the end of the block schematic, the detection signal (a binary value) is generated depending upon a threshold level, which is given by:

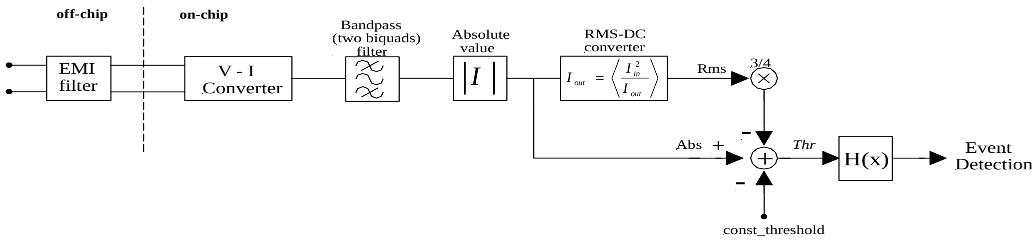


Fig. 1. Block diagram of the sense amplifier

$$Thr = Abs - \left(\frac{3}{4} Rms + const\_threshold \right) \tag{1}$$

where *Thr* is the adaptive threshold level, *the* A*bs* variable is the output signal of the absolute value circuit. *Rms* is the output of the RMS-DC converter. *const_threshold* is a constant value that can be derived from typical values of the input signal.

3. STATIC AND DYNAMIC TRANSLINEAR PRINCIPLE

Translinear (TL) circuits can be divided into Static (STL) and Dynamic Translinear (DTL) circuits.

STL circuits are employed to realize any static transfer function. In order to describe the STL principle, an example of a four-transistor TL loop is shown in Fig. 2 [6]. The STL principle states that this circuit can be best described in terms of the collector currents I_1 through I_4. The translinear loop is thus described by a simple equation in terms of products of (collector) currents

$$I_1 I_3 = I_2 I_4 \tag{2}$$

Linear or nonlinear dynamic (i.e., frequency-dependent) functions (differential equations) can be implemented by DTL circuits. The DTL principle is shown in the sub-circuit in Fig. 3 [7]. This circuit implements a relation between the collector current I_C and the current I_{cap} flowing through the capacitance C according to

$$CU_T \dot{I}_C = I_{cap} I_C \tag{3}$$

where the dot represents differentiation with respect to time.

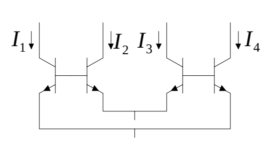


Fig. 2. A four-transistor TL loop.

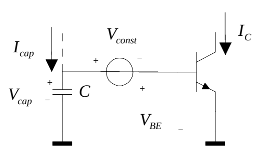


Fig. 3. Principle of dynamic translinear circuits

The combination STL and DTL principles can thus be applied to the implementation of functions described by linear or nonlinear polynomial differential equations.

4. DIFFERENTIAL VOLTAGE TO SINGLE-ENDED CURRENT CONVERTER

The output signal of the EMI filter is a differential voltage, in the order of a few millivolts, and the input signal of the bandpass filter is a single-ended current. The required transformation of the differential input voltage into a single-ended current can be simply performed by a differential pair loaded by two current mirrors as shown in Fig.4. Note that the transconductance factor is determined by the value of the current *Io* and equals $Io/4U_T$. Since the output nodes of the EMI filter are floating, the differential input nodes of the V-I converter need to be biased at a voltage in between the power supplies. This CM (common-mode) input voltage is set by the CM loop comprising Q3-Q7 and approximates $V_{cc} - 3V_{be}$.

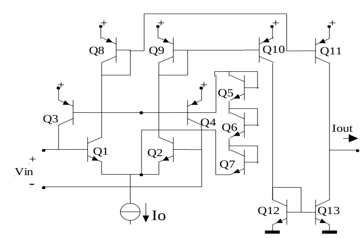


Fig. 4. Differential input voltage to single-ended current converter

5. BANDPASS FILTER

To achieve sufficient selectivity around 25 Hz the filter is implemented by a cascade of two biquadratic bandpass filter sections. These biquads, in turn, are realized by two lossy integrators according to the block diagram given in Fig. 5a. The integrators comprise four transistors and one capacitor in a loop and implement

$$CU_T \dot{I}_{out} + I_o I_{out} = I_o I_{in} \tag{4}$$

where *Io* is a dc bias current and *Iout* is the low-pass filtered version of *Iin*. The expression above is a linear differential equation, describing a low-pass filter with cutoff frequency ω_C according to

$$\omega_C = \frac{I_o}{CU_T} \tag{5}$$

In Fig. 5b the circuit diagram of one biquad for realizing a part of the bandpass filter is given. The integrator loops are defined by transistors Q1-Q4 and capacitor C1 and Q5-Q8 and C2, respectively. A positive feedback network using current mirror Q11-Q12 turns the lossy integrator into a lossless integrator.

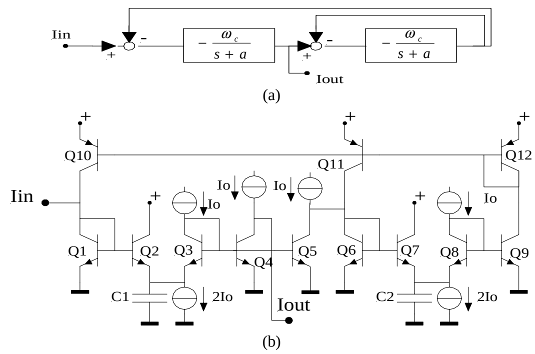


Fig. 5. (a) Block diagram of the bandpass biquad filter (b) Circuit schematic

For a system with the poles in Butterworth position the values of the capacitances are given by

Lossy integrator: $$C_1 = \frac{I_o}{U_T.(p_1 + p_2)} \tag{6a}$$

Lossless integrator: $$C_2 = \frac{I_o}{U_T.\sqrt{p_1 p_2}} \tag{6b}$$

Where p_1 and p_2 are the poles of the Butterworth polynomial implemented by the biquad.

6. ABSOLUTE VALUE AND RMS-DC CONVERTER CIRCUITS

Since the polarity of the input signal is not known, its absolute value is generated. The required function $I_{out} = |I_{in}|$ is realized with the circuit in Fig. 6 [3]. The translinear loop in the circuit consists of transistors Q2, Q1, Q5 and Q7, implementing

$$(I_o + I_{out})(I_o - I_{out}) = (I_o + I_{in})(I_o - I_{in}) \tag{7}$$

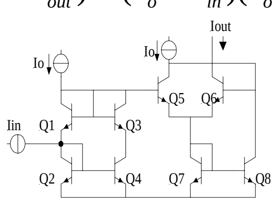


Fig. 6. Absolute value circuit

The RMS transfer is implemented by a squarer/divider circuit [4] and a low-pass filter and produces

$$I_{out} = \left\langle \frac{I_{in}^2}{I_{out}} \right\rangle \tag{8}$$

Its translinear differential equation describing a first-order RMS-DC conversion then follows as [5]

$$CU_T \dot{I}_{out} I_{out} + I_o I_{out}^2 = I_o I_{in}^2 \tag{9}$$

Note that this is a nonlinear differential equation.

A possible implementation is shown in Fig.7 [5]. Q1 through Q6 form the static translinear loop implementing $(I_{cap} + I_o)I_{out}^2 = I_o I_{in}^2$ and C, Q4-Q6 the dynamic translinear loop, implementing $2CU_T \dot{I}_{out} = I_{cap} I_{out}$. The quadratic factors I_{in}^2 and I_{out}^2 are implemented by Q1-Q2 and Q5 – Q6 respectively. Q7 and Q8 are buffers to avoid the base current error in Q2 and Q4.

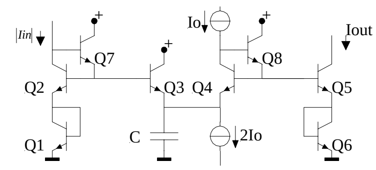


Fig. 7. RMS-DC converter circuit

7. DETECTION (SIGN FUNCTION) CIRCUIT

Since TL circuits can implement polynomial functions only, we first need to approximate the Sign function by a polynomial function. A static translinear loop equation to achieve a good approximation to the Sign function is described by [3]:

$$(I_o + I_{in})(I_o - I_{out})(I_o + I_{out}) = (I_o - I_{in})(I_o - I_{out})(I_o + I_{out}) \tag{10}$$

Its corresponding TL circuit is given in Fig. 8.

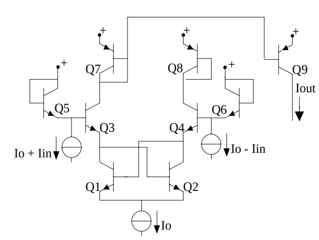


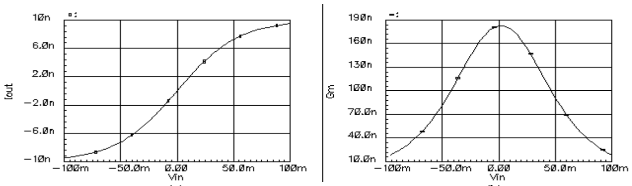
Fig. 8. Comparator circuit.

8. SIMULATION RESULTS

To validate the system principle and to check the circuit performance, the sub-circuits as well as the whole system have been simulated using models of our in-house bipolar semi-custom IC process, SIC3A [8]. Typical transistor parameters are $f_{T,\text{npn,max}}$ = 15GHz and $\beta_{F,\text{npn}}$ = 150 (smallest emitter size).

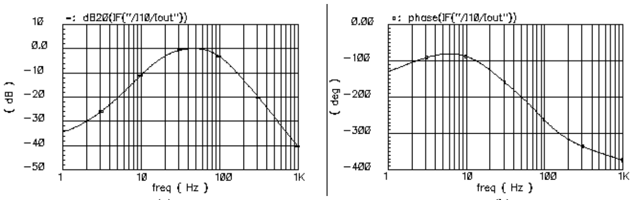
First, we simulated the V-I converter circuit. The dc transfer is given in Fig. 9. The value of current Io is 10.4nA resulting in a transconductance factor of 0.18μA/V to accommodate the desired input signal range.

The magnitude and phase response of the bandpass filter is shown in Fig.10a and Fig.10.b, respectively. Note that the center frequency of the bandpass is indeed located around 25 Hz. The first biquad has Io and C1 and C2 equal to 2nA, 80pF and 170pF respectively. For the second biquad these values are 0.4nA, 94pF and 131pF, respectively



(a) (b)

Fig. 9. DC transfer of the V-I converter (a) V-I characteristic (b) Transconductance factor.



(a) (b)

Fig. 10. Frequency response of the biquad (a) Magnitude (b) Phase

The dc transfer of the absolute value circuit is given in Fig.11. The circuit provides correct operation up to *Io*. In Fig. 12, the DC transfer of the comparator circuit, with *Io* equal to 1nA, is shown.

The output current of the RMS-DC converter is a time average of the input signal as seen from (9). The cut-off frequency is given by (5). To achieve a cut-off frequency of 1.5Hz, the values of Io and C (Fig.7) are 0.125nA and 1nF respectively. A transient analysis of the RMS-DC converter connected to the absolute value circuit is given in Fig.13. With a sinusoid applied at the input to validate the operation of the circuit, having a frequency of 10Hz and amplitude of 1.5nA, the RMS-DC circuit produces an output (drawn line) amplitude around 1nA, which is close to the ideal response (dotted line).

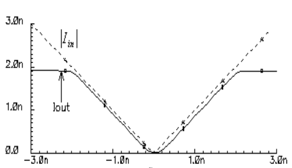


Fig. 11. DC transfer of the Absolute value circuit

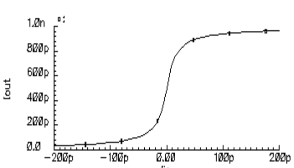


Fig. 12. DC response of the comparator circuit

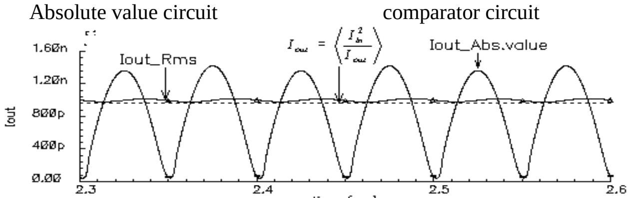


Fig. 13. Transient response of the RMS_DC connected to the Absolute value circuit

Finally, a test signal is applied to the system to verify the performance and efficiency of the complete sense amplifier according to Fig.1. A typical intra-cardiac signal measured in the ventricle, shown in Fig.14a, is applied to the input of the system. The transient response of the circuit is shown in Fig.14b. The system is clearly able to detect the R-wave, which represents the cardiac event that the circuit was supposed to detect.

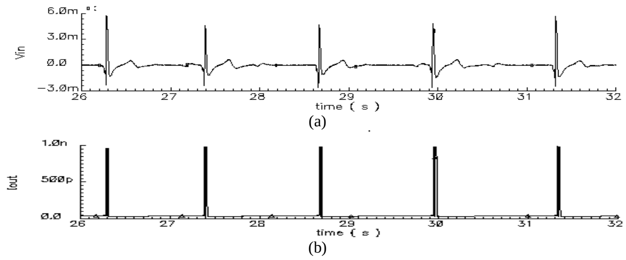


Fig. 14. Transient response of the complete sense amplifier circuit (a) Input voltage (b) Output current

The characteristics of the sense amplifier are summarized in Tab.1.

Table 1. Simulated sense amplifier characteristics.

Power supply	2.0V
Total bias current	120 nA
Power consumption	240 nW
Eq. rms noise voltage @ V-I converter input	0.1 mV
Eq. rms noise current @ Abs. value circuit output	3.6 pA
SNR @ Abs. value circuit output (10Hz – 1kHz)	39 dB
Eq. rms noise current @ comparator input while switching	6.5 pA

9. CONCLUSIONS

A cardiac sense amplifier based on the Dynamic Translinear circuit technique has been proposed. It comprises a V-I converter, a bandpass filter and absolute value, RMS-DC converter and comparator circuits. The whole system operates from a 2-V supply voltage and dissipates only 240nW. The obtained results in the sense amplifier demonstrate the desired performance of the sub-circuits and efficient detection of the R-wave for a typical intracardiac signal in an ultra low-power environment.

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