High-Frequency Dynamic Translinear and Log-domain Circuits in CMOS Technology

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ABSTRACT

A new topology for translinear filters in CMOS IC technology is presented. This translinear filter is based on the exponential relation of passive PN-diodes in CMOS technology while the CMOS transistors only provide gain. From simulations, it is demonstrated that this topology leads to an improvement in high-frequency performance. Cut-off frequencies higher than 200 MHz with Total Harmonic Distortion (THD) figures around 2% are reported.

Keywords – dynamic translinear, translinear, log domain, analog electronics, CMOS, filter.

1. INTRODUCTION

The trend toward lower power consumption, lower supply voltage and higher frequency operation has increased the interest of new design techniques for analogue integrated filters.

The class of translinear (TL) filters has emerged in recent years as a promising approach to face these challenges. The translinear approach is inherently companding, which offers low-voltage and low-power operation. Dynamic Translinear (DTL) circuits, also known as Log-domain or Exponential-State Space circuits, exploit the exponential large-signal transfer function of the semiconductor devices to implement a desired linear or nonlinear differential equation.

Usually, only active exponential devices are used, being bipolar transistors [1], MOS transistors in the weak inversion region [2] or lateral bipolar transistors in standard CMOS technology [3]. Their applications, however, are limited for, in CMOS technology, their high-frequency performance is rather poor. An alternative topology to implement DTL and Log-domain circuits, which improves the high-frequency performance, is proposed here. It is based on the exponential relation between voltage and current of passive PN-diodes and uses the CMOS transistor only to provide gain, in accordance with the original idea proposed by Adams [4].

The outline of the paper is as follows. In Section 2, the dynamic translinear principle and the basic translinear filter is described. Section 3 treats the employed voltage followers as well as the circuit description. Some simulation results are presented in Section 4. Finally, Section 5 presents the conclusions.

2. TRANSLINEAR FILTERS

2.1. Dynamic Translinear Principle

Translinear circuits are based on the exponential relation between voltage and current, characteristic for the diode, the bipolar transistor and the MOS transistor in the weak inversion region. They can be divided into Static and Dynamic TL circuits. The Static translinear circuits are applied to realize static transfer functions. Linear or nonlinear dynamic (i.e., frequency-dependent) functions (differential equations) can be implemented by DTL circuits.

The DTL principle is shown in the sub-circuit in Fig.1 [5].

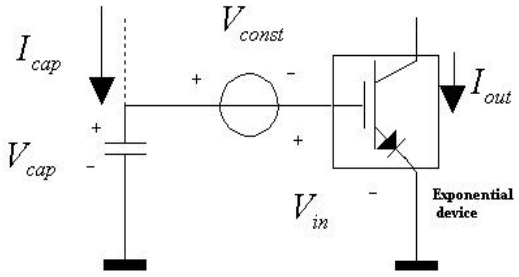

Fig. 1. Principle of dynamic translinear circuits

This circuit is described in terms of the output current I_{out} of the exponential device and the current I_{cap} flowing through the capacitance C. Note that the dc voltage source

V_{const} does not affect I_{cap}. I_{out} is based on the exponential law and can thus be described by:

$$I_{out} = I_s e^{V_{in}/U_T} \quad (1)$$

V_{in}, I_s, U_T being the input voltage, a specific current and a specific voltage respectively.

An expression for I_{cap} can be derived from the time derivative of the output current:

$$CU_T \dot{I}_{out} = I_{cap} I_{out} \quad (2)$$

where the dot represents differentiation with respect to time.

This expression defines the principle of dynamic translinear circuits: *"A time derivative of a current can be mapped onto a product of currents."* For the realization of this product of currents the conventional static translinear principle can be used.

Using dynamic translinear circuits, several classes of filters have been proposed [5, 6]. The characteristics of these classes can be derived from their output structures. The class of log-domain filters is based on a single-transistor output structure in line with Fig.1.

However, the DTL principle can also be used to implement non-linear differential equations, e.g., the ones that belong to oscillators [7] and RMS-DC converters [8].

2.2. Basic translinear filter

An earlier method of log-domain filtering as proposed by Adams, 1979, that lends itself to be implemented in any CMOS IC technology, and does not require exponential behavior of the CMOS transistors is depicted in Fig. 2. Typically, log-domain filters operate in class A. The circuit is a first-order low-pass filter and can be analyzed as follows [9].

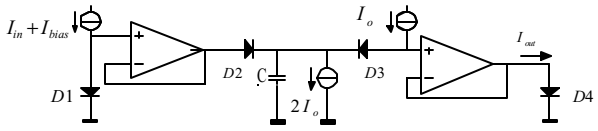

Fig. 2. Log-Domain filter

The four (exponential) diodes, D1-D4, constitute a TL loop. The combination of the capacitor C, the right opamp and diode D_4 is similar to the output sub-circuit shown in Fig. 1. Diode D_3 is biased by a dc current I_o and therefore complies with a constant voltage source. The output current flows through diode D_4. The current through D_2 equals (I_o + I_{cap}) and the input current, together with biasing current I_{bias} flow through diode D_1.

According to the TL principle, the products of the currents of forward biased junctions in the clockwise and counter-clockwise oriented devices are equal. Hence:

$$(I_{bias} + I_{in})I_o = (I_0 + I_{cap})(I_{dc} + I_{out}) \quad (3)$$

Using eqn (2), this yields:

$$CU_T \dot{I}_{out} + I_o I_{out} = I_o I_{in} \quad (4)$$

which is a linear differential equation, describing a low-pass filter with cutoff frequency ω_C according to:

$$\omega_C = \frac{I_o}{CU_T} \quad (5)$$

3. VOLTAGE FOLLOWER

The main requirements of the unity-gain amplifiers that are employed in the circuit of Fig.2 are high-frequency response, low gain error, high linearity and a sufficiently low output resistance.

The proposed voltage follower, to be implemented in CMOS technology, is based on a symmetrical structure of a two-stage topology [10]. Compared to single-stage topologies, two-stage topologies increase the loop gain and therefore decrease the output impedance of the circuit. The characteristics of the proposed circuit are a nominally zero systematic offset and highly reduced harmonic distortion and transfer gain error.

3.1. Frequency Compensation

The two-stage topology adopts the Miller compensation technique to achieve stability in closed-loop conditions. However, such compensation also results in a right half-plane zero in the open-loop gain, due to the forward path through the compensation capacitor to the output. The right half-plane zero reduces the maximum achievable gain-bandwidth product, since it makes a negative phase contribution to the open-loop gain at a relatively high frequency. An optimized compensation strategy is based on the use of a voltage follower [11]. It efficiently uses the finite output conductance of a voltage buffer to provide pole-zero compensation, thus allowing a great increase in the loopgain-poles [12] product to be achieved.

The voltage buffer is implemented with the common-drain configuration shown in Fig. 3

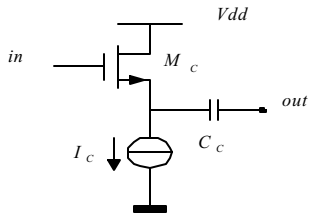

Fig. 3. Voltage buffer for frequency compensation

3.2. Circuit description

The circuit diagram of the voltage follower is depicted in Fig.4. M1 and M2 form the source-coupled pair of the differential stage. M3 and M4 are both diode-connected to improve the symmetry of the topology. The transistors M5 and M6 enhance the overall loop gain while maintaining identical the source-drain voltage drops across transistors M7 and M8. Transistors M7-M14 implement the bias circuit. M13 is employed to obtain a good matching between p-channel and n-channel current sources. Finally, transistor M15 is used for the frequency compensation as described above. M1-M4, M13 and M5-M9 have the same aspect ratios respectively.

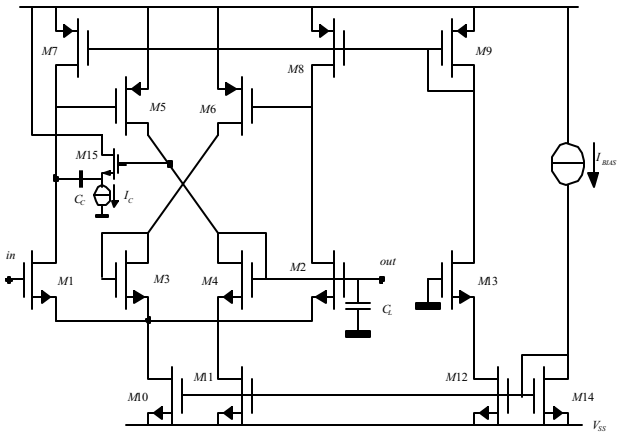

Fig. 4. Circuit diagram of the voltage follower

4. SIMULATION RESULTS

The circuit was simulated using PSPICE transistor and diode models of the 0.35 µm CMOS Si-gate AMS IC process [13].

The filter has been designed to operate from a 3.3V supply voltage. The bias current I_o ranges from 50nA to 0.5mA.

Fig. 5 depicts the cut-off frequency as a function of current I_o for four different capacitance (C) values: 100 fF, 1 pF, 10 pF and 100 pF. From this plot, it can be deduced that this filter can be controlled over a wide frequency range. Also indicated is that the filter exhibits less than 1% THD for a capacitance equal to 10pF for a 316 kHz input signal and 2.4% THD for a capacitance equal to 100 fF at 100 MHz. The cut-off frequency for Io = 50µA and C = 100 fF equals 220 MHz. Note that this circuit exhibits a better high-frequency performance than the circuit presented in [3] which yields a cut-off frequency below 30 MHz.

The AC responses of the low-pass filter with I_o equal to 5nA, 50nA, 0.5µA, 5µA and 50µA, respectively, and C equal to 10pF are shown in Fig. 6. The cut-off frequencies of these filter responses are 3.13 kHz, 31.6 kHz, 316 kHz, 3.10 MHz and 31.62 MHz, respectively.

Note that, starting from this lossy integrator, lossless and inverting lossy integrators can be realized as well, by adding appropriate unity-gain positive feedback or applying current mirrors, respectively.

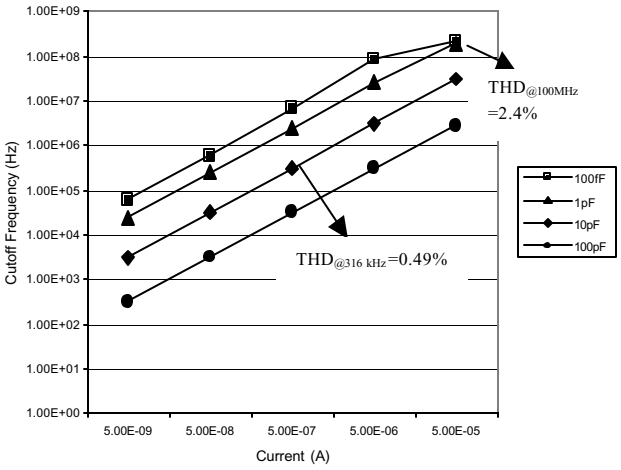

Fig. 5. Simulated cut-off frequencies as a function of current I_o for four different capacitor values.

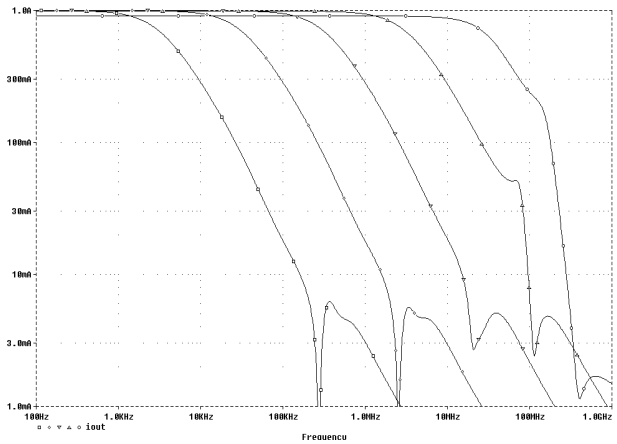

Fig. 6. Simulated log domain filter responses with C = 10pF.

5. CONCLUSION

A design technique for implementing a translinear filter in standard CMOS technology has been proposed. This technique makes use of the exponential relation between voltage and current of passive PN-diodes and uses the CMOS transistor only to provide gain. Simulations using realistic transistor and diode models indicate that cut-off frequencies of over 100 MHz can be achieved with a THD lower than 2,4%. The circuit presents an even better high frequency performance with cut-off frequencies up to 200 MHz, albeit at the expense of a degraded THD, for a very small capacitance and a control current equal to 50μA.

6. REFERENCES

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