

# 1.5 Low-voltage ultra-low-power analog IC design — switched-MOSFET technique

### Outline

- Introduction
- The basic Switched-MOSFET (SM) cell
- Why Switched-MOSFET
- Basic SM Integrators
- Universal SM Biquad
- Practical Issues
- Results
- Conclusions


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## Switched-MOSFET Sampled-Data Technique for Low-Voltage Supply

Luis Cléber C. Marques<sup>1</sup>, Carlos Galup-Montoro,  
Sidnei Noceti Filho, Fathi Farag, Wouter Serdijn<sup>2</sup>,  
and Márcio Chereim Schneider

Universidade Federal de Santa Catarina (UFSC)/Brazil

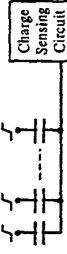
<sup>1</sup> - Centro Federal de Educação Tecnológica de Pernambuco (CEFET-PE)/Brazil;  
Currently in a cooperation with TU Delft, Bolsista do CNPQ - Brazil.  
<sup>2</sup> TU Delft 2 - Delft University of Technology (TU Delft)/The Netherlands



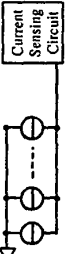
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### Sampled-data Circuits

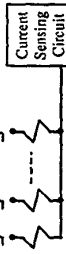
Three basic elements may be used




Capacitors




Current Sources




Resistors



Charge Sensing Circuit



Current Sensing Circuit



Current Sensing Circuit

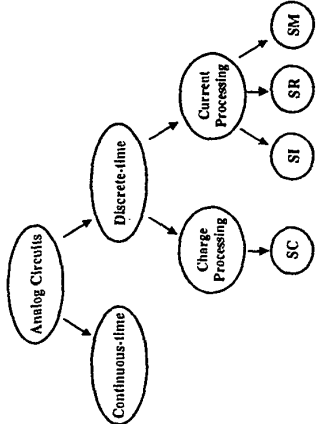
Switched-capacitor (SC)

Switched-current (SI)

Switched-resistor ?? (SR)

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### Introduction



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### Sampled-data Circuits – Basic building blocks

Switched-capacitor (SC) Integrator

Switched-current (SI) Delay Cell

Switched-resistor (SR) Delay Cell

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### Switched-resistor / Switched-MOSFET

$$i_o = -[R1/R2]i_{in}$$

$$i_o = -[(W/L)_{M2}/(W/L)_{M1}]i_{in}$$

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### Why Switched-MOSFET ? (1) – Low-voltage operation

#### Conduction Gap of CMOS Switches

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### Why Switched-MOSFET ? (1) – Low-voltage operation

#### Op\_amp input stage

The maximum common-mode input voltage  $V_{CM}$  is around  $V_{DD} - (|V_{Tnp}| + |V_{DSsat}|)$

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### Why Switched-MOSFET ? (2) – Programmability

#### The MOSFET-Only Current Divider (MOCD)

$$a = \sum_{i=0}^{M-1} b_i \cdot 2^{i-M}$$

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### Generation of common-mode voltage

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### Basic SM Integrators

#### 1st Generation Integrator

$$\frac{I_{OA}^+(z)}{I_{in}^+(z)} = -\alpha \frac{1}{1 - \beta z^{-1}}$$

$$\frac{I_{OA}^-(z)}{I_{in}^-(z)} = \gamma \frac{z^{-1}}{1 - \beta z^{-1}}$$

$$\alpha = (W/L)_{M1} / (W/L)_{M11}, \beta = (W/L)_{M2} / (W/L)_{M12} \text{ and } \gamma = (W/L)_{M3} / (W/L)_{M13}$$

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### Basic SM Integrators

#### 2nd Generation Integrator

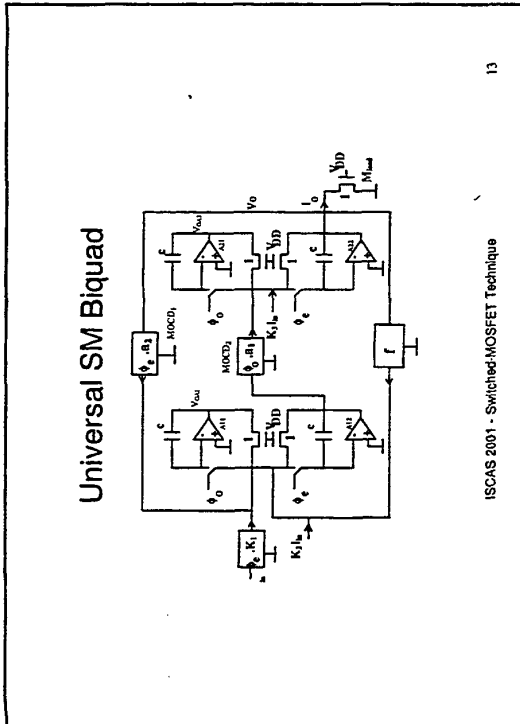
$$\frac{I_{OA}^+(z)}{I_{in}^+(z)} = -\alpha \frac{1}{1 + \beta z^{-1}}$$

$$\frac{I_{OA}^-(z)}{I_{in}^-(z)} = \gamma \frac{z^{-1}}{1 + \beta z^{-1}}$$

$$\alpha = (W/L)_{M1} / (W/L)_{M11}, \beta = (W/L)_{M2} / (W/L)_{M12} \text{ and } \gamma = (W/L)_{M3} / (W/L)_{M13}$$

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### First Conclusions

1. SM does not need any special process or voltage doubler;
2. SM allows independent digital programming of the filter center frequency ( $f_0$ ), quality factor (Q) and gain.
3. Programming is not area demanding.

✦ The SM technique is adequate for the implementation of programmable filters at low-voltage supply.

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### Some practical issues

- 1 - SM technique relies on opamps. Opamp GBW > 3.5 fs (same as for SC circuits) and  $AV_{(DC)} > 77$  dB (linear - easily achievable) for THD < 0.1% (sinusoidal signals).
- 2 - Charge injection will give rise to harmonic distortion. The nonlinearity of the output current is dependent on both the Q-to-V conversion of the holding capacitor and the V-to-I conversion of the MOSFET. Therefore, switches should be minimum-size.
- 3 - In the SM technique, there are no "natural" integrators as in SC circuits. In SC circuits the integrator (non-switched capacitor in the feedback loop of an op amp) is the "natural" element while current amplifier is the "natural" element of the SM technique. Integrators of the SM technique are implemented by feeding back a fraction of the output current to the input. As a consequence of the operating principle of the SM technique, the offset of filters is not as easily compensated as in SC circuits.

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### Some practical issues

- 4- Offset-compensating schemes may be used. In this case, the compensating capacitor contributes to total noise in the same way as holding capacitor, and thus cannot be made very small.
- 5 - Opamps must drive resistive loads. Hence, opamps with class AB output stage should be employed in order to avoid large power consumption.

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### Some practical issues

#### Offset Compensation

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### Some practical issues

#### Offset Compensation / Clock Generation

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### Some practical issues

#### V/I and I/V Converters

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### Some Results

#### Circulating FIR Structure

$y(n) = h_1 x(n) + h_2 x(n-1) + h_3 x(n-2) + h_4 x(n-3)$

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