1.3 Low-voltage ultra-low-power analog IC design — dynamic translinear circuits

Dynamic Translinear Circuits

by Wouter A. Serdijn

Overview

- History of dynamic translinear circuits
- Dynamic translinear principle
- Properties of dynamic translinear circuits
- Dynamic translinear synthesis
- Design of linear and non-linear dynamic functions: a phaselock loop

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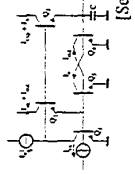
History of dynamic translinear circuits



[Adams, AES '79]

[Seevinck, EL'90]

[Frey, IEE-G'93]

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Mathematical foundation

Electronics design = mapping of a set of mathematical functions on silicon

Exponential mapping

Static translinear: $e^a \cdot e^b = e^{a+b}$

Dynamic translinear: $\frac{d}{dt} e^{x(t)} = \frac{dx(t)}{dt} \cdot e^{x(t)}$

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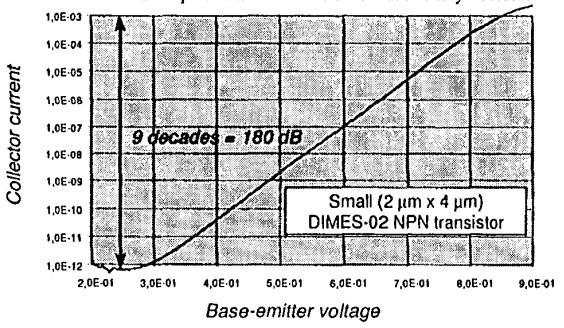
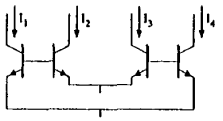
The bipolar transistor

Barrie Gilbert: "Bipolar transistors are nice and friendly devices."



Static translinear principle



Kirchhoff: $V_{BE1} + V_{BE3} = V_{BE2} + V_{BE4}$

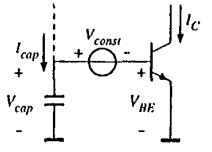
Equal number of transistors in both directions of the loop

$$I_1 I_3 = I_2 I_4$$

$g_m = \frac{I_C}{U_T}$ → transconductance linear with collector current

⇒ translinear

Dynamic translinear principle



capacitance current:

$$I_{cap} = C\frac{dV_{BE}}{dt} = CV_T\frac{\dot{I}_C}{I_C}$$

dynamic translinear principle:

$$CV_T\dot{I}_C = I_C I_{cap}$$

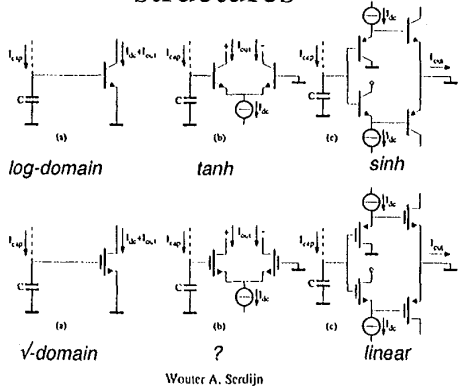
$V_T = \frac{kT}{q}$ = *thermal voltage*

$\dot{I}_C = \frac{d}{dt} I_C$

A time derivative can be mapped on products of currents

⇒ translinear principle

Dynamic translinear output structures



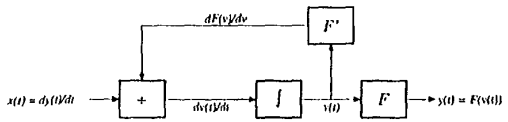
Quality aspects

- Signal-to-noise ratio and dynamic range
- Bandwidth
- Low power
- Low voltage
- Controllability
- Integratability

Signal-to-noise ratio versus dynamic range

- The (maximal) signal-to-noise ratio (SNR) equals the (maximal) ratio of the signal power and the noise power *at the same time*
- The dynamic range (DR) equals the ratio of the maximal signal power and the noise power in the absence of any signals
- The maximal signal power is given by an application-specific specification of the distortion level

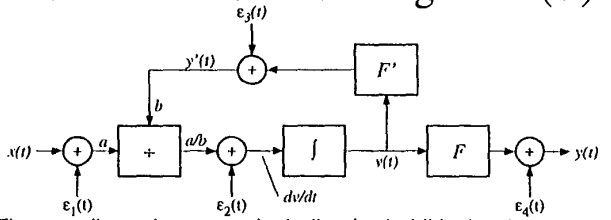
Noise in translinear integrators (I)



general block diagram of a translinear integrator

$$x(t)=\frac{dy(t)}{dt}=\frac{dy(t)}{dv(t)}\cdot\frac{dv(t)}{dt}=\frac{dF}{dv}[v(t)]\cdot\frac{dv(t)}{dt}$$

Noise in translinear integrators (II)



The translinear integrator including its (additive) noise sources

$$S_y(\omega,t)=\frac{S_x(\omega,t)}{\omega^2}+\frac{S_{\varepsilon_1}(t)}{\omega^2}+S_{\varepsilon_3}(t)\cdot\frac{E_x[G_1^2(x,t)]}{\omega^2}+S_{\varepsilon_2}(t)\cdot\frac{E_x[G_2^2(x,t)]}{\omega^2}+S_{\varepsilon_4}(t)$$

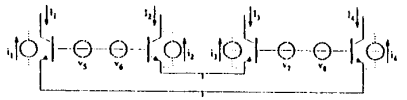
$$G_1(x,t)=\frac{x(t)}{G_2(x,t)}=\frac{dF}{dv}\left[F^{-1}\left(\int_t x(\tau)d\tau\right)\right]$$ ⇒ Signal × noise intermodulation

Noise

- Noise in linear circuits:
  - Is wide-sense stationary
  - Can be represented by independent noise sources
  - Can be transformed independently of the signal
- Noise in non-linear circuits:
  - Is non-stationary
  - Must be modeled by signal-dependent noise sources
  - Noise << signal ⇒ linear time-varying approximation

Non-stationary noise

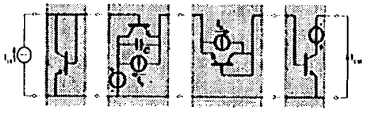
- Multiplication of currents ⇒ signal × noise intermodulation (aliasing)



$$(I_1 + i_1)(I_3 + i_3) = (I_2 + i_2)(I_4 + i_4) \cdot \exp\left(\frac{v_5 + v_6 + v_7 + v_8}{U_T}\right)$$

- Noise level increases with the signal power
- Saturation of the SNR

Dynamic translinear noise



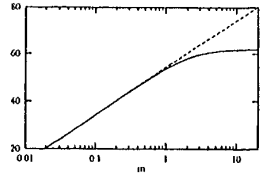
- $SNR_Q \sim I_C$
- Q_2 and Q_3 determine SNR_{max}

$$\frac{1}{2} \cdot \frac{I_o^2}{qI_o \cdot \frac{I_o}{2CU_T}} = \frac{CU_T}{q}$$

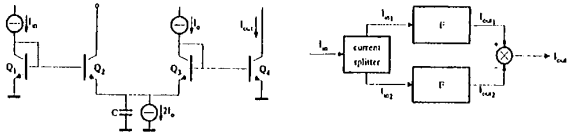
Collector current power

Noise power spectral density

Noise bandwidth

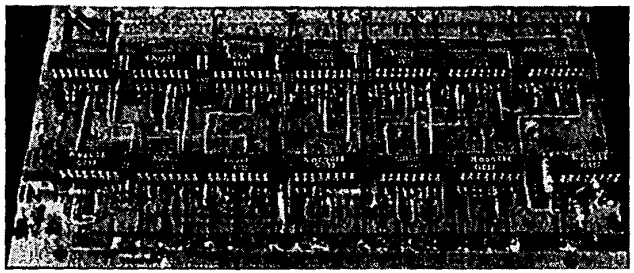


Noise in class AB



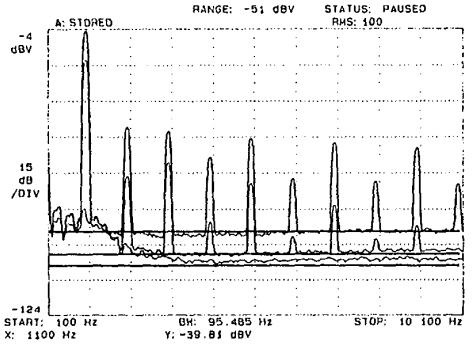
- Signal >> bias current ⇒ noise behavior strongly non-linear ⇒ DR > SNR_{max}
- Harmonic decomposition into two class-AB signals requires a good matching of both signal paths to prevent distortion

Photograph



Breadboard realization.
For biasing purposes the integrator is enclosed in a unity-feedback configuration

Experimental results (I)



Experimental results (II)

Quantity	Value	Comment
Cutoff frequency	1.6 kHz	C = 100 nF, I_F = 26 nA, room temperature
Maximum SNR	63 dB	for 1-kHz, 400-nA (RMS) input signal and 2 % output THD
Dynamic range	76 dB	ditto
Supply voltage	3.3 V	
Quiescent current	310 nA	

Quality aspects: signal-to-noise ratio and dynamic range

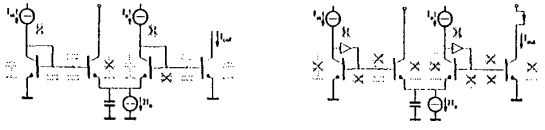
- The fundamental limit of DTL circuits, $SNR_{DTL,max} = CU_T/q = CU_T^2/kT$, is always smaller than the fundamental limit of linear circuits, $SNR_{lin,max} = CV_{DD}^2/4kT$
- Class-AB operation extends the dynamic range of DTL circuits at the upper side
- Due to out-of-band signals, the SNR deteriorates. Therefore, DTL filters are better suited for shaping than for selection.

Quality aspect	DTL (class A)	DTL (class AB)	linear
SNR	–	–	+
DR	–	++	+

Bandwidth

- Bandwidth of linear circuits:
  - Independent of the signal
  - Eigenvalues are equivalent to poles
  - Stability and frequency behavior are equivalent
- Bandwidth of non-linear circuits
  - Depends on the signal
  - Eigenvalues and poles are not equivalent
  - Stability and frequency behavior are not equivalent

Quality aspect: bandwidth (I)



$$I_{in} + \underbrace{\frac{C_{par}U_T}{I_O}\left(\frac{\dot{I}_{in}I_{out} - \dot{I}_{out}I_{in}}{I_{in}}\right)}_{\text{additional non-linear term resulting from } C_{par}} = \frac{CU_T}{I_O}\dot{I}_{out} + I_{out}$$

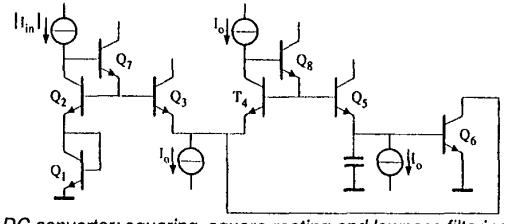
Bandwidth (II)

- In DTL circuits, the voltage excursions are small ⇒ effects of parasitic capacitances are reduced ⇒ relatively wide bandwidth operation

Quality aspect	DTL	MOSFET-C	gm-C
Bandwidth	+	–	++

Quality aspect: low power

- A high functional density
- No resistors ⇒ especially interesting for ultra low power



An RMS-DC converter: squaring, square-rooting and lowpass filtering in a six-transistor dynamic-translinear core

Quality aspect: low voltage

- In DTL circuits, the voltage excursions are small ⇒ beneficial in a low-voltage environment
- The supply voltage of DTL circuits must be larger than one junction voltage and two current-source voltage drops ⇒ 1V

Quality aspect	DTL	MOSFET-C	gm-C
Low voltage	+	–	+

Quality aspect: controllability

- DTL filters are easily controlled by currents over a wide range of parameters
  - Good designability
  - Standard cells
  - Programmable building blocks

Quality aspect: integratability

- In DTL circuits, only three types of components are required:
  - Well-matched, purely-exponential transistors
  - Large-gain, high-f_T transistors
  - Capacitors
- Thus
  - Possible to implement linear or non-linear polynomial differential equations, using only transistors and capacitors
  - A high functional density
  - No resistors ⇒ especially interesting for ultra low power

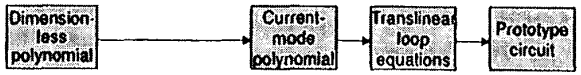
Quality aspects of dynamic translinear circuits in general

Quality aspect	ranking	comment
SNR/CNR	–	for large input currents the SNR saturates
DR	++	due to companding the DR can be very high
Linearity	+	exponential over a wide range of currents
Bandwidth	+	high functional density
Low power	+	high functional density
Low voltage	++	minimum voltage loss over the devices
Controllability	++	all parameters are current-controlled
Integratability	++	only transistors and capacitors are required

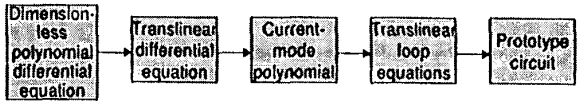
Application areas

- Filters [almost every conference, workshop or colloquium] for shaping, not for selection. E.g., a reconstruction filter
- RMS-DC converter [ESSCIRC'96, JSSC'97]
- Oscillator [ESSCIRC'97, JSSC'98]
- Phase detector [Payne et al., El. Lett. 1997]
- Infra-red front-end (amplifier and AGC function)
- QPSK demodulator (quadrature oscillator, mixing and filtering of I and Q) [ISCAS'99]
- Subminiature hearing-aid adapter [ISCAS'00]
- Artificial dendrite (DTL Hodgkin-Huxley)

Synthesis procedure

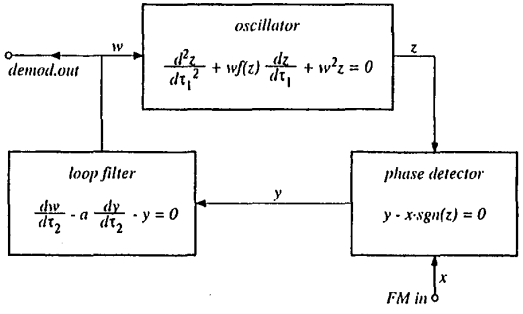


Static translinear circuits



Dynamic translinear circuits

(Second-order) PLL design



Transformations (I)

$$w = \frac{I_F}{I_{O1}}$$

$$x = \frac{I_{in}}{I_{O1}}$$

$$y = \frac{I_D}{I_{O1}}$$

$$z = \frac{I_{osc}}{I_{O1}}$$

Transformations (II)

$$\frac{d}{d\tau_i} = \frac{C_i V_T}{I_{01}} \frac{d}{dt}$$

- Time (t) is inversely proportional to current I_{01}
- I_{01} must be proportional to the absolute temperature (PTAT) to eliminate the influence of the temperature on the PLL

Transformations (I + II)

$$C_1^2 V_T^2 \ddot{I}_{osc} + C_1 V_T I_F f(I_{osc}, I_F) \dot{I}_{osc} + I_F^2 I_{osc} = 0$$
$$C_2 V_T \dot{I}_F - a C_2 V_T \dot{I}_D - I_D I_{01} = 0$$
$$I_D - I_{in} \operatorname{sgn}(I_{osc}) = 0$$

PLL properties

- the 'CCO gain factor' $K_{osc} = 1/V_T C_1$
- the phase detector gain $K_d = 4I_{in}/\pi$
- the loop gain $K = aK_{osc}K_d$
- the natural frequency of the loop, $\omega_n = \sqrt{\frac{K_{osc} K_d I_{01}}{V_T C_2}}$
- the damping factor $\zeta = \frac{\omega_n a V_T C_2}{I_{01}}$
- ...

Definition of the capacitance currents

- Each capacitance current reduces the order of the differential equation by one, until finally a set of current-mode multivariant polynomials results.
- Result:

$$FI_{cap2} I_F + I_{cap1}(I_{cap2} + I_F)(I_F + I_{osc}) - I_F[I_{cap2}(I_F + I_{osc}) - I_F I_{osc}] = 0$$
$$I_{cap3}(I_F - aI_D) - I_D I_{01} = 0$$
$$I_D - I_{in} \operatorname{sgn}(I_{osc}) = 0$$

Translinear decomposition (I)

- Aim: always positive collector or drain currents
- Often: parametric decomposition, i.e. introduction of 'intermediate' currents
- F must be a non-linear time-invariant odd-symmetry function of I_{osc} and I_F, whose derivative f with respect to I_{osc} is negative for small values of I_{osc} and positive for large values of I_{osc}. A suitable choice is

$$F = 2I_{osc} - \frac{2GI_{osc}I_F^2}{I_{osc}^2 + I_F^2}$$

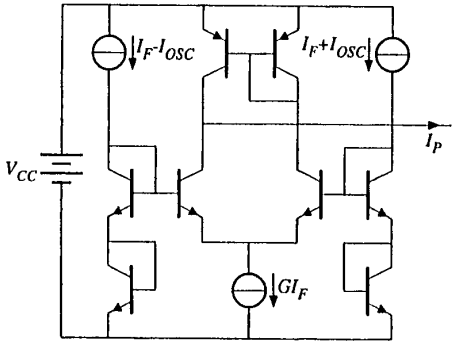
Translinear decomposition (II)

oscillator:
$$\begin{cases} (I_F + I_P - I_Q)I_F = (I_F + I_{cap1})(I_{osc} + I_F) \\ (I_F + I_P)I_F = (I_F + I_{cap2})(I_Q + I_F) \\ I_P = 2I_{osc} - F(I_{osc}, I_F) \end{cases}$$

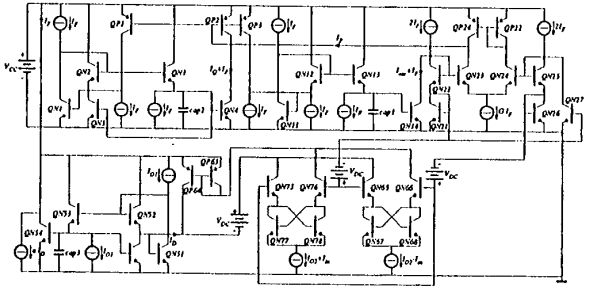
loop filter: $[(1-a)I_D + I_F]I_{O1} = (I_F - aI_D)(I_{cap3} + I_{O1})$

phase detector:
$$\begin{cases} \left(I_{O2} + \frac{I_{in}}{2}\right)\mathrm{sgn}(I_{osc}) = I_R \\ \left(I_{O2} - \frac{I_{in}}{2}\right)\mathrm{sgn}(I_{osc}) = I_S \\ I_D = I_R - I_S \end{cases}$$

Implementation of $I_p(F)$



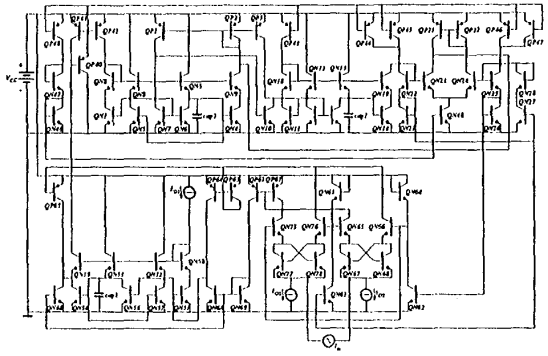
Possible biasing arrangement



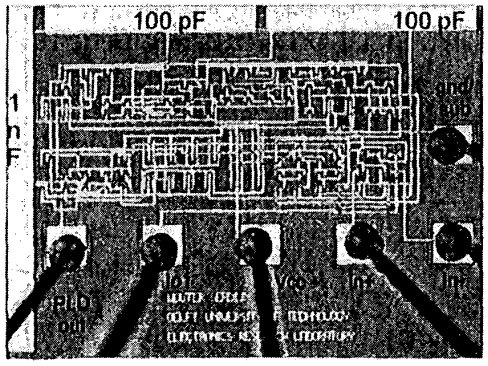
Design example: the PLL as an FM detector

- f_c = 100 kHz
- Δf = 40 kHz
- ζ = 0.9 (pull-in time and noise bandwidth), $C_1 = C_2$ = 100 pF, C_3 = 1 nF
- Semicustom version (SIC2A) of 2-μ, bipolar IC process (DIMES-02, $h_{fe,\mathrm{NPN}} = 100$, $f_{T,\mathrm{NPN}} = 7$ GHz, $h_{fe,\mathrm{LPNP}} = 80$, $f_{T,\mathrm{LPNP}} = 40$ MHz), G = 5/4 by design
- Supply voltage: 2 V

Circuit diagram



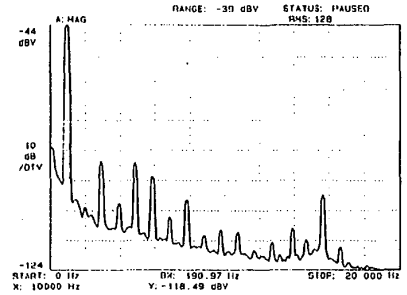
Micrograph



Measurement results (I)

- f_c = 100 kHz:
- Supply voltage: 1.5 V - 5 V
- Current consumption: 17 I_F + 8 I_{O1} = 40 μA
- Hold-in range: 40 kHz - 150 kHz
- Lock-in range: 55 kHz - 150 kHz

Measurement results (II)



- Δf = 40 kHz (!), f_m = 1 kHz, THD < 1 %
- SNR (B = 10 kHz) = 57 dB