# IDENTIFYING TRANSLINEAR LOOPS IN THE CIRCUIT TOPOLOGY

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**ABSTRACT**

This paper presents a topological method for identifying multiple static translinear loops using a graphical representation. It is found that the translinear principle has a new formulation based on graph theory concepts and it is applied to circuits containing BJTs and MOS transistors. In addition, it is introduced the concept of translinear circ for representing a translinear loop. The types of interaction between translinear loops are studied and its properties are established. The method is illustrated with a generic example.

## 1. INTRODUCTION

The translinear principle introduced by Gilbert [1] provides a way to analyze and synthesize circuits that exploit the exponential current-voltage characteristic present in the BJTs. In [2], the principle has been generalized and extended to circuits containing MOS transistors operating in strong inversion.

A novel class of translinear circuits taking into account the presence of the bulk terminal of MOS transistors operating in the weak inversion (both saturated and ohmic) regimes was proposed in [3]. In addition a symbolic representation for MOS transistors is used for identifying translinear loops.

This paper shows how multiple translinear loops (TLs) can be identified using graph theory concepts in circuits containing MOS transistors and BJTs. Graphical models for BJTs operating in the active region and MOS transistors operating in the weak inversion (both subthreshold and ohmic) regimes are introduced. These models are based on Serrano's work [3]. The method proposed here allow us to know possible interactions between translinear loops, and some properties related with translinear loops are established.

The main result of this work is to find a graphical representation that can be used for the future development of a verification tool that plays an important and fundamental role in the structured design of translinear circuits.

The paper is divided into six Sections. Models and basic notations are established in Section 2. Section 3 presents the new formulation of the translinear principle and the Section 4 presents a method for identifying loops. Section 5, focusses on presenting a classification for translinear loops and analyzing its properties. Section 6 concludes the paper.

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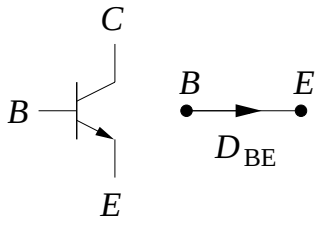


Figure 1: Graphical equivalent for NPN bipolar transistors.

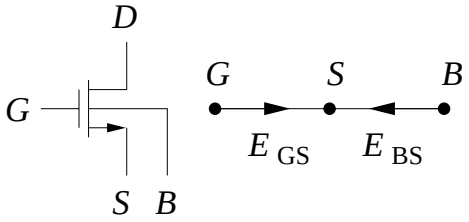


Figure 2: Graphical equivalent for the NMOS transistor operating in the subthreshold regime.

## 2. MODELS AND BASIC NOTATIONS

### 2.1. Graphical Equivalent for BJTs

Each NPN BJT will be modeled by the Ebers-Moll schematic and its graphical equivalent will contain an edge as shown in Figure 1. A PNP transistor will be modeled by a similar graphical equivalent to the shown in the figure 1, but the direction of the edge is inverted.

### 2.2. Graphical Equivalent for MOS transistors

A NMOS transistor operating in the saturated subthreshold regime will be represented by a pair of edges as shown in Figure 2, since both the GS and the BS junction are part of two coupled TL loops.

A NMOS transistor operating in the ohmic subthreshold regime will be represented by a set of four edges as shown in Figure 3, since this ohmic device will have four junctions that can be part of several TL loops.

A PMOS transistor will be modeled by a similar graphical equivalent to the one shown in Figures 2 and 3, but all directions of the edges are inverted.

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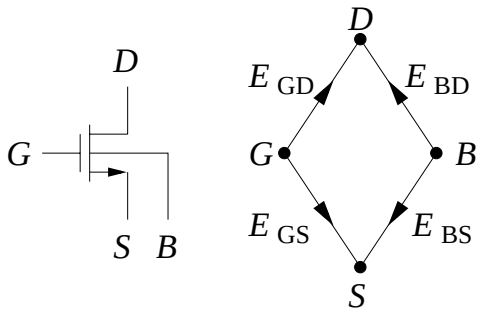


Figure 3: Graphical equivalent for the NMOS transistor operating in the ohmic regime.

### 3. TRANSLINEAR PRINCIPLE

In this Section, a new concept is introduced taking into account a previous definition called *circ* [4]. A translinear loop can be represented by a translinear circ. A *translinear circ* $TC$ is a connected finite alternating sequence of vertices and directed edges

$$v_1, e_1, v_2, e_2, \ldots, v_{n-1}, e_n, v_1$$

whose $n$ vertices $v_i$ are distinct and where each edge represents a translinear element. A translinear circ has an equal number of edges oriented in the clockwise (CW) direction and edges oriented in the counterclockwise (CCW) direction.

A simple derivation of the translinear principle for a single loop containing $N$ idealized translinear elements can be expressed as follows [3]:

**Theorem 1** *In a translinear circ ($TC$), containing an equal number of oppositely connected edges, the product of the normalized currents in the edges connected in the clockwise (CW) direction is equal to the corresponding product for edges connected in the counterclockwise (CCW) direction.*

In a translinear circ (translinear loop), the sum of voltage drops adds to zero. Applying Kirchhoff's voltage law to the translinear circ, the following holds:

$$0 = \sum_{j \in \{CW\}} V_{e_j} - \sum_{l \in \{CCW\}} V_{e_l} \tag{1}$$

where $e$ represents an edge (translinear element). For each edge,

$$V_e = K \ln\left(\frac{I}{I_d}\right) \tag{2}$$

where $K$ is equal to $V_T$ for BJT's, $nV_T$ for the GS junction of MOST's or $k$ for the BS junction of MOST's, $k$ being equals to $n/(n-1)$, approximately 3 when $n$ approximates 1.5, which is often found in practice. $V_T$ equals the thermal voltage $kT/q$, approximately 26 mV at room temperature. $I_d$ is the transistor current. Then, using (2) in (1) and assuming the loops to be composed of equivalent devices, this results in:

$$0 = K \sum_{j \in \{CW\}} \ln\left(\frac{I_j}{I_d}\right) - K \sum_{l \in \{CCW\}} \ln\left(\frac{I_l}{I_d}\right)$$

so

$$0 = K \ln\left(\frac{\prod_{j \in \{CW\}} I_j}{\prod_{l \in \{CCW\}} I_l} \frac{\prod_{l \in \{CCW\}} I_d}{\prod_{j \in \{CW\}} I_d}\right)$$

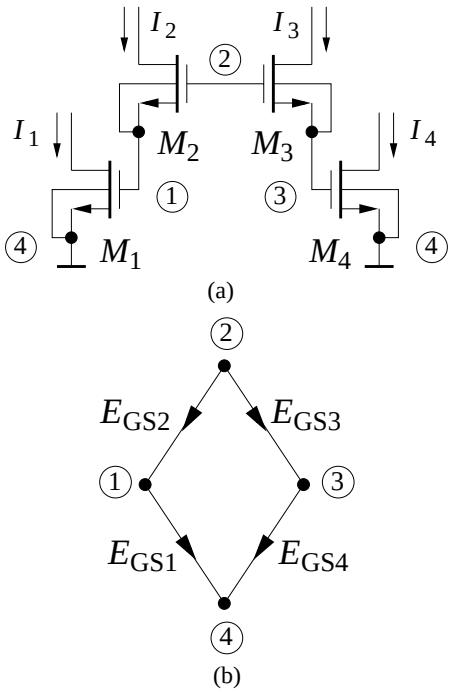


Figure 4: MOS translinear loop. (a) Circuit schematic representation. (b) Graphical equivalent.

and thus

$$1 = \frac{\prod_{j \in \{CW\}} I_j}{\prod_{l \in \{CCW\}} I_l} \frac{\prod_{l \in \{CCW\}} I_d}{\prod_{j \in \{CW\}} I_d}. \tag{3}$$

Since the number of CW-oriented edges is equal to the number of CCW-oriented edges, the $I_d$ coefficients in (3) cancel out, thus resulting in

$$\prod_{j \in \{CW\}} I_j = \prod_{l \in \{CCW\}} I_l. \tag{4}$$

Note that the logarithm of the weight of each edge corresponds to the voltage drop across a translinear element in the loop. Then, the sum of the weights of the edges oriented in the clockwise direction is equal to the total weight of the edges oriented in the counterclockwise direction.

$$\sum_{j \in \{CW\}} W_{e_j} = \sum_{l \in \{CCW\}} W_{e_l} \tag{5}$$

To illustrate Theorem 1, the circuit shown in Figure 4 is analyzed. The circuit has a single translinear loop containing four identical translinear elements, two of which face in the clockwise direction and two of which face in the counterclockwise direction. In Fig. 4(a) a circuit schematic representation implemented with MOS transistors is shown. Fig. 4(b) shows the same loop, but the graphical equivalent is used. The $E_{BS}$ edges are not shown because their terminals are short circuited together and they will not have any effect on the circuit behaviour.

## 4. TOPOLOGICAL METHOD

The aim of the method is to find the topological equivalent called translinear circ embedded in the dead graph of the circuit. A dead graph is the graph obtained by eliminating all independent sources, i.e. the voltage sources and current sources are transformed into short circuits or open circuits, respectively. A first consequence of this fact is the following property.

**Property 1** *A circuit is translinear if one or more translinear circs are found embedded in the resulting dead graph of the circuit.*

Each device present in the circuit will be replaced by a graphical equivalent. The resulting dead graph will be formed by a set of graphical equivalents. The purpose of the method is to identify the devices involved in each translinear loop. A translinear circuit may consist of more than one translinear loop.

A systematic method can be implemented to realize this identification using the dead graph of the circuit.

The method can be recast in the next steps:

1. Find a translinear circ that represents a fundamental translinear loop.
2. Extract the information about each edge of the translinear circ.
3. Enumerate the devices involved.
4. Repeat the whole procedure (if posssible) again.

Fig. 5 illustrates this method. In Fig. 5-(a) a translinear circuit containing BJTs is presented [5]. The dead graph of the circuit is shown in the figure 5-(b). The application of the method allow us identify a pair of embedded translinear loops in the circuit topology. The first loop is formed by $Q_1 - Q_2 - Q_3 - Q_4$. The second loop is formed by $Q_5 - Q_6 - Q_7 - Q_4$. Fig. 6 shows the translinear loops represented by translinear circs.

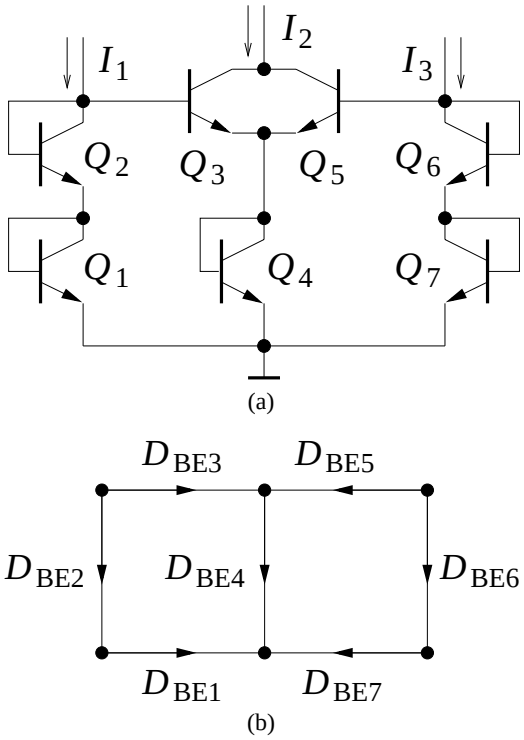


Figure 5: A BJT translinear cell. (a) Circuit schematic representation. (b) Graphical representation.

## 5. CLASSIFICATION AND PROPERTIES OF TRANSLINEAR LOOPS

The presence of more than one translinear loop allow us to define some properties of the different loops involved and classify them. The classification is established by taking into account the following definitions. Note that the term translinear circ is the graph theory concept used for representing a translinear loop.

**Definition 1** *A translinear circ is said to be fundamental if its elements produce multiplications of currents.*

**Definition 2** *A translinear circ is said to be trivial if it contains no multiplications of currents.*

**Property 2** *A translinear circuit have $L$ fundamental translinear circs. The number of fundamental loops is given by $L = N_{TE} - N_V + 1$ where $N_{TE}$ is the number of translinear elements and $N_V$ is the number of vertices of the circuit.*

As an example, consider the translinear cell depicted in Figure 5. Here $L = 7 - 6 + 1 = 2$.

Different translinear circs can either be disjoint or coupled. Coupled loops can be coupled directly or indirectly.

**Definition 3** *Two translinear circs are said to be coupled directly if they have one or more edges in common.*

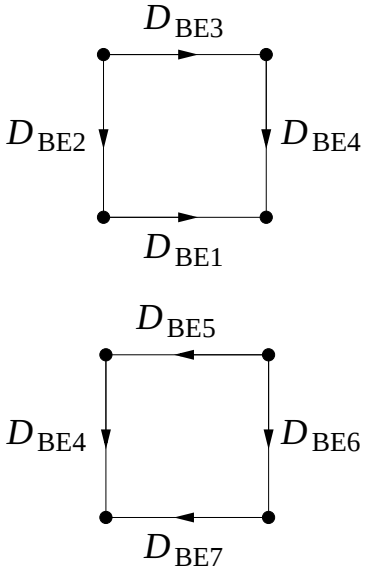


Figure 6: Embedded translinear loops in the circuit of Figure 5.

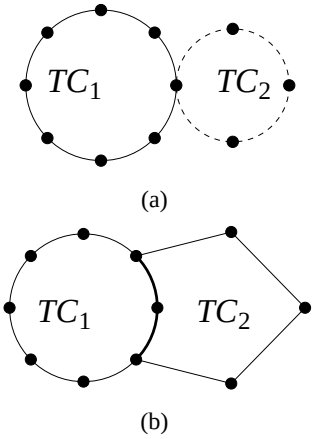


Figure 7: (a) Coupled indirectly translinear circs. (b) Coupled directly translinear circs.

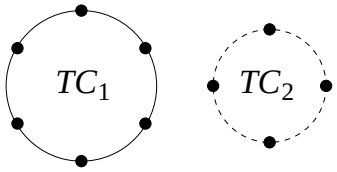


Figure 8: Disjoint translinear circs.

**Definition 4** *Two translinear circs are said to be coupled indirectly if they have a vertex in common.*

**Definition 5** *Two translinear circs are said to be disjoint if they belong to two disjoint graphs.*

**Property 3** *If coupled translinear circs exist in a dead graph, then more than L different translinear circs are present.*

The possible elements are BJTs and MOS transistors. When a mixed loop appears, an equal number of devices of each type of device must be present.

**Definition 6** *A translinear circ is said to be pure circ, if the circ contains a unique type of possible devices.*

**Definition 7** *A translinear circ is said to be mixed circ, if the circ contains both types of possible devices.*

**Property 4** *A translinear loop contains at least two elements.*

**Property 5** *Let $TC_1$ and $TC_2$ be different translinear circs and $G_s = TC_1 \cap TC_2$, then $G_s$ is either*

1. *A vertex (coupled undirectly circs), or*
2. *A path (coupled directly circs), or*
3. *An empty set.*

As an example, consider the pair of translinear circs in Figure 6. The application of Property 6 allow us to obtain the graph shown in Figure 9. The resulting graph is a path composed by one edge.

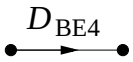


Figure 9: The application of the Property 6 to the translinear circs shown in Figure 6.

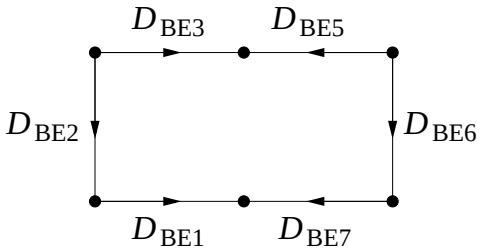


Figure 10: The application of the Property 7 to the translinear circs shown in Figure 6.

**Property 6** *Let $TC_1$ and $TC_2$ be different translinear circs and $G_s = TC_1 \oplus TC_2$, where $oplus$ denotes the factored graph notation, then $G_s$ is either*

1. *A translinear circ, or*
2. *The union of disjoint translinear circs.*

As an example, consider the pair of translinear circs in Figure 6. The application of Property 7 allow us to obtain the graph shown in Figure 10. The resulting graph is a translinear circ.

## 6. CONCLUSIONS

A method based on graph theory concepts for identifying translinear loops is provided. Concepts related with the interaction between translinear loops are studied. The new formulation is used for analyzing and searching embedded multiple translinear loops (represented by translinear circs) in a circuit topology (represented by a graph). A classification and several properties for translinear loops are derived. In addition, the method can be easily modified to identify dynamic translinear loops. Further work is the development of a verification tool used in a future structured analog design methodology for translinear circuits.

## 7. REFERENCES

[1] B. Gilbert, "Translinear Circuits: A Proposed Classification," *Electronics Letters*, vol. 11, no. 1, pp. 14–16, January 1975.

[2] E. Seevinck and R.J. Wiegerink, "Generalized Translinear Circuit Principle," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 8, pp. 1098–1102, August 1991.

[3] T. S. Gotarredona, B. L. Barranco, and A. G. Andreou, "A General Translinear Principle for Subthreshold MOS Transistors," *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, vol. 46, no. 5, pp. 607–616, May 1999.

[4] L.M. Maxwell and M. B. Reed, *The Theory of Graphs: A Basis for Network Theory*, Pergamon Press, 1971.

[5] B. Gilbert, "Translinear Circuits: An Historical Overview," *Journal of Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers*, vol. 9, pp. 95–118, 1996.