A New CMOS Current Conveyors based Translinear Loop for Log-domain Circuit Design

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Abstract

A novel topology for Translinear (TL) loops comprising of CMOS Second Generation Current Conveyors (CC-II) and diodes is proposed. The proposed methodology opens a new paradigm towards the design of Static and Dynamic TL circuits in CMOS technology. Simulation of a current multiplier and a Log-domain integrator demonstrates the concept.

1. Introduction

The on-going trend towards lower supply voltages and lower-power operations has brought the area of analogue integrated filters into limelight. In conventional filter implementation techniques using Opamp–MOSFET–C, transconductance–C and switched capacitors, the supply voltage restricts the attainable maximum dynamic range. Further, the use of linear resistors in low-power environment demands large silicon area for on-chip integration and hence renders impractical. High frequency of operation and the requirement for tunability of the filter complicates the situation further.

TL filters are based on Dynamic Translinear (DTL) principle [1], which is a generalization of Static TL (STL) principle formulated by Gilbert in 1975 [2]. Gilbert's Translinear principle provides a simple and efficient way of analysing and synthesizing non-linear circuits based on Bipolar Junction Transistors (BJT). Both static & dynamic TL circuits exploit the exponential function, which is at the base of relation between collector current and base emitter voltage of a BJT [3] or between drain current and gate to source voltage of a MOS transistor in weak inversion region [4]. In a MOS/CMOS based implementation of TL circuit, the current range where the approximately exponential I-V characteristic can be used, is limited to typically three decades. compared to more than six decades for BJT, which restricts the choice and optimization of operating point within the weak inversion region. Another fundamental limitation of the weak inversion MOS transistors is the poor matching of threshold voltages, which affects the distortion performance of CMOS log-domain filters. Further, TL circuits implemented in CMOS technology, operating in sub-threshold region, suffer from low bandwidth limitations.

Although, a topology for TL filters in CMOS IC technology is presented [6], no generalization could be done for implementation of higher order filters. The topology proposed in this paper generalizes the concept to ease the implementation of DTL (as well as STL) & log-domain circuits in CMOS technology.

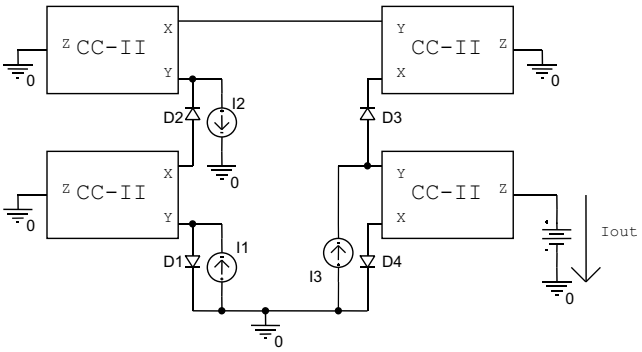

Figure 1: The Proposed Translinear loop using Current Conveyors

2. CMOS CC Based TL circuit principle

The CC-II based TL loop proposed is shown in Fig. 1. This technique allows decoupling of the exponential behavior and gain, where CC-II at the output provides the gain, whereas the diodes (also implemented in CMOS technology) take care of the exponentiation. An alternate topology with diodes D_2 and D_3 reversed is also possible but that requires higher voltage supplies. Using the I-V relationship of the diodes and the voltage tracking properties of the CC-II, the loop formed by the diodes D1 - D4 gives,

$$I_{D1} * I_{D3} = I_{D2} * I_{D4} \quad (1)$$

where I_{Dx} is the current through diode D_x.

The above equation shows the multiplier/divider behavior of the circuit in Fig. 1. Cascading more CCs and diodes can expand the TL loop further as shown in Fig. 2. An

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expansion where the diodes are connected in toggled manner (alternate diodes in opposite direction) does not require any increase in the supply voltages. For such a loop, the generalized equation is given by,

$$\prod_{k=1}^{3,5,\ldots} I_{D_k} = \prod_{j=2}^{4,6,\ldots} I_{D_j} \qquad (2)$$

where I_{Dx} is the current through diode D_x.

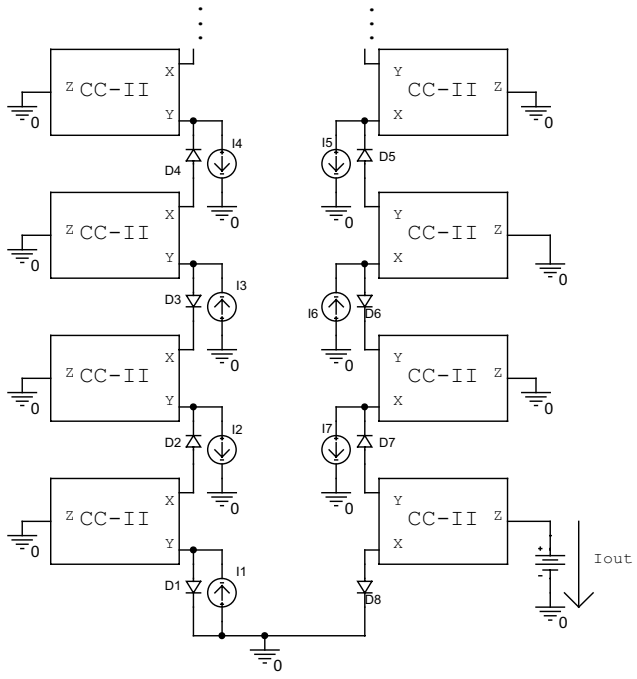

Figure 2: The Extended TL loop using Current Conveyors

Linear and nonlinear functions (differential equations) can be implemented by DTL circuits. As an example, a lossy integrator is implemented as shown in Fig. 3(a). This design is not meant for optimization with respect to the number of current conveyors used, however, the generalization of the CC-II based TL loop is proved for DTL circuits. The Transfer function of the integrator can be derived as follows. For the TL loop in Fig. 3(a) and using Eqn. 1, we get,

$$I_{in} * I_3 = I_{out} * (I_2 + I_c) \qquad (3)$$

the current through a capacitor depends upon the time derivative of the voltage across it, therefore, we get,

$$I_2 I_{out} + CV_t I_{out} * (\frac{\dot{I}_{out}}{I_{out}}) = I_{in} I_3 \qquad (4)$$

where V_t is Thermal voltage and $\dot{I}_{in}$ denotes time derivative of I_{in} ,or, in s-domain,

$$\frac{I_{out}}{I_{in}} \approx \frac{I_3}{I_2 + sCV_t} \qquad (5)$$

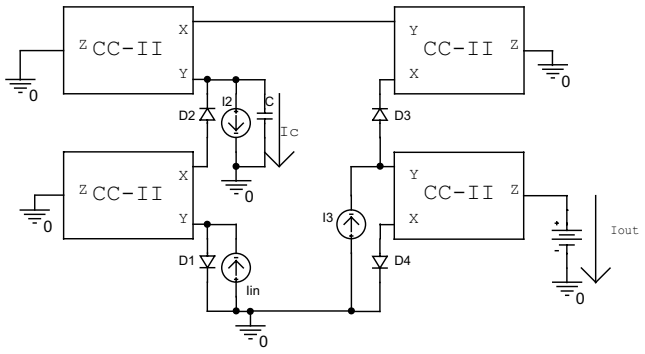

Figure 3(a): The Integrator formed using the proposed topology

The equation shows that the circuit in Fig. 3(a) behaves as a lossy integrator with corner frequency (ω_c) given by,

$$\omega_c = I_2 / CV_t \qquad (6)$$

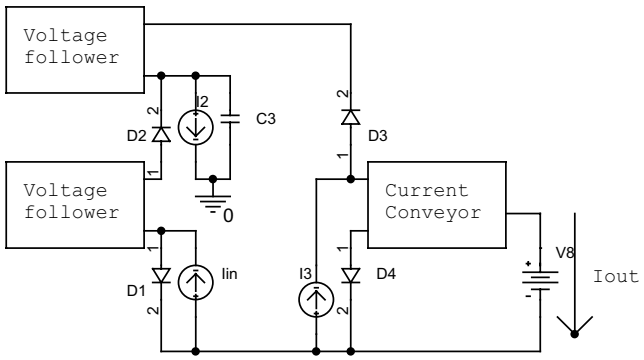

Figure 3(b): The Optimized Integrator

The circuit shown in Fig. 3(a) can be optimized as shown in Fig. 3(b) to save silicon area as well as the power dissipation. This design does not change the output function or any other performance characteristics circuit, however in this case, we do not have any generality.

A Biquadratic filter is also formed to demonstrate the application of the loop in filter design. The filter is formed using an Integrator-Integrator topology as shown in Fig. 4.

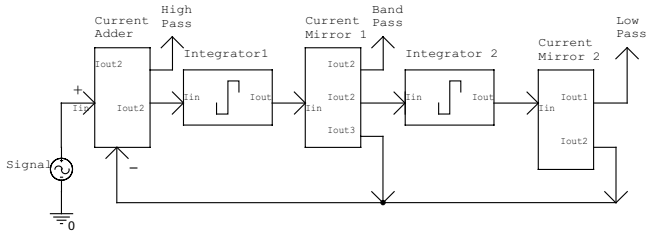

Figure 4: The Integrator-Integrator topology

The integrators were realized with the help of the CC-II TL loop as shown in Fig. 3(a) and cascaded with the help

of simple mirrors. The expressions for Low Pass, High Pass and Band Pass Transfer functions, Center Frequency (W_o) and Quality Factor (Q) are shown in Table 1. From the table, it can be easily inferred that the capacitor tuning as well as the current tuning can control all these parameters.

Table 1.
Transfer functions of the Biquad

High-Pass	$\frac{s^2 + (a+b)s + ab}{s^2 + (W_o/Q)s + W_o^2}$
Band - Pass	$\frac{s + b}{s^2 + (W_o/Q)s + W_o^2}$
Low – Pass	$\frac{1}{s^2 + (W_o/Q)s + W_o^2}$
Center Frequency (W_o)	$\sqrt{\frac{I_3(I_{12}+I_{13}) + I_2 I_{12}}{C_1 C_2 V_t^2}}$
Quality Factor (Q)	$\frac{\sqrt{C_1 C_2 \{I_3(I_{12}+I_{13}) + I_2 I_{12}\}}}{I_2 C_2 + I_{12} C_1 + I_3 C_2}$

In Table 1, $a = \frac{I_2}{C_1 V_t}$, $b = \frac{I_{12}}{C_2 V_t}$, $A = \frac{I_3}{C_1 V_t}$, $B = \frac{I_{13}}{C_1 V_t}$ and I_2, I_3 are currents through diodes D_2 and D_3 in Integrator-1 (as shown in Fig. 3(a)) whereas I_{12} and I_{13} are similar currents in Integrator-2 (as shown in Fig. 4).

3. Simulation and Results

PSpice simulations have been carried out for the circuits shown in Fig. 1, 2, 3(a) and 3(b) in which class AB current conveyors (shown in Fig. 5) as proposed in [8] have been used with VDD=1V, VSS=-1V, VB1=VB2=0V and aspect ratios of M19, M20 and M21 set to 1. The Voltage followers used in Fig. 3(b) were also realized by the same design but with M17 and M18 removed, thus resultant circuit acting only as a voltage buffer. Device model parameters were taken from MIETEC 0.5um CMOS process.

The multiplication/division action of the STL depicted in Fig. 1 for three values of Multiplication factor (MF) ($=I_3/I_2$) is shown in Fig. 6. This is in conformity with Eqn. 1. The error (found to be less than 0.5%) in the output corresponds to the finite offsets of the CCs.

The AC characteristics of the integrator at Fig. 3(a) are shown in Fig. 7 and Fig. 8 with I_{in} = 1uA(DC) + I_{signal}, I_3 = I_4 =1uA and C=100nF. The Maximum operating frequency was found to be 3.4MHz. The power consumed by the Integrator at the bias conditions was found to be 300uW. The AC characteristics of the optimized integrator at Fig. 3(b) were similar to those shown in Fig. 7 and Fig. 8. However, the power consumed by the optimized integrator was found to be 40% less.

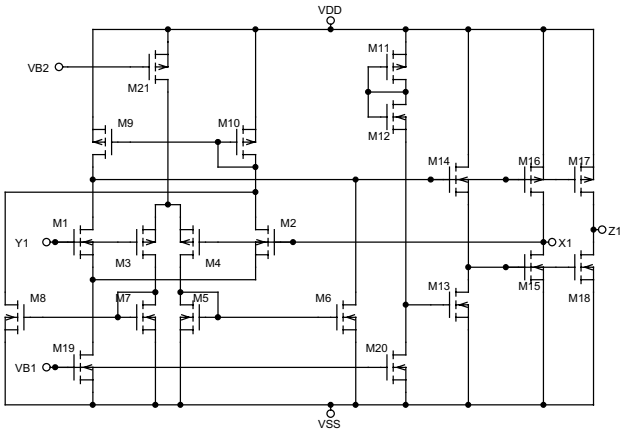

Figure 5: Class AB Current Conveyor Circuit

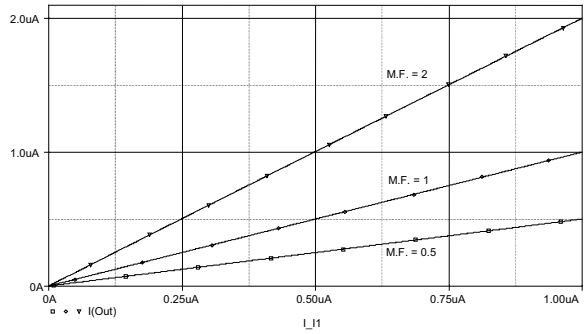

Figure 6: Multiplication/Division characteristics

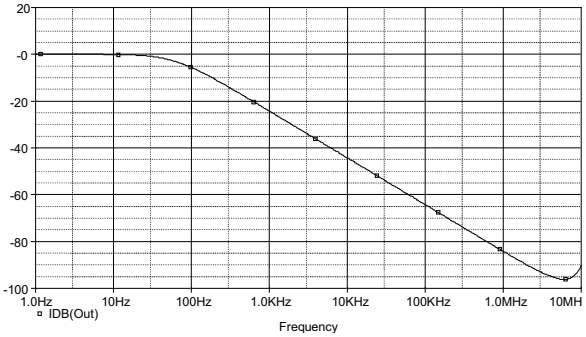

Figure 7: Magnitude Frequency Plot of the Integrator

The output signal integrity was also verified from the transient response (shown in Fig. 9) carried out with I_{in} = 1uA(DC) + 100nA(AC), C = 10nF and I_3= I_4 = 1uA at frequency 1KHz. THD calculated up to 100KHz was found to be less than 0.5%.

The Corner Frequency tuning and gain variation with current I_2 and the gain variation with current I_3 are shown in Fig. 10 and Fig. 11 respectively which were found to be in accordance with the theoretical values as given by Eqn. 5.

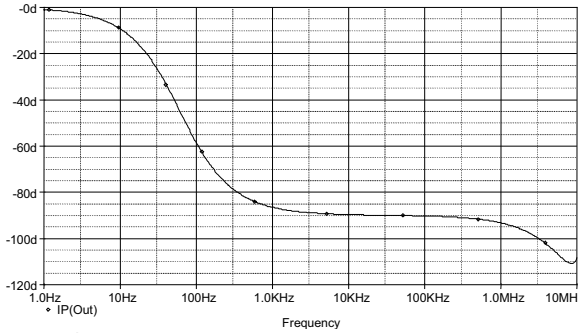

Figure 8: Phase Frequency Plot of the Integrator

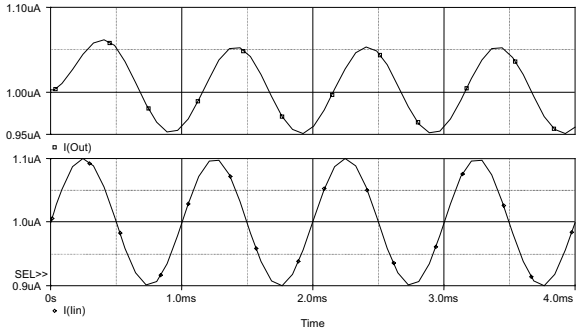

Figure 9: The Transient Response of the Integrator

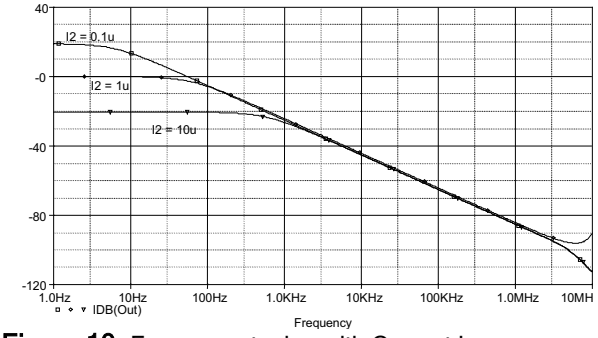

Figure 10: Frequency tuning with Current I_2

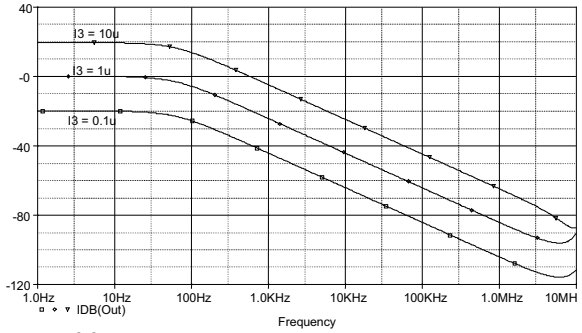

Figure 11: Gain tuning with Current I_3

Simulation of the Biquad (depicted in Fig. 4) formed was also carried out with $I_3/I_2 = I_{13}/I_{12} = 5$, C1 = 100pF and C2 = 100pF. The plots of High pass, Band pass and Low pass signals are shown in Fig. 12. The curves are in accordance with the Transfer functions and parameter expressions given in Table 1. The comparison of theoretical values with the simulated ones is given in Table 2.

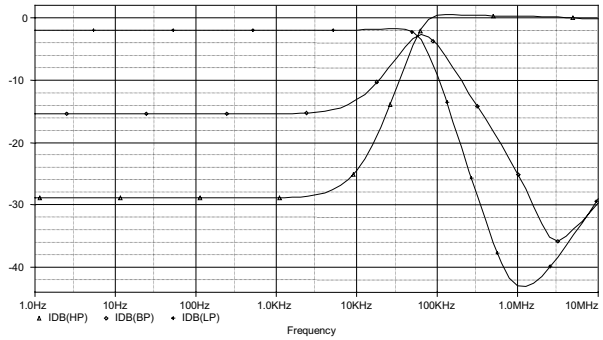

Figure 12: Frequency Response (Magnitude)

Table 2.
Comparisons of results with theoretical values

Parameter	Theoretical	Obtained	% Error
W_0(KHz)	68.164	63	7.576
Q	0.795	0.747	6.038
Bandwidth (KHz)	85.698	84.26	1.678

4. Conclusion

A design technique for implementing STL and DTL circuits using CMOS CC-II based TL loops has been proposed. This technique makes use of the exponentiation property of the diodes and the current conveying and voltage following properties of the CC-II. The operating range of the loop is bound by the bandwidth of the CC architecture as also the CMOS technology used. Using wider bandwidth CCs and shorter channel processes, the performance can be improved significantly. The power required is also very low which makes this technique highly suitable for low power filter design.

5. References

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