A Quantized Analog Delay for an ir-UWB Quadrature Downconversion Autocorrelation Receiver

Sumit Bagga, Lujun Zhang, Wouter A. Serdijn, John R. Long and Erik B. Busking

***Abstract*—A quantized analog delay is designed as a requirement for the autocorrelation function in the Quadrature Downconversion Autocorrelation Receiver (*QDAR*) [1]. The quantized analog delay is comprised of a quantizer, multiple binary delay lines and an adder circuit. Being the foremost element, the quantizer consists of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to binary delay lines, which are a cascade of synchronized D-latches. The outputs available at each line are linked together to reconstruct the incoming signal using an adder circuit. For a delay time of 550 ps, simulation results in IBM's CMOS 0.12 µm technology show that the quantized analog delay requires a total current of 36.7 mA at a 1.6 V power supply. Furthermore, delays in the range of several nanoseconds are feasible at the expense of power. After a Monte Carlo simulation it becomes evident that the response of the quantized analog delay does not suffer drastically from neither process nor component mismatch variations.**

***Index Terms*—analog delay, analog integrated circuits, quadrature downconversion autocorrelation receiver, impulse radio, quantizer, ultra-wideband**

I. INTRODUCTION

Although impulse radio ultra-wideband technology promises enhanced data throughput with low-power consumption, it inseparably introduces several challenging design issues [2] [3] [4]. Ultra-wideband systems transmit at very low spectral densities and occupy a large amount of bandwidth, thus it is unequivocal that interference introduced from neighboring narrowband systems is a serious predicament, which could severely hamper or even degrade the overall performance of the system.

In the transmit reference scheme proposed by Hoctor and Tomlinson [5] (see Fig. 1), consecutive pulses are transmitted with a predefined delay τ_d between them. The first pulse acts as a reference, whereas the second pulse is modulated. The autocorrelation receiver correlates the incoming signal with a delayed version of the previous signal. The absolute value of the output after integration is in fact the energy of the pulse while the polarity of the output contains the data.

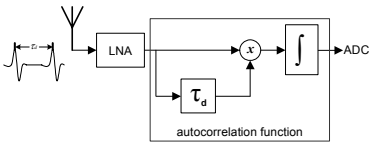

Fig. 1. Transmit reference scheme by Hoctor and Tomlinson

A *Quadrature Downconversion Autocorrelation Receiver (QDAR)* (see Fig. 2) [1] is designed to operate in the presence of strong narrowband interference, while still being able to detect the incoming UWB signal.

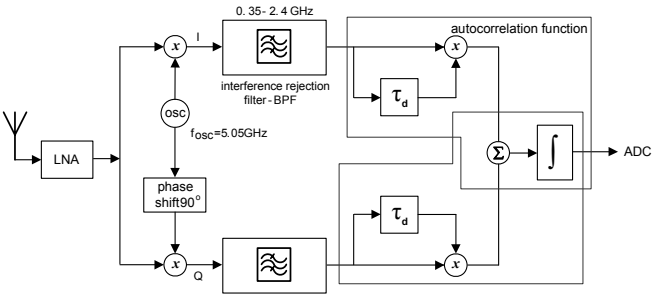

Fig. 2. Quadrature downconversion autocorrelation receiver

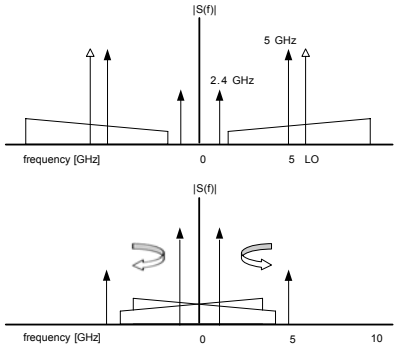

Fig. 3. Frequency spectrum before (top) downconversion and after (bottom) downconversion

The QDAR works on the principle of frequency wrapping or in other words, it folds the ultra-wideband frequency spectrum around the origin. At the same time, the narrowband interferers are positioned outside the band of interest and are simply removed by the means of a band-pass filter (see Fig. 3). Besides resolving the issues

S. Bagga, Lujun Zhang, Wouter A. Serdijn and John R. Long are with the Electronics Research Laboratory, Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Mekelweg 4, 2628CD, Delft, The Netherlands (e-mail: {s.bagga, w.a.serdijn, j.r.long}@ewi.tudelft.nl).

Erik B. Busking is with TNO, Defence, Security and Safety, P.O. Box 96864, 2509JG, The Hague, The Netherlands (e-mail: erik.busking@tno.nl).

0-7803-9398-8/05/$20.00 ©2005 IEEE

of synchronization and capturing multipath energy, the QDAR exploits the fact that detection with an autocorrelation receiver is feasible as long as the relative polarity and shape of consecutive pulses is preserved.

In regards to the transmit reference scheme and from an implementation point of view, one is drawn to the conclusion that the bottleneck to this concept is the physical realization of an accurate continuous-time delay required to execute the autocorrelation function at high frequencies.

As delaying a binary signal requires significantly less hardware complexity as compared to a continuous-time signal, the continuous-time incoming signal should be *"quantized"* before it is delayed. Consequently, this paper proposes a quantized analog delay to be used in the QDAR's (see Fig. 1) autocorrelation function.

The architecture of the quantized delay is discussed in Section 2. A system analysis is performed in Section 3. Section 4 describes the design and implementation of the quantizer, the binary delay line and the adder circuit that implement the delay. Simulation data of the quantized analog delay is given in Section 5. Section 6 presents the conclusions.

II. SYSTEM ARCHITECTURE

Flash or parallel-encoding analog-to-digital converters are often regarded as the fastest way to convert an analog signal into a digital signal [6].

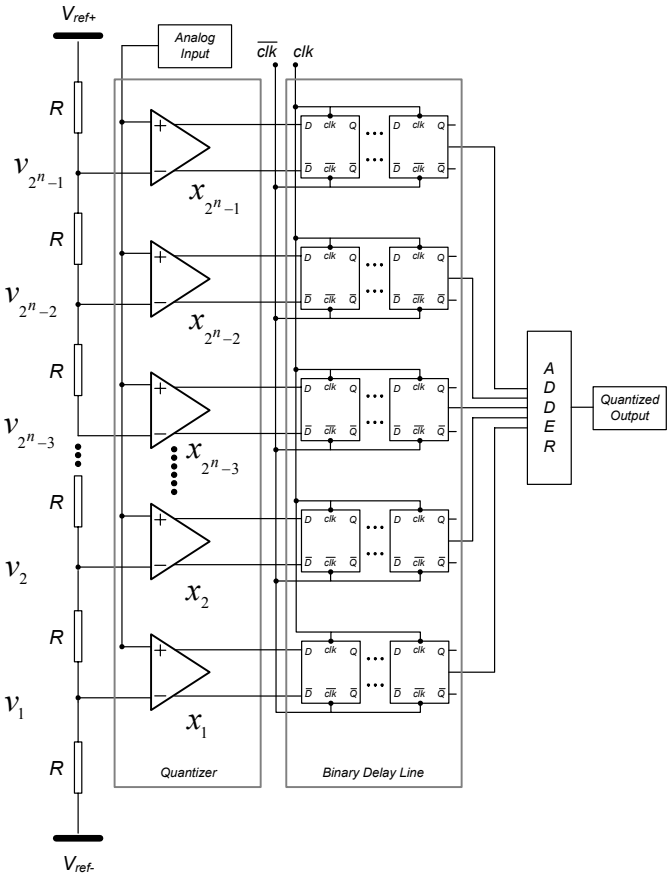

Fig. 4. *Quantized Analog Delay* derived from a conventional Flash ADC

In this paper the concept of a quantized analog delay is derived from the parallel structure of a conventional flash ADC, as so far as the incoming signal is first parallelized before the resulting *states/bits* are delayed using binary delay lines.

As illustrated in Fig. 4, the proposed quantized delay is comprised of a quantizer or *"n"* bits, multiple binary delay lines and an adder circuit. Being the foremost element, the quantizer consists of a series of comparators (2^n-*1*), each one comparing the input signal to a unique reference voltage. The comparator outputs connect to binary delay lines, which constitute a cascade of synchronized D-latches. In autocorrelation receivers the accuracy of the delay element is paramount for proper detection, hence a synchronous delay line is employed. Finally, by using an adder circuit, the outputs available at each delay line are linked together to reconstruct the quantized signal.

III. SYSTEM ANALYSIS

The quality of the approximation of the incoming signal is directly related to the number of bits of the quantizer (*n*) and thus influences the power consumption. For varying quantization levels as well as signal-to-noise ratios (*SNR*), the probability of error is plotted in Fig. 5 for the QDAR. This quantitative analysis undoubtedly shows that by increasing the amount of quantization levels, one is capable of reducing the probability of error during autocorrelation. In addition, the value of *n* is determined based upon the trade-off between power consumption and bit precision, as well as taking into account the probability of error at the desired SNR. Note that *n=0* is the state of no quantization.

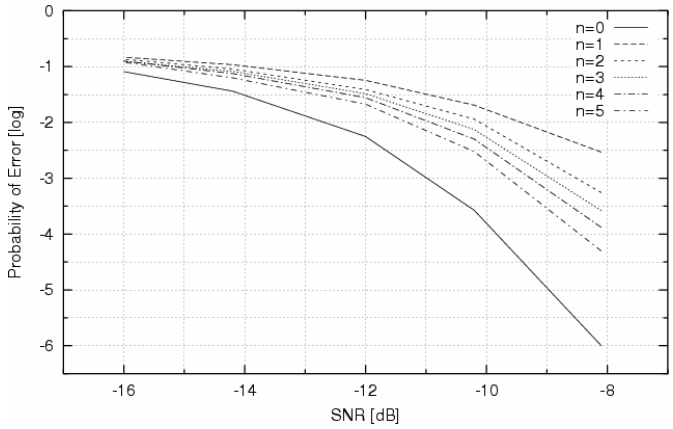

Fig. 5. Probability of error for an *AWGN limited system* for different quantization levels

A. Error analysis

The results illustrated in Fig. 5 assume all devices in the system to behave ideally. However, certain errors may manifest during implementation, as a consequence of process variations or even component mismatch. Hence, it is necessary to analyze the system's true performance under the influence of:

- Variation in delay time
- Variation in comparator's offset voltage
- Variation in gain

Simulations were done using Simulink for 10,000 iterations with a bit precision (*n*) of 3 at an SNR of –10 dB.

1) Variation in delay time

Manufacturing inaccuracies may introduce device mismatches in the binary delay line, which could lead to an inaccurate delay time. To analyze this phenomenon, the delay time, τ_d, is distributed normally with a mean (μ) equal to τ_d and a variance of $k \cdot \tau_d$, assuming that the variation factor (k) is $0<k<1$. In Fig. 6, the probability of error in detection with respect to the delay variation factor k is plotted. It is evident that if the delay time were to deviate by only 1%, the probability of correct detection would be small.

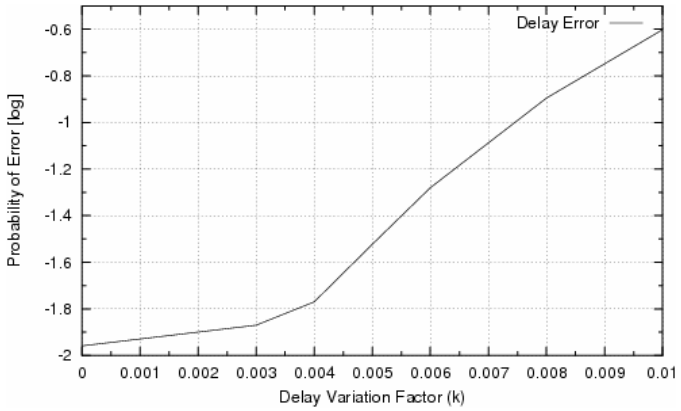

Fig. 6. Error curve for *delay time* variations

2) Variation in offset voltage

The comparator's input offset voltage is assumed to be normally distributed with a mean (μ) equal to 0 and a variance described as, $l \cdot (0.5 \cdot V_{p\text{-}p})/(2^{n-1})$, assuming the variation factor (l) is $0<l<1$ (Note: $V_{p\text{-}p}$ is the input voltage range of the comparator.) In Fig. 7, the probability of error in detection with respect to the offset variation factor l is plotted. If l were to deviate even by 100%, the probability of error remains relatively unchanged.

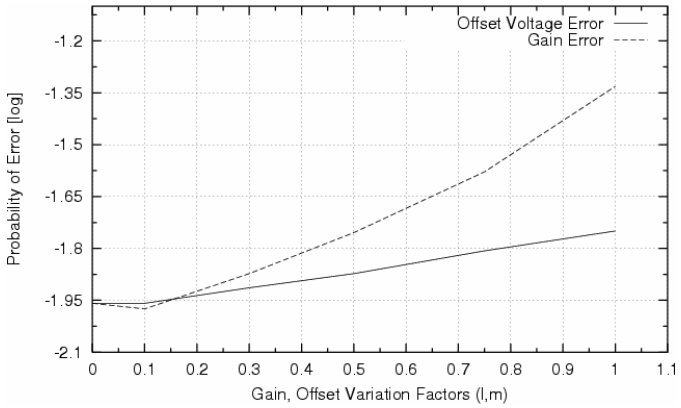

Fig. 7. Error curves for *offset* and *gain variations*

3) Variation in gain

Similar to variations in delay time and offset voltage(s), changes in the gain of the comparator are also considered. In Fig. 7, the probability of error of detection with respect to the gain variation factor m ($0<m<1$) is plotted. If m, were to deviate even by 100%, the probability of error remains relatively unaffected.

From Fig. 6 and Fig. 7, one clearly sees that the variations in the binary delay line play a dominant role in terms of correct detection in the autocorrelation function. As compared to the variation in delay time, the performance degradation due to the variations in the comparator's offset voltage and gain are negligible.

In conclusion, it can now be said that to achieve perfect synchronization in the autocorrelation receiver, designing a binary delay line with little to no variation in delay time is absolutely critical. As a result, a synchronous binary delay line is chosen and is designed in the following section.

IV. SYSTEM DESIGN

In this section the building blocks of the quantized analog delay are designed.

A. Comparator

The key element of the quantizer is the comparator, which compares the input signal to a unique reference voltage and delivers a binary signal as a result of the comparison. Factors such as gain, bandwidth, offset voltage at the input and bit precision are taken into consideration when designing a high-speed low-voltage comparator. In Section III, errors in gain and offset voltage were proven to be negligible when the quantized analog delay is part of the QDAR. Bandwidth and bit precision directly influence power and accuracy, respectively.

The comparator proposed in Fig. 8 is a two-stage design. The first stage or the *preamplifier* is a differential pair made up of transistors M_1 and M_2. The reason to employ a preamplifier is to obtain higher resolution. The second differential stage (M_3 and M_4) primarily acts as *limiting* stage to deliver adequate binary voltage swing to the subsequent stages, i.e. the series of D-latches.

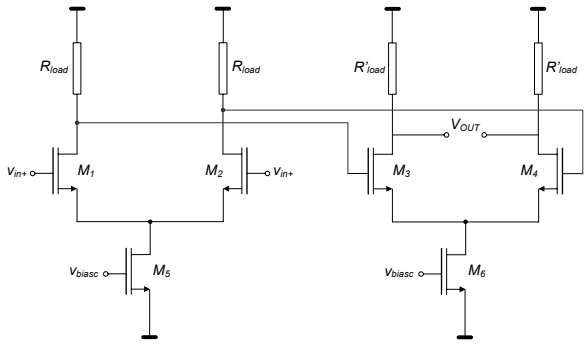

Fig. 8. Two stage comparator

B. Current-mode logic D-Latch

For our application, we adopt the D-latch working on the principle of current-mode logic (*CML*) in [7], which is designed for high-speed low-power applications. Circuits based on CML do not provide a rail-to-rail output swing; however, they are faster than other logic families since they only use NMOS transistors. Other factors such as immunity towards common-mode noise, less dynamic power dissipation and the ability to perform at high speeds make the CML D-latch a viable candidate for the quantized analog delay.

Transistors M_1 and M_2 make up the input tracking stage utilized to sense and track the data variation of the D-latch in Fig. 9. The data is stored with the use of transistors M_3 and M_4. The clock signals V_{clk} and $invV_{clk}$, applied to the gates of transistors M_5 and M_6, respectively, determine whether the latch operates in either the track or the latch mode. The output signal is tracked by the input signal, when the clock signal is "*high*". Likewise, as soon as the clock signal goes "*low*", the transistors of the tracking stage enter the cut-off region and now the logic at the output is stored in the latch pair.

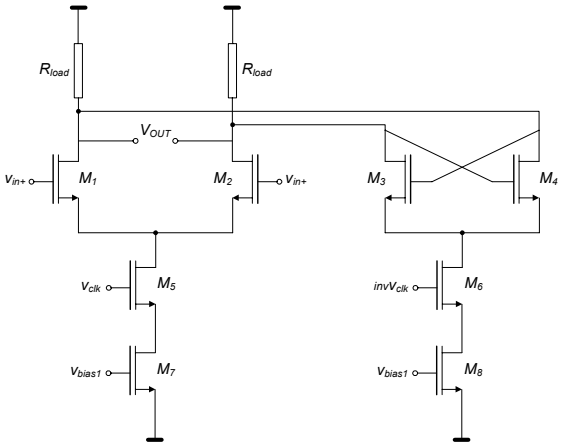

Fig. 9. CML D-latch

C. *Voltage Adder*

In Fig. 10, a voltage adder is used to reconstruct the signal by adding the delayed binary bits at all levels.

Assuming that all transistors operate in the saturation region and that all transistors are identical and have equal aspect ratios, that is,

$$\sum_{i=1}^{n} m_i = \sum_{i'=1}^{n} m_{i'} \tag{1}$$

one obtains a relationship between the sums of the currents in both branches as given by,

$$\sum_{i=1}^{n} I_i = \sum_{i'=1}^{n} I_{i'} \tag{2}$$

(Note, (1) is only true if one uses identical current sources)

After equating the two sides together,

$$\sum_{i=1}^{n} \frac{1}{2} k \frac{W}{L} ((\frac{v_i}{2} - v_x) - v_{th})^2 = \sum_{i'=1}^{n} \frac{1}{2} k \frac{W}{L} ((\frac{v_{i'}}{2} - v_y) - v_{th})^2 \tag{3}$$

one arrives at,

$$v_{out} = v_x - v_y = \sum_{i=1}^{n} \frac{v_i}{n} \tag{4}$$

where n, once again is the bit precision of the quantizer.

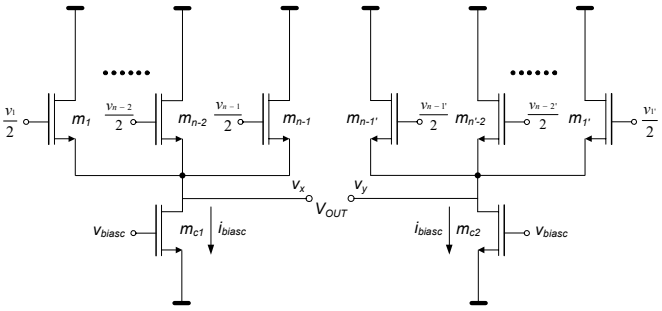

Fig. 10. Voltage adder

V. SIMULATION RESULTS

In UWB systems, it is generally seen that either the 1st or the 2nd derivative of the Gaussian monocycle is used as the transmitted pulse [8]. Taking into consideration [1], the pulse ($g(t)$) fed to the quantized analog delay is chosen to be the real part of a Morlet.

$$g(t) = e^{\frac{-t^2}{2\cdot\sigma^2}} \cdot \cos(\omega \cdot t) \tag{5}$$

where σ determines the pulse width and ω is the center frequency of the spectrum. The Morlet waveform that is used has a center frequency at 4.6 GHz and an effective pulse width of 1 ns. Its frequency spectrum is seen in Fig. 11.

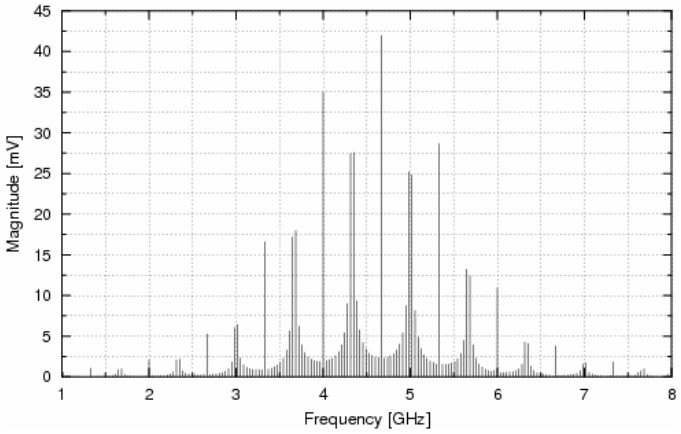

Fig. 11. Frequency spectrum of Morlet waveform

Fig. 12 illustrates the performance of the quantized analog delay synchronized to a clock frequency (f_{clk}). The time delay (τ_d) between the analog and the quantized signal is calculated using the following equation,

$$\tau_d = \frac{f_{clk}}{2} \cdot (n_o) \tag{6}$$

where n_o denotes the number of D-latches per level. Just to re-iterate, the delay time is paramount for autocorrelation and not the exact preservation of the waveform. A detailed list of specifications is given in Table 1. The time delay of 549 ps seen here differs from the actual value by only 0.02 %, which is acceptable based on the plots in Fig. 6. A realistic 10 GHz clock signal was used. In addition, Fig. 13 illustrates the simulated and extracted waveforms.

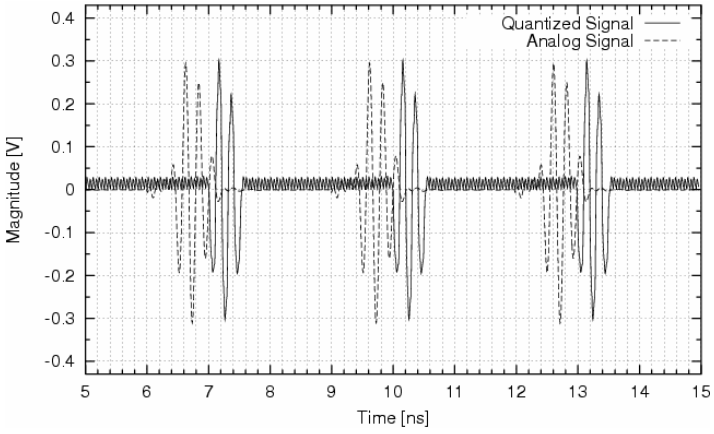

Fig. 12. Quantized signal vs. analog signal

TABLE I
SIMULATION PARAMETERS OF THE QUANTIZED TIME DELAY

Specifications	Simulated (w.r.t *Morlet Waveform*)	
Quantizer Precision (n)	3	
Time delay (τ_d)	Actual	Simulated
n_o=10	550 ps	549 ps
Current consumption	36.7 mA @ 1.6 V	
Max. operating freq.	4.6 GHz	
Clock frequency (f_{clk})	10 GHz	
Process	IBM CMOS 0.12 µm	
Size	1.25 mm^2	

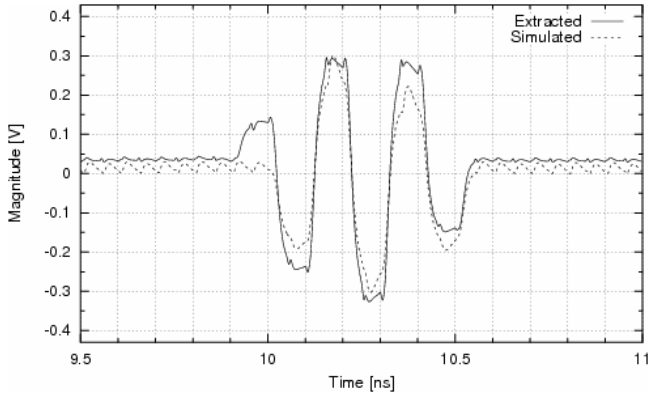

Fig. 13. Quantized signal – simulated vs. extracted

Finally, the circuit's sensitivity to process and component mismatch variations is analyzed by randomly varying (i.e. 5 iterations) the component tolerances as well as the model parameters between their specified tolerance limits. This is done with a Monte Carlo simulation. From Fig. 14 it is inferred that the desired delay time is relatively unlikely to show a substantial discrepancy as a result of process and mismatch variations. The iterations seen here show a gain error of the quantized signal, which in the Section 3 has been analyzed and is less influential to the outcome of the autocorrelation function.

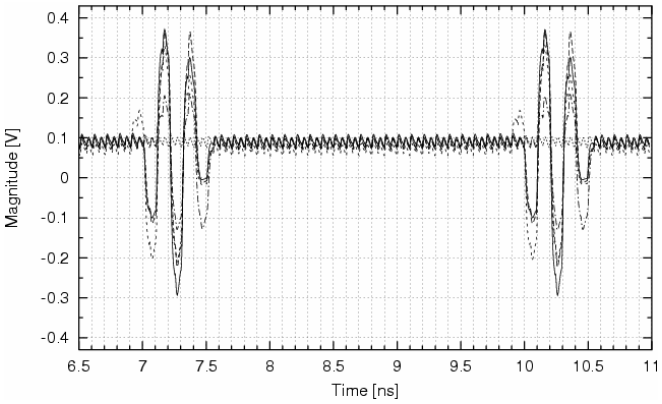

Fig. 14. Monte Carlo – Statistical Analysis

To further elaborate on the aforementioned, and to quantitatively comprehend the effect of gain error on the overall performance of the autocorrelation function, the autocorrelation coefficient is calculated, defined as,

$$\rho = \frac{\int_{t1}^{t2} \left| E_m \cdot E_{qm} \right| \, dt}{\sqrt{\int_{t1}^{t2} \left| E_m \right|^2 dt \cdot \int_{t1}^{t2} \left| E_{qm} \right|^2 dt}} \tag{7}$$

where E_m and E_{qm} are the respective energy contents of the incoming Morlet waveform and the quantized Morlet waveform at the output, ρ is the autocorrelation coefficient and t_1, t_2 represent the integration time [9].

The parameter ρ is a measure of the error in the autocorrelation due to gain or offset variations. Subsequent to simulation results, if the gain (m) were to vary between 0.1-1, ρ would change by only 0.05 %, which is in fact negligible.

VI. CONCLUSIONS

A quantized analog delay is designed as a requirement to execute an autocorrelation function in the Quadrature Downconversion Autocorrelation Receiver (QDAR) [1]. A comprehensive quantitative analysis has shown the outcome of the autocorrelation function is more susceptible to time delay errors as compared to gain or offset voltage variations. For a delay time of 550 ps, simulation results in IBM's CMOS 0.12 µm technology show that the quantized analog delay requires a total current of 36.7 mA at a 1.6 V power supply. Furthermore, delays in the range of several nanoseconds are feasible. A Monte Carlo simulation has also been performed to validate the performance of the quantized analog delay and results show that the response of the delay does not suffer drastically from neither process nor component mismatch variations.

VII. REFERENCES

[1] Simon Lee, S. Bagga and W.A. Serdijn, "A Quadrature Downconversion Autocorrelation Receiver Architecture for UWB," Joint *UWBST and IWUWBS*, pp. 6-10, May 2004

[2] D. Porcino and W Hirt, "Ultra-wideband radio technology: potential and challenges ahead," *IEEE Communications Magazine*, vol. 41, no. 7, pp. 66-74, July 2003

[3] L. Yang and G. B. Giannakis, "Ultra-wideband communications: an idea whoes time has come," *IEEE Singal Processing Magazine*, vol. 21, no. 76, pp. 26-54, November 2004

[4] M. Z. Win and R. A. Scholtz, "Imulpse radio: how it works," *IEEE Communications Letters*, vol. 2, no. 2, pp. 36-38, Feburary 1998

[5] R.T. Hoctor and H.W. Tomlinson, "Delay-Hopped Transmitted-Reference RF Communications," *Proceedings of the IEEE Conference on Ultra Wideband Systems and Technologies*, pp. 265-270, May 2002

[6] R. Blazquez, F. S. Lee, D. D. Wentzloff, P. P. Newaskar, J. D. Powell, A. P. Chandrakasan, "Digital architecture for an ultra-wideband radio receiver ", *Vehicular Technology Conference, 2003. VTC 2003-Fall. 2003 IEEE 58th ,* Volume: 2, 6-9, pp. 1303-1307, October 2003

[7] P. Herdari and R Mohavavelu, "Design of ultra high speed CML buffers and latches", *Proceedings International Symposium on Circuits and Systems,* pp. 208-211, May 2003

[8] S. Bagga, W.A. Serdijn and J. R. Long, "A PPM Gaussian monocycle transmitter for ultra-wideband communications," *Joint UWBST and IWUWBS*, pp. 130-134, May 2004

[9] Erwin Kreyswig, "Advanced Engineering Mathematics," *John Wiley and Sons, Inc., 1999*