Design of Static and Dynamic Translinear Circuits based on CMOS CCII Translinear Loops

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ABSTRACT

A novel technique to implement static and dynamic translinear circuits based on CMOS CCII translinear (TL) loops is proposed. Various examples of static translinear circuits, such as squaring, square-root, geometric-mean circuits, are introduced. Falling into the category of dynamic translinear circuits, a second-order low-pass filter and a fourth-order filter offering high-pass, low-pass and band-pass transfer functions are presented.

This approach opens a new paradigm for design of translinear circuits using CMOS CCIIs and diodes implemented using CMOS technology. The filters realized are electronically tunable by altering the magnitude of the bias/control currents.

1. INTRODUCTION

The ongoing trend towards lower supply voltages and low-power operation has brought the area of analog integrated filters into prominence. In conventional filter implementation techniques using opamp–MOSFET–C, transconductance–C or switched capacitors, the supply voltage restricts the attainable maximum dynamic range. Further, the use of linear resistors in a low-power environment demands a large silicon area for on-chip integration and hence this approach is impractical. High-frequency operation and the requirement for tunability of the filter complicate the situation further.

TL filters are based on the dynamic translinear (DTL) circuit principle [1], which is a generalization of the static TL (STL) principle formulated by Gilbert in 1975 [2]. Both static and dynamic TL circuits exploit the inherent exponential transfer function obtained from the relation between the collector current and base-emitter voltage of bipolar junction transistors (BJT's) [3] or between the drain current and gate-source voltage of a MOS transistor operating in its weak-inversion region [4]. In a MOS/CMOS based implementation of a TL circuit the current range where the exponential V-I characteristic can be used, is typically limited to three decades compared to more than six decades for a BJT, thus restricting the choice and optimization of the operating point within the weak-inversion region.

Another fundamental limitation of MOS transistors operating in weak inversion is the poor matching of the threshold voltages which affect the distortion (and thus dynamic-range) performance of CMOS log-domain filters. Moreover, TL circuits implemented in CMOS technology operating in sub-threshold region suffer from low bandwidth limitations.

CCII-based translinear loops [5] open a new paradigm towards the design of static and dynamic TL circuits in CMOS technology. In this paper we discuss the realization of various STL circuits generating non-linear static transfer functions such as square, square root, cube, cube root, geometric mean, etc. We also present the implementation of a second-order low-pass filter and a fourth-order filter. These demonstrate the possible use of CCII-based TL loops for implementing DTL circuits for generating linear dynamic transfer functions.

2. TL PRINCIPLE AND EXTENDED TL LOOP

The CCII-based translinear loop proposed in [5] is shown in Fig. 1. Applying the TL principle to the loop formed by diodes D1-D4 (and the four CCIIs), we get the following expression.

$$I_{D1} * I_{D3} = I_{D2} * I_{D4} \quad (1)$$

where I_{DX} is the current through diode D_x.

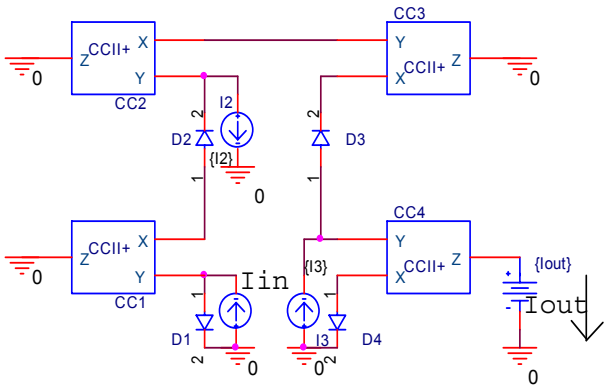

Fig. 1: TL loop employing CCII's and diodes

The proposed TL loop can be extended to third order by including two additional diodes and two additional CCIIs. This extended TL loop is shown in Fig. 2. Using the V-I relationship of the diodes and the voltage tracking properties of the CCII, the loop formed by the diodes D1-D6 results in the following relation:

$$I_{D1} * I_{D3} * I_{D5} = I_{D2} * I_{D4} * I_{D6} \quad (2)$$

Generalization of the extended TL loop can be used to realize different mathematical functions e.g. $f(x^N)$ and $f(x^{1/N})$.

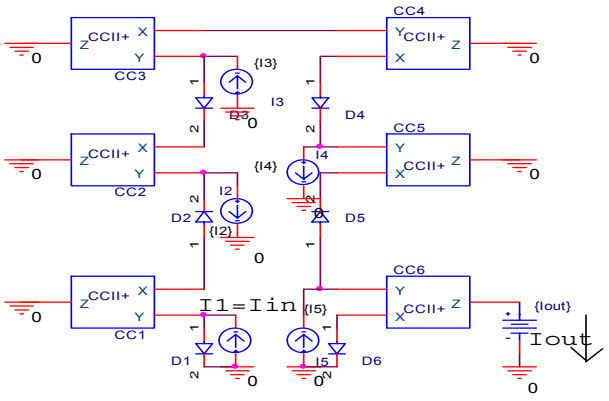

Fig. 2: Extended TL loop using 6 CCII's

DTL circuits can implement differential functions. Using the DTL principle, a 2nd-order low-pass filter can be realized as shown in Fig. 3.

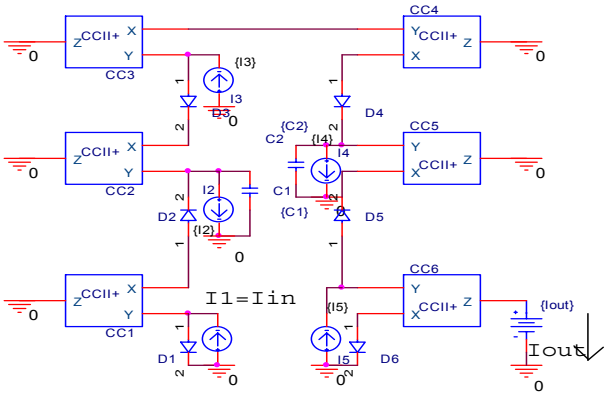

Fig. 3: The 2nd order LPF using extended TL loop

Applying the DTL principle to analyze the circuit shown in Fig. 3 and using Equation 2, we can derive the transfer function of the LPF as follows:

$I_{in} * I_{D3} * I_{D5} = I_{D2} * I_{D4} * I_{out}$ (3)

$\Rightarrow I_{in} * I_3 * I_5 = I_{out} * (I_2 + I_{C1}) * (I_4 + I_{C2})$

The current in the capacitor depends on the time-derivative of the voltage across it, so

$\Rightarrow I_{in} * I_3 * I_5 = (I_{out} * I_2 + C_1 * dV_{cap}/dt * I_{out}) * (I_4 + I_{C2})$

$\Rightarrow I_{in} * I_3 * I_5 = (I_{out} * I_2 + C_1 * V_t * dI_{out}/dt) * (I_4 + I_{C2})$

$\Rightarrow I_{in} * I_3 * I_5 = I_{out} * (I_2 + sC_1V_t) * (I_4 + I_{C2})$

Similarly, $I_{in} * I_3 * I_5 = I_{out} * (I_2 + sC_1V_t) * (I_4 + sC_2V_t)$

$\Rightarrow I_{out} / I_{in} = I_3 * I_5 / ((I_2 + sC_1V_t) * (I_4 + sC_2V_t))$ (4)

According to Equation 4, the circuit of Fig. 3 behaves as an inherently linear 2nd-order low-pass filter with corner frequencies (f_c), given by:

$f_{c1} = I_2/C_1V_t$ and $f_{c2} = I_4/C_2V_t$ (5)

Here, V_t is the thermal voltage and I_2 and I_4 represent two currents that control the cutoff frequencies of the filter.

The circuit shown in Fig. 3 can be optimized as shown in Fig. 4 to save silicon area and reduce power dissipation. The optimized version has exactly the same transfer characteristics as the CCII-based TL loop and can be derived as follows: i) any CCII that has its Z-terminal grounded is replaced by a voltage follower, and ii) any cascade of two (or more) voltage followers is replaced by a single voltage follower.

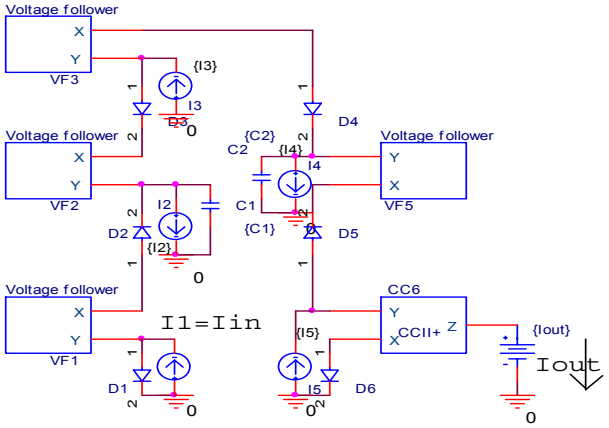

Fig. 4: Optimized 2nd order LPF

A fourth-order filter was also realized using two 2nd-order LPF's in cascade and applying feedback to demonstrate the application of the CCII-based TL loop in filter design. The resulting 4th-order is depicted in Fig. 5. Table 1 gives the three transfer functions.

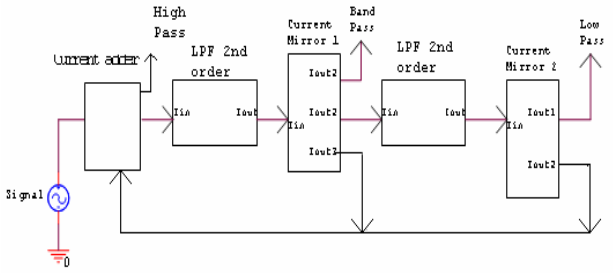

Fig. 5: LPF-LPF topology to implement a 4th-order filter

Table 1: Transfer functions of the 4th-order filter

High Pass -	$\frac{(s+a)(s+b)(s+c)(s+d)}{D_r}$
Band Pass -	$\frac{K_1 * K_2 * (s+c)(s+d)}{D_r}$
Low Pass -	$\frac{K_1 * K_2 * K_3 * K_4}{D_r}$
Center Freq (ω_o) -	$\sqrt[4]{(a \cdot b \cdot c \cdot d + K_1 \cdot K_2 \cdot c \cdot d + K_1 \cdot K_2 \cdot K_3 \cdot K_4}$

Here,

$D_r = (s+a)(s+b)(s+c)(s+d) + (K_1K_2K_3K_4) + (K_1K_2(s+c)(s+d))$

$K_1 = I_{13}/C_11V_t$ $K_2 = I_{15}/C_{12}V_t$

$K_3 = I_{23}/C_{21}V_t$ $K_4 = I_{25}/C_{22}V_t$

$a = I_{12}/C_{11}V_t$ $b = I_{14}/C_{12}V_t$

$c = I_{22}/C_{21}V_t$ $d = I_{24}/C_{22}V_t$

I_{12}, I_{13}, I_{14}, I_{15} are the currents flowing through diodes D_2, D_3, D_4 and D_5 in the LPF-1and I_{22}, I_{23}, I_{24}, I_{25} are similar currents in LPF-2. C_{11}, C_{12} are capacitances in LPF-1 and C_{21}, C_{22} are capacitances in LPF-2.

3. SIMULATION RESULTS

The proposed circuits shown in Fig. 2, 3, 4 and 5 have been simulated using PSpice. In these simulations, the class AB current conveyor proposed in [6] has been used with I_{bias} = 3uA, V_{dd} = 1.25V, V_{ss} = -1.25V. The voltage

followers used in Fig. 4 were also realized using the same design [6] but by removing the transistors responsible for the CCII current-follower action. Device model parameters used in the simulations were taken from MIETEC's 0.5um CMOS process.

The multiplication/division action of the circuit shown in Fig. 2 has been simulated and is plotted in Fig. 6 for different multiplication factors (M.F. = I_3*I_5/I_2*I_4). The output was in agreement with that expected from equation 2.

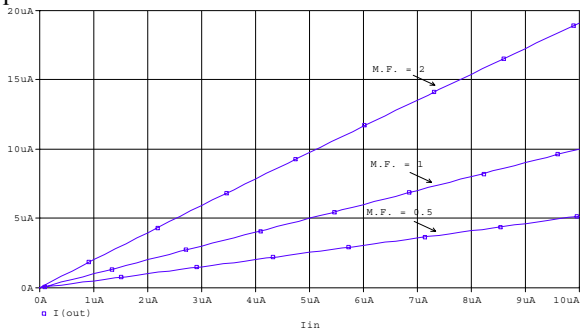

Fig. 6: Static multiplication/division behavior

Squaring characteristics were also realized by giving the same input to I_1 and I_3 and keeping I_2=I_4=I_5=1u. The obtained simulation result is shown in Fig 7.

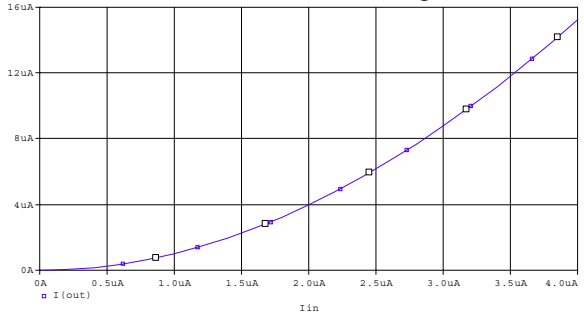

Fig. 7: Squaring behavior

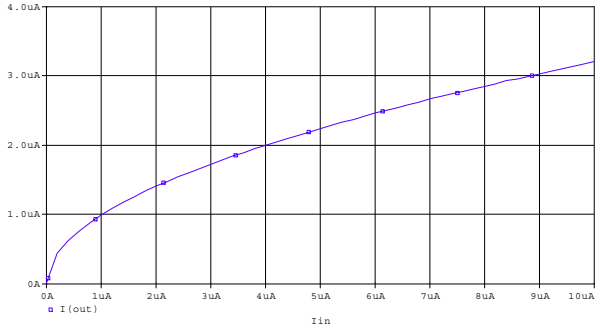

Fig. 8: Square-root behavior

Square-root, cube-root and cube characteristics were also obtained by varying the values of the relevant current sources depending on the function being realized. Simulations of these are shown in figures 8, 9 and 10. Geometric mean of I_1 and I_3 (set to either 1u or 4u) is depicted in Fig. 11.

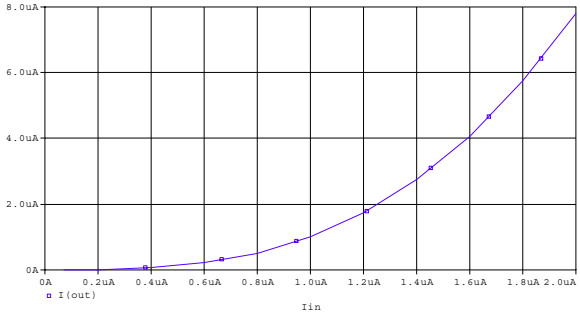

Fig. 9: Cubing behavior

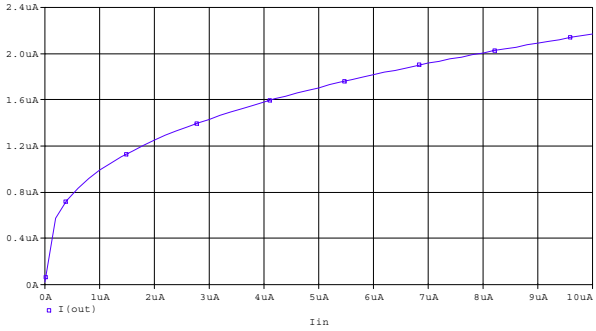

Fig. 10: Cube-rooting behavior

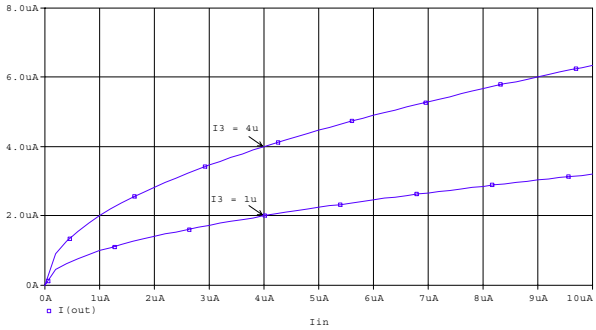

Fig. 11: Geometric mean of I_1 and I_3

An AC analysis of the LPF (Fig. 3) was carried out with I_{in} =1uA_{dc} + I_{ac} keeping the value of other current sources at 1 uA and the capacitances at 30pF. The magnitude and phase response of the LPF are shown in Fig 12 and 13 respectively. The maximum operating frequency was found to be 30 MHz. The power consumed by the LPF was found to be 250uW at the aforesaid bias conditions.

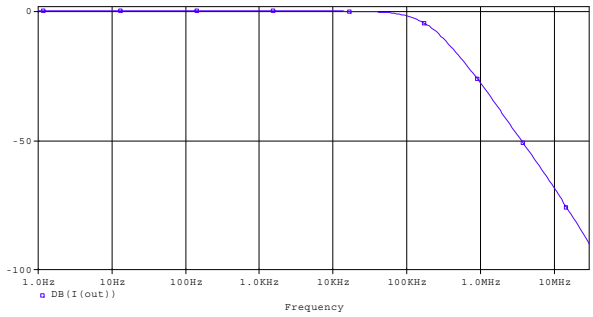

Fig 12: Magnitude response of the LPF

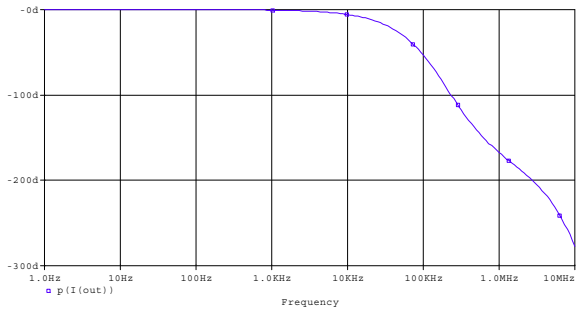

Fig 13: Phase response of the LPF

The AC characteristics of the optimized LPF (Fig. 4) were found to be similar to Fig. 12 and 13. However the power consumed was 115.5uW (54.8% less).

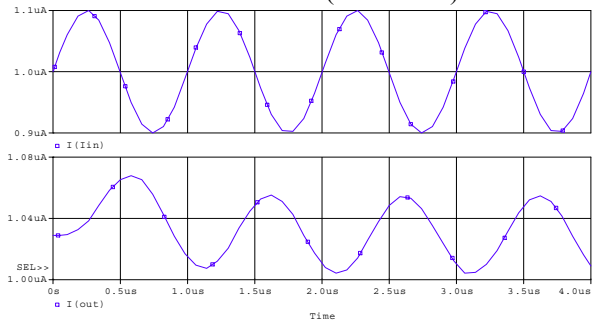

Fig 14: Transient response of the LPF

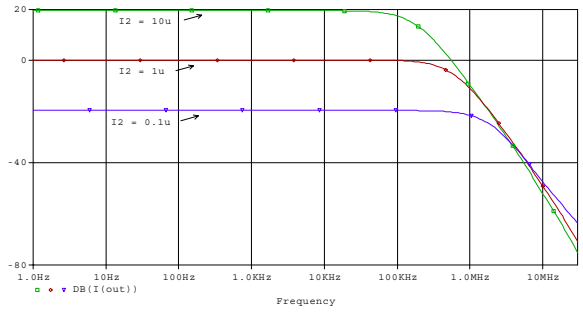

Fig 15: LPF frequency tuning by changing I_2

A transient analysis of the LPF (Fig. 3) was carried out at 1MHz frequency with I_{in}=1uA_{dc} + 0.1uA (signal peak value), I_2=I_4=I_5=1uA; C1 = C2 = 10pF and is shown in Fig. 14. Total harmonic distortion was found to be under 0.5% up to 1MHz.

The corner frequency of the LPF (Fig. 3) can be tuned by altering the value of current sources (I_2/I_4), while the gain can be varied with any of the current sources (I_2, I_3, I_4, I_5). These are shown in Fig. 15 and 16, respectively.

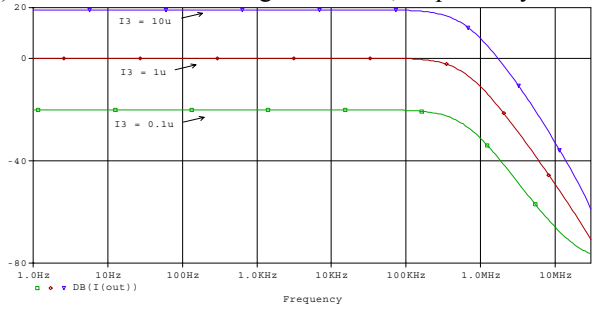

Fig 16: LPF gain tuning by varying I_3

Simulation of the 4th order LPF (Fig. 5) was carried out with I_{13}/I_{12} = I_{23}/I_{22} = 3.1; C_{11}=C_{12}=C_{21}=C_{22}= 10pF while keeping the input bias the same as for LPF (Fig 3). The high-pass, band-pass and low-pass characteristics are shown in Fig. 17. The quality factor was found to be 1.43 and the power dissipation amounts to 500uW.

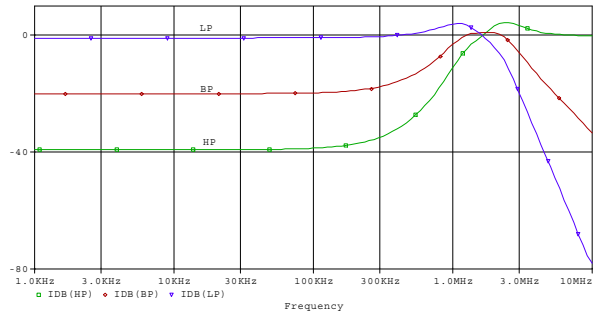

Fig 17: Frequency response of the biquad

4. CONCLUSIONS AND DISCUSSION

A design technique for implementing static translinear (STL) and dynamic translinear (DTL) circuits using CMOS CCII-based extended TL loops has been proposed. This technique makes use of the exponential property of the diodes and the current-conveying and voltage-following property of the CCII's. Generation of various mathematical functions has been demonstrated using the STL behavior of the extended TL loop. Second-order and fourth-order filters employing the DTL circuit principle were demonstrated. The operating range of the TL loop is bound by the bandwidth of the CCII's employed and the CMOS technology used. Using CCII's exhibiting larger bandwidths and shorter channel processes the performance can be improved significantly. The power required is also very low, which makes this technique highly suitable for low-power designs.

5. REFERENCES

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