A 39 dB DR CMOS Log-Amp RF Power Detector with ±1.1 dB Temperature Drift from -40 to 85°C

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***Abstract*—This paper presents a temperature compensated logarithmic amplifier (log-amp) RF power detector implemented in CMOS 0.18 μm technology. The input power can range from -50 to +10 dBm for RF signals ranging from 100 MHz to 1.5 GHz. This design attains a typical DR of 39 dB for a ±1 dB log-conformance error (LCE). Up to 900 MHz the temperature drift is never larger than ±1.1 dB for all 24 measured samples over a temperature range from -40 to +85°C. The current consumption is 6.3 mA from a 1.8 V power supply and the chip area is 0.76 mm².**

I. Introduction

To accurately set the output power of a PA in handsets, a power control loop is often used. A coupler senses a fraction of the output RF signal and feeds it to an RF power detector (Fig. 1). It's output is a measure of the average peak value of the input RF signal. Knowledge about the modulation type employed allows for the accurate calculation of the transmitted power. Log-amp detectors in Bipolar technology present good temperature stability for RF applications [1], [2]. CMOS log-amps for RF power-detection so far published fail to demonstrate consistent performance over a wide temperature range [3], [4]. This prototype IC demonstrates that a temperature compensated log-amp RF power detector can be designed using standard CMOS technology while attaining a temperature drift bounded to ±1.1 dB and low power consumption.

II. System architecture

The architecture of a log-amp detector is based on a cascade of N gain cells (A), N+1 detector cells (D), an output low-pass filter (LPF1) to reject high-frequency components at the output and finally an offset cancellation loop around the cascade of gain cells and another low-pass filter (LPF2). In this design $N = 4$, as shown in Fig. 2. The transfer characteristic of A and D are respectively:

$$V_{\text{out-A}}\,[\text{V}] = \begin{cases} A \cdot V_{\text{in-A}}, & \text{if } |V_{\text{in-A}}| < E_{\text{kA}}, \\ A \cdot E_{\text{kA}}, & \text{if } |V_{\text{in-A}}| \geq E_{\text{kA}}, \end{cases} \quad (1)$$

$$I_{\text{out-D}}\,[\text{A}] = \begin{cases} \frac{\beta}{4} \cdot V_{\text{in-D}}^2, & \text{if } |V_{\text{in-D}}| < E_{\text{kD}}, \\ I_{\text{biasD}}, & \text{if } |V_{\text{in-D}}| \geq E_{\text{kD}}, \end{cases} \quad (2)$$

in which A is the voltage gain of the gain cell, E_{k} is the input referred clipping voltage (knee voltage) and in CMOS technology $\beta = \mu C_{\text{ox}} W/L$. In this design $AE_{\text{kA}} > E_{\text{kD}}$ is chosen. For an input signal with amplitude E_{kD}/A^4, only the last detector cell reaches its maximum output current, I_{biasD}.

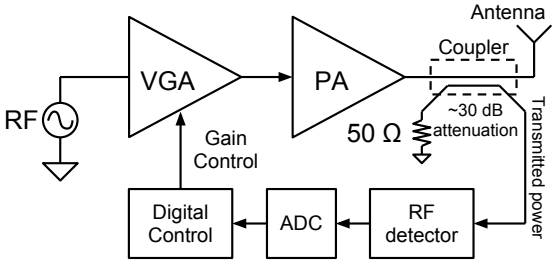


Fig. 1: Transmitted-power control loop

Increasing the input signal to E_{kD}/A^3 will clip the output of the last two detector cells to I_{biasD}. Consequently, for every multiplication of the input signal magnitude by A, a linear increase of the output current equal to I_{biasD} is expected. A piece-wise linear approximation of a logarithmic function is obtained. This logarithmic transfer can be represented by a linear relation between V_{out} and the input power P_{in} expressed in dBm:

$$V_{\text{out}}\,[\text{V}] = K_{\text{slope}}(P_{\text{in}} - P_0)\,, \quad (3)$$

where K_{slope} and P_0 are given by:

$$K_{\text{slope}}\,[\text{V/dB}] = \frac{I_{\text{biasD}} R_{\text{out}}}{20\log(A)}\,, \quad (4)$$

$$P_0\,[\text{dBm}] = 20\log\left(\frac{E_{\text{kD}}}{\sqrt{50\,\Omega}\cdot A^{N+1}}\right) + 30\,. \quad (5)$$

A. Temperature compensation

To implement a log-amp detector for which the transfer characteristic is temperature independent, both the slope (K_{slope}) and the intercept power (P_0) should be kept constant over temperature. This is achieved by temperature stabilization of both the gain cells and the detector cells and by temperature scaling of the input/output signals of the log-amp detector core (Fig. 2). Fig. 3 shows the architecture of the complete temperature compensated log-amp detector.

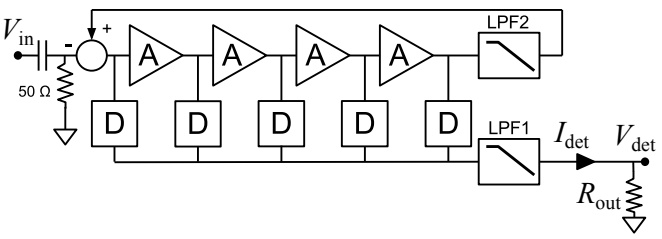


Fig. 2: Log-Amp Detector Core

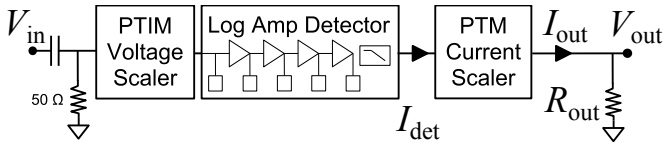


Fig. 3: Log-Amp Detector with temperature compensation

1) Gain Cell: The gain (A) variation over temperature affects the transfer's slope (4) and intercept (5). To keep both parameters constant over temperature, the gain cell (Fig. 4) should be designed to attain a voltage gain $g_m \cdot R$ that is constant over temperature:

$$A(T) = g_m(T) \cdot R(T) \quad (6)$$

$$= \sqrt{\mu(T) C_{\text{ox}} \frac{W}{L} I_{\text{biasA}}(T)} \cdot R(T)\,, \quad (7)$$

where $\mu(T) = \mu_0 (T/T_{\text{ref}})^{N_\mu}$ models the temperature dependence of the mobility with $1.5 < N_\mu < 2$ [5] and $R(T)$ represents the temperature behavior of all resistors in this design (except the resistors in the front-end scaler). If current $I_{\text{biasA}}(T)$ is designed to have a temperature dependence proportional to the inverse mobility (PTIM) and $R(T)^{-2}$, the gain A becomes to a first order constant over temperature.

2) Input PTIM Voltage Scaler: After temperature compensation, the maximum output swing of every gain cell presents a PTIM temperature dependence. Consequently the gain and detector cells, except the front-end cells, experience a maximum input voltage with PTIM temperature behavior. Therefore a PTIM voltage scaler in front of the log-amp detector core is required.

3) Detector Cell: Detector bias current I_{biasD} and knee voltage E_{kD} appear in the expressions for slope (4) and intercept (5) respectively. Rewriting (2) yields $E_{\text{kD}} = \sqrt{4 I_{\text{biasD}}/\beta}$. Because the maximum output voltage of the gain cells exhibit a PTIM behavior, E_{kD} should follow the same temperature behavior. This can be achieved using a PTIM bias current $I_{\text{biasD}} = K_0 L/(C_{\text{ox}} W R^2(T) \mu(T))$. The knee voltage becomes:

$$E_{\text{kD}}(T) = \sqrt{\frac{4 I_{\text{biasD}}(T)}{C_{\text{ox}} \frac{W}{L} \mu(T)}} = \frac{2\sqrt{K_0}}{\beta(T) R(T)}\,. \quad (8)$$

The temperature dependence of E_{kD} on both $\beta(T)$ and $R(T)$ needs to be compensated for in (5). This can be achieved through the front-end PTIM voltage scaler. The transfer of the input voltage scaler is given by:

$$S(T) = \frac{S_0}{\beta(T) R(T)}\,. \quad (9)$$

Substitution of (9) into (5) results in:

$$P_0(T) = 20 \log \left(\frac{E_{\text{kD}}(T)}{\sqrt{50\,\Omega} \cdot S(T) \cdot A^5} \right) + 30 \quad (10)$$

$$= 20 \log \left(\frac{2\sqrt{K_0}}{\sqrt{50\,\Omega} \cdot S_0 \cdot A^5} \right) + 30\,, \quad (11)$$

which yields a temperature independent intercept power P_0.

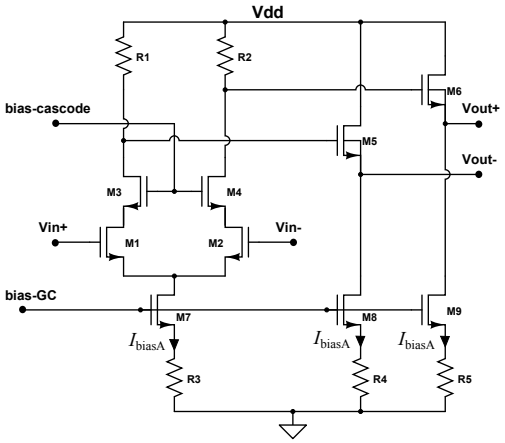


Fig. 4: Circuit of Gain-cell (A)

4) PTM Current scaler: The output current I_{det} of the log-amp detector core presents the same PTIM dependence as I_{biasD}. In order to obtain a log-amp detector with a constant transfer over temperature, a proportional to mobility (PTM) current scaler is required between the log-amp detector core and the final I-V conversion (Fig. 3):

$$I_{\text{out-CONST}} = I_{\text{det-PTIM}} \cdot (I_{\text{CONST}}/I_{\text{PTIM}})\,. \quad (12)$$

III. Circuit Design

A. Input PTIM Voltage Scaler

A resistor π-network, with a $50\,\Omega$ input impedance and 5.7 dB attenuation, implements the passive front-end voltage scaler by employing positive- and negative-temperature coefficient resistors. The first-order temperature behavior of the desired relation (9) can be approximated by controlling the resistor values R_{PTC} and R_{NTC}:

$$S(T) = \frac{R_{\text{PTC}} R_{\text{NTC}}}{(R_{\text{PTC}} + R_{\text{NTC}})^2} \cdot (\text{TC}_\text{P} - \text{TC}_\text{N})\,. \quad (13)$$

B. Gain Cell

The circuit of the gain cell, shown in Fig. 4, is a differential pair with cascodes, the latter to improve the bandwidth by decreasing the Miller multiplication of C_{GD} of M1/M2 seen at the input of the gain cell. The voltage followers provide a lower common-mode output voltage needed to bias the next gain cell. To limit the V_{GS} voltage drop, the voltage followers were implemented with isolated NMOS devices ($V_{\text{BS}} = 0$).

C. Detector Cell

The circuit of the detector cell is depicted in Fig. 5. It is an NMOS version of the detector circuit from [6]. Differently from it's bipolar counterpart, where $E_{\text{kD}} = 4V_{\text{T}}$, E_{kD} is a function of transistor size and bias current in a MOS implementation. For a sinusoidal input signal $V_{\text{in}} = V_P \sin(\omega_p t)$, were $V_P \leq E_{\text{kD}}$, the detector output current can be expressed by:

$$I_{\text{out}} = \frac{\beta}{4} V_P \sin^2(x) = \frac{\beta V_P}{8} \Big(1 - \cos(2\omega_p t)\Big)\,[\text{A}]\,, \quad (14)$$

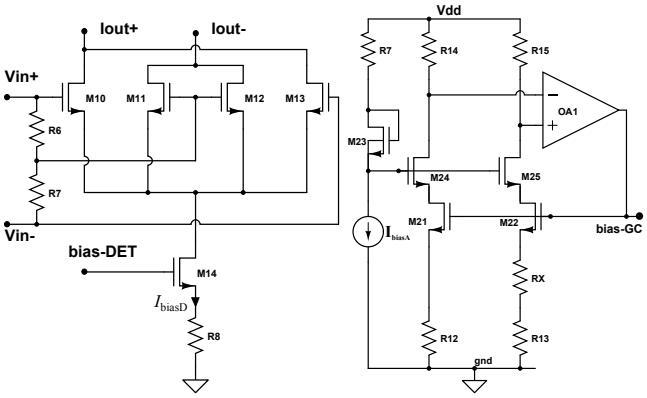


Fig. 5: Circuit of detector-cell (D)

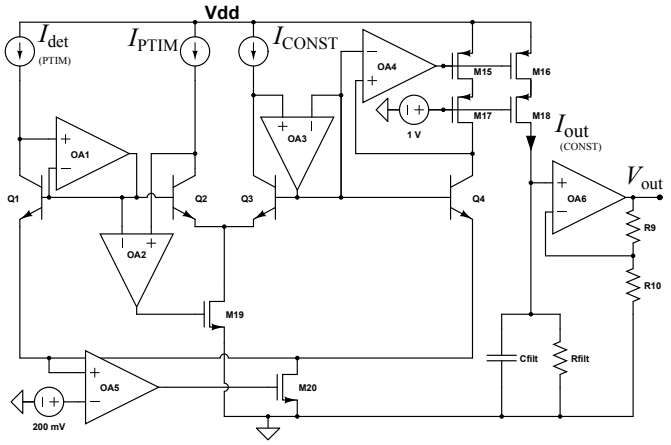


Fig. 8: Circuit of PTM current scaler and I-V converter.

Fig. 6: Circuit of PTIM current generator.

which contains a DC and a double frequency component ($2\omega_p$). After low-pass filtering only the DC component remains. The current output of the detector ($\beta V_P/8$) is thus a measure of the peak amplitude of the input signal.

D. PTIM Bias Generator

From (5) it follows that the intercept is inversely proportional to A^5. Small variations of the gain will yield relatively large intercept shifts over temperature, which requires an accurate constant-g_m bias circuit.

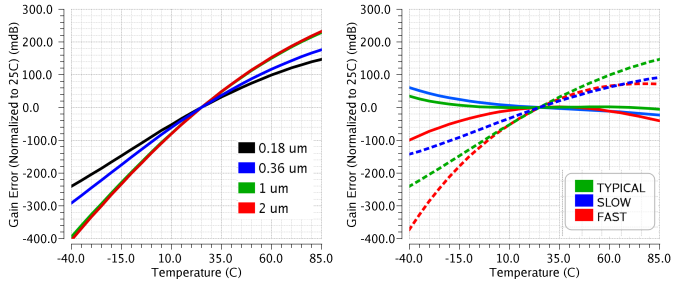
The chosen architecture for constant-g_m biasing is shown in Fig. 6. The current through transistors M21 and M22 is given by [7]:

$$I_{\text{PTIM}}(T) = \frac{1}{R^2(T)} \frac{2L_{\text{M21}}}{\mu(T) C_{ox} W_{\text{M21}}} \frac{(\sqrt{n}-1)^2}{n}, \qquad (15)$$

where n is the ratio between the areas of M21 and M22. To increase the accuracy of the bias current two phenomena should be accounted for in the PTIM bias generator: mobility degradation and velocity saturation, which are both short channel effects. The effective mobility is given by [5]:

$$\mu_{0\text{-eff}} = \frac{\mu_0 v_{\max} L}{v_{\max} L(1+\theta V_{\text{OV}}) + \mu_0 V_{\text{DS}}}, \qquad (16)$$

where $v_{\max}$ is the maximum velocity of the carriers in the channel, θ is a technology dependent fitting parameter and $V_{\text{OV}} = V_{\text{GS}} - V_{\text{TH}}$ is the overdrive voltage. The effective mobility is thus dependent on the MOSFET's biasing conditions. The overdrive voltage of the gain cell transistors M1/M2 is equal to the overdrive voltage of M21/M22 in the bias generator if they have the same current density and the same unit device. Simulation results in Fig. 7a show the gain error over temperature for different L sizes inside the bias generator (same W/L ratio). When M21/M22 use the same unit device as M1/M2, the gain error over temperature reduces to <0.5 dB. In order to bias M1/M2 and M21/M22 with similar V_{DS} voltages, cascode devices M24/M25 are employed in the bias generator. This further reduces the gain error over temperature to <0.1 dB for the extreme corners, as shown in Fig. 7b.



(a) Different L-sizes in bias generator, constant W/L, $L = 0.18\,\mu$m in gain cells.

(b) With- (solid) and without- (dotted) cascodes in bias generator, $L = 0.18\,\mu$m in gain cells and bias generator.

Fig. 7: Normalized gain error over temperature.

E. PTM Current Scaler and I-V Conversion

The translinear-loop shown in Fig. 8 implements the current relation from (12). As a result, the PTIM dependence is removed from the log-amp detector current output. For convenience the available bipolar devices were used for the translinear-loop. For a complete CMOS implementation these can be replaced with MOSFET's biased in weak-inversion. Resistor R_{filt} and a non-inverting amplifier performs the final I-to-V conversion.

IV. Measurements

A. Performance Metrics

1) Log-Conformance Error (LCE): This metric shows the error versus an ideal logarithmic curve:

$$\text{LCE}_{\text{error}}(\text{dB}) = \frac{(V_{\text{out},1} - (K_S \cdot (P_{\text{in},1} - P_0))}{K_S}. \qquad (17)$$

2) Temperature Drift: This metric shows the difference between the log-amp detection transfer at a certain temperature in relation to the transfer obtained at a reference temperature (generally 25°C). It is expressed in dB in this paper.

B. Measurement results

A batch of 24 samples was measured for sinusoidal inputs at 100, 700, 900, 1500, 1800 and 2100 MHz over the full input power range (-50 to +10 dBm). The detection curves were obtained at -40, +25 and 85°C for a fixed 1.8 V supply

voltage. The prototype IC has an active area of 0.76 mm^2 and draws 6.3 mA from the supply.

Fig. 9 shows the typical (average among the 24 samples) detection (a) and LCE (b) curves for all measured input frequencies. Up to 900 MHz the intercept shift is negligible. This is accordance with the simulated -3 dB BW of the four cascaded gain cells at 930 MHz.

Fig. 10 shows the typical LCE plots at -40, +25 and +85°C. The DR for ±1 dB LCE is 39 dB at 25°C for frequencies between 100 and 700 MHz.

Fig. 11 shows the temperature drift for the extremes of the temperature range (-40°C and 85°C) in relation to 25°C. Up to 900 MHz the temperature drift is never larger than ±1.1 dB for all 24 measured boards. This result was achieved without employing any method of temperature calibration. For input frequencies above the -3 dB BW of 930 MHz, the temperature errors become larger.

Table I shows the measured DR and temperature drift for several frequencies and metrics. Fig. 12 shows a microphotograph of the prototyped IC.

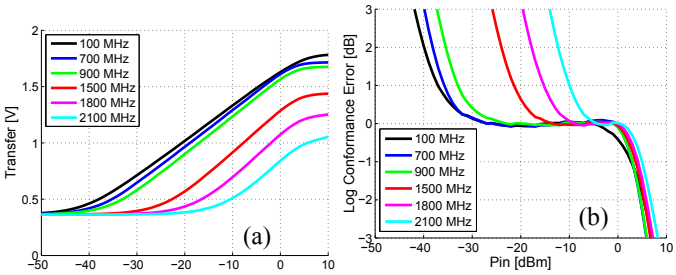


Fig. 9: Typical Detection Curves (a) and LCE (b) over frequency.

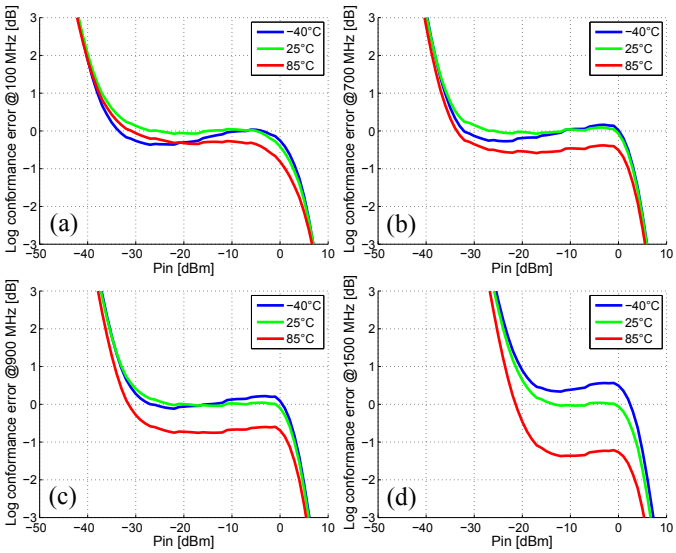


Fig. 10: Typical LCE for 100 (a), 700 (b), 900 (c) and 1500 MHz (d).

V. Conclusions

A complete implementation of a RF power detector in 0.18 μm CMOS technology based on the log-amp structure was demonstrated. Thanks to the temperature compensated architecture, the temperature drift is bounded to ±1.1 dB from -40°C to 85°C for frequencies up to 900 MHz. The use of nanometer-scale CMOS technologies would extend the bandwidth of this architecture, enabling the coverage of higher frequency bands.

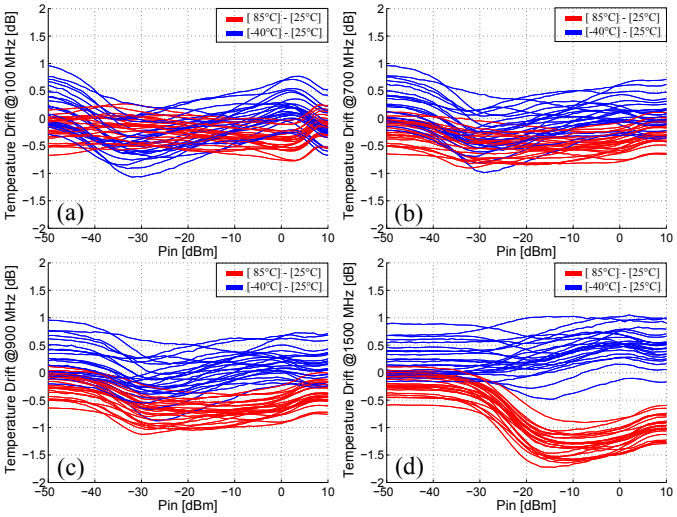


Fig. 11: Temperature Drift for 24 Samples at 100 (a), 700 (b), 900 (c) and 1500 MHz (d).

TABLE I: Performance summary - Typical DR [dB] at 25°C LCE and Max Temperature Drift [dB] for 24 samples.

Frequency	0.1 GHz	0.7 GHz	0.9 GHz	1.5 GHz	1.8 GHz
DR for ±1 dB LCE	40 dB	39 dB	36 dB	25 dB	19 dB
DR for ±3 dB LCE	49 dB	46 dB	43 dB	32 dB	27 dB
Max Temp. Drift	±1.1 dB	±1.0 dB	±1.1 dB	+1.1,-1.7 dB	+1.4,-1.9 dB

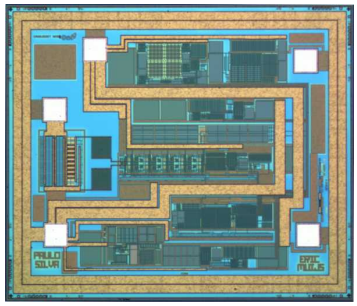


Fig. 12: Chip microphotograph

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