Fully Integratable Class-AB Rear-End with Smart Quiescent Current Control for a General-Purpose Hearing Aid Chip

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Abstract: In this paper, the core of the rear-end of an universally applicable analog hearing aid chip is described. It contains, apart from some subcircuits, a current-level Class-AB controlled preamplifier with three independent gain controls and a novel *half-switching* bridged final amplifier for various hearing aid receivers from low-power up to medium-power. To minimize supply current, the quiescent current of the amplifier string is optimized at any value of the input current and the controlled gain by a translinear quiescent current processor. Chip area in a 2.5-μm BiCMOS process amounts to 2.6 mm^2. Measured THD remains below 2% in all cases (1kHz). The bandwidth is >12kHz. All circuits operate correctly with a battery voltage down to 1.05V. Total current drain (without input signal) varies between 140μA and 425μA.

Introduction: A general problem in hearing aid industries is the fact that many different device types have to be constructed, each for a relatively small number of patients. Apart from the special demands with respect to filtering and AGCs, a great variety of output power ranges is demanded. To meet a major part of this problem, a general-purpose hearing aid chip was developed. The front-end, containing, among others, two preamplifiers, two AGC circuits, and two second-order filters, is described in [1]. This paper concentrates on the design of the most important circuits of the rear-end.

Boundary conditions and specifications: Battery voltage: 1.05-1.6V; (nominally 1.3V). Fully integratable on a 2.5 μm standard BiCMOS process including high-f_T vertical p-n-p's. Current drain must be minimized; Input current of the rear-end can vary from 60nA to 5μA. Maximal output voltage swing must be 2.4V (bridged final amplifier) The output current at 1kHz varies from 0.2mA to 1.5mA into the load, the impedance of which varies from 800Ω-6kΩ (1kHz). THD at 1kHz must remain below 2% at an output swing up to 6dB below maximum in all control situations. Finally, minimal bandwidth must be 8kHz. ***Desired gain controls and control ranges:*** The maximal *voltage* gain from microphone to receiver amounts to 60dB. ***Volume control:*** 0 to 40dB (normalized); ***Rx control:*** Tolerance compensation and voltage gain adaptation to the employed receiver: -20dB to +20dB; ***Rg control:*** Individual gain adaptation controlled by the audiologist: -20dB to 0dB.

General design aspects: Due to the large range of (very complicated) receiver impedances, the use of overall feedback to reduce distortion and inaccuracy is hardly feasible. An extra problem is that the amplifier must have a gain control range of totally 100dB! (volume control + Rx control + Rg control). Another serious problem concerns the offset and noise behavior of the amplifier. To cope with all problems the total amplifier string has been designed in *current-mode* with *indirect feedback* and is *class-AB operated.* Recently it has been shown, that these design strategies earn serious consideration in a low-voltage/low-power environment [2],[3].

Block diagram of the rear-end (Fig. 1): We resort to a description of the main amplifier string and the quiescent current processor. *Main amplifier string:* The output current of the front-end is fed to a phase splitter. Both signal halves are amplified by controllable current

amplifiers. Finally, the signal halves are amplified to their desired output levels by a bridged class-AB current amplifier. *The control voltages* vary from 10mV to 70mV (volume and Rx) and from 5mV to 35mV (Rg). In the *buffers*, a linear turning of the potentiometers (all 50kΩ) is converted into proportional control voltages, resulting in a gain control, directly into dB.

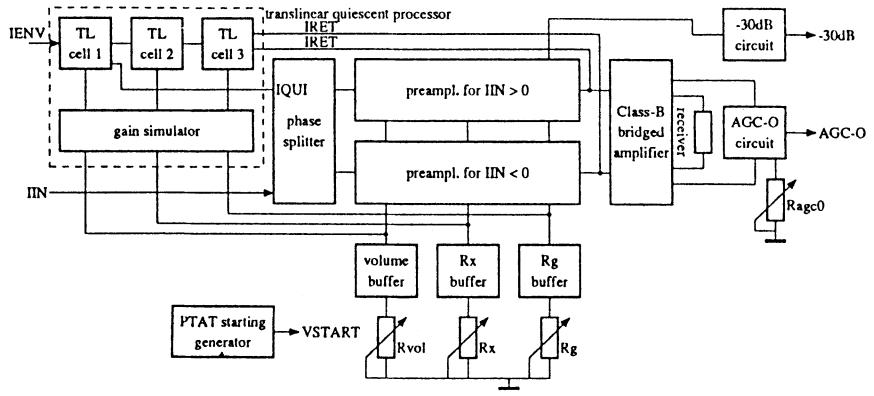

Fig. 1. Block diagram of the rear-end

The *translinear quiescent current processor* adapts the quiescent current at any combination of gain controls and IIN(peak), so that THD remains below 2%. In the front-end, a signal, proportional to the square root of IIN(peak) is already available [1]. This signal (IENV) is squared in the processor. As the preamplifier needs relatively more quiescent current than the final amplifier, the processor must also draw adequate return currents out of the final amplifier. Hence, optimal efficiency is gained. The correct values of the quiescent current (IQUI) and the return currents (IRET) were found by measurements. They are

$$IQUI = C_1 * \frac{IENV^2}{IGAIN} \text{ for } 2nA \le IQUI \le 500nA \text{ and } IRET = C_2 * IQUI * IGAIN, \qquad (1),(2)$$

with $C_{1,2}$ are constants and IGAIN is proportional to the total gain setting. IGAIN is calculated by the block *"gain simulator"*; IQUI by the block *TL-cell 1* ; and IRET by the blocks *TL-cell 2 and 3*. (Fig. 1). Eq. (1) and (2) could suggest, that IRET can directly be derived from IENV. However, the range of IRET must be much larger than that of IQUI, so that both currents must be calculated separately.

Detailed description (Fig. 2): The phase splitter splits the input current into a part IIN>0 and a part IIN<0 by the translinear cell Qa,b,c,d so that Ic(Qc).Ic(Qd)=$IQUI^2$. (classical class-AB relationship). *Note:* The two diodes being series circuited (Qa,b) suggests that the minimal supply voltage exceeds 1.05 volts. However, with the applied (small) values of IQUI the collector voltage of Qa never exceeds 1 volt. ***The controllable preamplifier*** amplifies input currents IIN>0 directly by an n-p-n current mirror. Currents IIN<0 are first inverted with a p-n-p current mirror. The current gain is controlled by the d.c. voltages in the emitter leads. Provided that Io/Ii<<βac of the n-p-n's, the gain amounts to 20log |Io/Ii|≈334(Ve1-Ve2)[dB] (at 300K) [4]. The preamplifier contains four of such combinations, two for the volume/Rx controls and two for the Rg control, each having a maximal gain (or attenuation) of 20dB (volume/Rx) or 10dB (Rg). ***The final amplifier:*** Currents >0 pass through Q1,2 for the driving of the left side of the receiver impedance Zl, and through Q3,4.5 for the driving of the right side of Zl. However, currents <0 pass through Q6,11,8,10 for driving the right side of Zl and through Q9,12,7 for driving the left side of Zl. Q2,5,7 and 10 are very large transistors to maintain a high efficiency. A special feature of the configuration is that the scaling of the p-n-p mirrors is much larger than that of the n-p-n mirrors (20 and 12, respectively). Consequently, the current gain is dominated by the n-p-n mirrors, whereas the p-n-p mirrors act as current

switches at relatively large output signals. The advantage is, that the collector voltages of Q2,5,7,10 have predictable values, so that a suitable AGC-O signal [1] easily can be derived.

The translinear quiescent current processor: To minimize tolerance errors, the *gain simulator* has been build up similarly as one half of the preamplifier. The three *TL-cells* are identical standard multipliers/dividers with a transfer z = x.u/y, where x, u, and y are the input currents [5]. The inputs of cell 1 through cell 3 are denoted in Fig. 2b as x1,2,3, y1,2,3, and u1,2,3, respectively. Cell 1 calculates IQUI in accordance with Eq. (1) and cell 2 and 3 calculate IRET in accordance with Eq. (2).

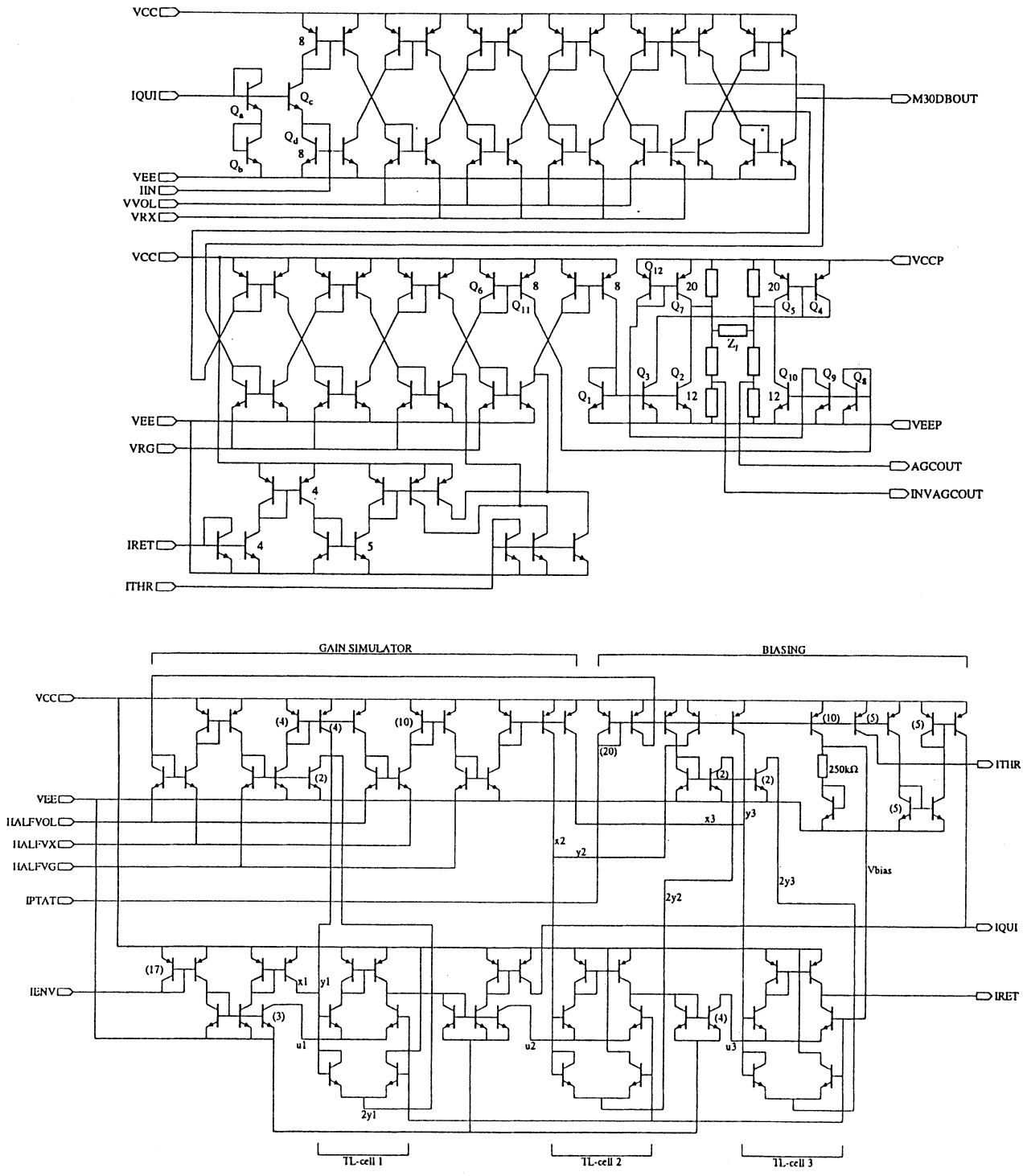

Fig. 2a,b. Circuit diagram of the amplifier string and the quiescent current processor

Simulation and experimental results: The following data are of simulations and measurements of a BiCMOS master chip with typical β-values of 215 (n-p-n) and 45 (v-p-n-p). ***Simulated voltages at both receiver terminals and their difference, at different gain values (fig. 3):*** Conditions: Input current IIN=60nA(peak) (1kHz); Rx=30kΩ; Rg=50kΩ (max.); Rreceiver=800Ω; Rvol linearly turned open in steps of 20% (yielding ≈ 8dB gain variation per step). The predicted switching effect of the p-n-p mirrors in the bridged final amplifier is clearly visible (upper plot). Further we observe that the receiver voltage reaches its saturation very smoothly, without irregular effects (lower plot). ***Demonstration of the (simulated) operation of the quiescent current processor (Fig. 4):*** Conditions: IIN=10sin(2π.600.t) exp.(41.47.t) [nA]; Rx=30k; Rreceiver=800Ω; Rvol=Rg=50k (max.). The lower plot shows the voltage over the receiver terminals; the central plot shows the outputs of the processor IQUI (lower trace) and IRET (upper trace). Finally, the upper plot shows the ultimate result: the current through one of the driver transistors in the final (bridged) amplifier (Q2 in Fig. 2). It is clear, that the lower peaks of this current remain at the same (low) dc value at any value of the input current, thus assuring efficient operation. Simulations with all other occurring values of the volume setting and the receiver impedance have shown similar results.

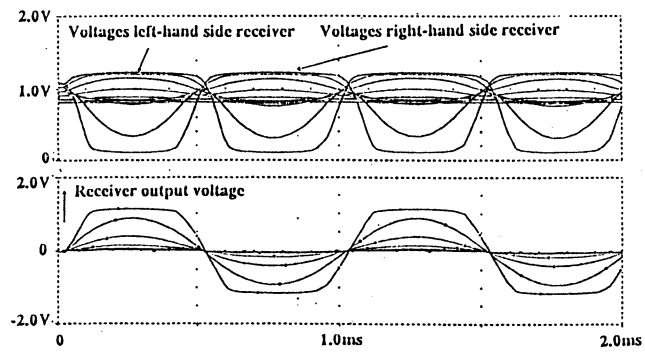

Fig. 3 Simulated output voltages

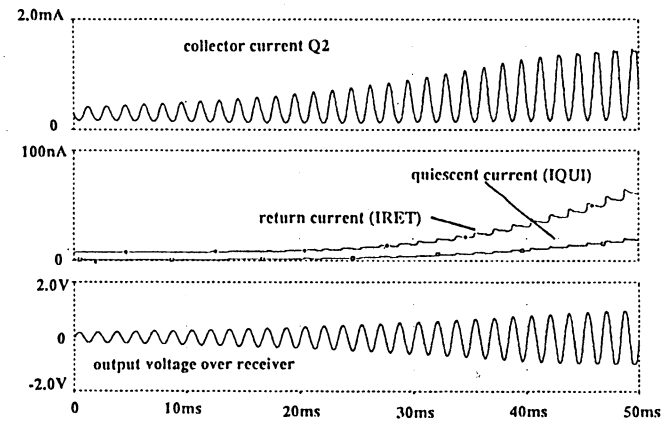

Fig.4 Operation of the quiescent processor

Measured results: Measured THD with various values of the controlled gain and IIN(peak) varied from 0.8% to 1.7% (at 1kHz, output signal 6dB below maximum); Quiescent supply current varied from 140μA to 425μA, depending of the employed receiver and the gain; Minimal bandwidth amounted to 12kHz; Minimal supply voltage for correct operation: 1.05V.

References:

[1] W.A. Serdijn; *The design of low-voltage low-power analog circuits and their applications in hearing instruments,* Delft University Press, Delft, ISBN 90-6275-955-6/CIP.

[2] W.A. Serdijn, A.C. van der Woerd, A.H.M. van Roermund, and J. Davidse; *Design principles for low-voltage low-power analog integrated circuits,* accepted for publication in Analog Integrated Circuits and Signal Processing 8 July 1995.

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[5] E. Seevinck, *Analysis and synthesis of translinear integrated circuits*. Elsevier; Amsterdam 1988, p.215.