Translinear sin(x)-circuit in MOS technology using the back gate

J. Mulder, A.C. van der Woerd, W.A. Serdijn, A.H.M. van Roermund

Electronics Research Laboratory, Delft University of Technology
Mekelweg 4, 2628 CD Delft, The Netherlands
Tel.: +31 15 78 11 83, Fax: +31 15 78 59 22
E-mail: j.mulder@et.tudelft.nl

Abstract - Though the MOS transistor is a four-terminal device, it is most often regarded as being a three-terminal device. Therefore, many possible MOS circuits are overlooked. In this paper, the four-terminal point of view is elaborated with respect to MOS weak inversion translinear circuits. It is shown that, by using the back gate, translinear networks can be derived which cannot be realized with bipolar transistors. These networks increase the possibilities offered by translinear technology. A sin(x)-circuit, which is one of the possible applications of the new network, was measured. The circuit can operate at supply voltages of less than 2 V and with a total bias current of only 14 nA.

I Introduction

The first translinear circuits, published in '68 by Gilbert [1], were designed using bipolar transistors. However, MOS transistors in weak inversion are also suitable for this type of circuit because of the almost exponential relation between the gate-source voltage and the drain current in this region [2]. In contrast with the bipolar transistor, the MOST is a four-terminal device. In subthreshold, the relation between the bulk-source voltage and the drain current is also exponential. A sufficiently accurate model for the drain current of a MOST in saturation is given by [3]:

$$I_{DS} = I_0 e^{V_{GS}/\kappa U_T} e^{V_{BS}/\eta U_T} \tag{1}$$

where I_0 is the zero-bias current, V_{GS} and V_{BS} are the gate-source and bulk-source voltage, $U_T = kT/q$ is the thermal voltage and κ and η are the inverses of the subthreshold slopes, which are constant in this model.

A simple way to design a MOS translinear circuit is to translate a bipolar circuit directly to its MOS equivalent, replacing the base-emitter junctions by gate-source voltages and connecting the substrate terminal of each MOS transistor to its source. Using this approach, the functionality of the substrate terminal as a second gate, or back gate, is not recognized and therefore a class of new circuits is ruled out in advance. As shown in this paper, the use of the back gate enables us to design translinear circuits that are not possible when using bipolar transistors. As an example, a sin(x)-circuit is presented. Measurements of a breadboard version of the circuit are shown.

II Translinear topology

The new translinear circuit topology is depicted in Fig. 1. The circuitry necessary to bias the MOSTs at the proper drain currents is not shown. For an NMOS implementation, as shown in Fig. 1, a double well process will be necessary. Of course, if the circuit is implemented in PMOS, only n-wells will be needed.

The circuit topology consists of a four-transistor gate-source loop in the up-down topology and two additional MOSTs biased at the same gate voltage. Of course, MOSTs with different back gate voltages have to be integrated in separate wells. Thus, M_1, M_3 and M_5 in the first well, and M_2, M_4 and M_6 in the second well. The back gates of M_1 and M_3 are connected together and the same applies for M_2 and M_4. The back gate voltages of M_1 and M_2 are determined by connecting their back gates to the back gates of M_5 and M_6. These two transistors have to be biased at the same gate voltage to obtain a theoretically process- and temperature-independent transfer function. Using the simple drain current model (1), the topology is described by an equation containing two squared currents:

$$\frac{I_1 I_3}{I_2 I_4} = \frac{I_5^2}{I_6^2} \tag{2}$$

The two squared currents result from the connection of the back gates of M_1 and M_3 and of M_2 and M_4. Because of this connection, the back gate voltages of M_1 and M_3 and of M_2 and M_4 are added, resulting in two factors 2. These factors 2 are the two exponents on the right-hand side of (2).

Equation structure (2) is different from the four different equations that can be realized with bipolar translinear networks [4]. Thus, this topology increases the number of possible translinear solutions for the realization of a given function. As this equation structure is more complex than the four mentioned 'bipolar' equation structures, in some cases, a higher functional density and thus area-efficiency can be obtained.

The topology shown in Fig. 1 can also be regarded in another way; the circuit consists of two loops of gate-bulk voltages. The first loop is formed by M_1, M_2, M_6 and M_5. The second by M_3, M_4, M_6 and M_5. The sources of M_1, M_4, M_5 and M_6 are connected to ground. The sources of M_2 and M_3 are tied together. Since no gate-source voltages are connected in series, the circuit is suitable for low-voltage applications.

III Sin(x)-circuit

As an example of the use of the new topology, a differential sin(x)-circuit was designed. Since the transfer function of a translinear circuit is always a rational function, an approximation for the sine function has to be used. According to [5], the sine function can be approximated by:

$$z = \sin \pi x \approx \frac{x - x^3}{1 + x^2} \tag{3}$$

where x and z represent the normalized input and output current, respectively. Another way of writing this approximation is the implicit decomposition [4]:

$$\frac{1 + z + x}{1 - z - x} = \frac{(1 + x)^2}{(1 - x)^2} \tag{4}$$

This decomposition can easily be fitted on equation structure (2) by choosing $I_2 = I_{bias} - I_{out} - I_{in}$, $I_3 = I_{bias} + I_{out} + I_{in}$, $I_5 = I_{bias} + I_{in}$, $I_6 = I_{bias} - I_{in}$ and $I_1 = I_4$. The sine shaped output current is obtained from $I_3 - I_2 - 2I_{in} = 2I_{out}$.

The complete circuit is depicted in Fig. 2. M_7 and M_8 are two simple floating voltage sources, which are used to keep M_5 and M_6 in saturation for bulk voltages of less than about 100 mV. Since the circuit is differential, a gain cell M_9 to M_{12} [1] is used to convert the input signal into a differential signal. Current mirrors are used to supply the currents to the actual sin(x)-circuit.

The applications of the general topology shown in Fig. 1 are not restricted to the example treated in this paper. Many other functions will fit on the topology, which in fact is the main strength of translinear technology.

IV Measurement results

A trivial application of (2) is the construction of a $\sqrt{x}$-circuit. To verify the new equation structure (2), a breadboard verion of the $\sqrt{x}$-circuit was measured. The drain currents through M_2, M_3, M_4 and M_6, shown in Fig. 1, are all biased at 1 nA. The drain currents of M_1 and M_5 are the input and output current, respectively. The gates of M_5 and M_6 are biased at 550 mV. The aspect ratios of the used NMOSTs are 108/7 μm/μm.

Measurements were performed using an HP4142B Modular DC Source / Monitor. In Fig. 3, the measured output current is compared with the theoretical curve. Clearly, the output current is proportional to the square root of the input current. The large errors at low and high values of the input current are caused by leakage currents of the measurement set-up and by the transition into the moderate inversion region, respectively. The main cause of error for intermediate current values is mismatch; the mismatch was quite large due to the breadboard realization. The average mismatch between the drain currents of two transistors at the same gate-source voltage was about 9%.

Next the sin(x)-circuit, shown in Fig. 2, was measured. The measured output current is shown in Fig. 4. The gates of M_5 and M_6 are biased at 350 mV. The supply voltages V_{dd} and V_{ss} are $\pm$1V and can even be lower, in principle. The bias current I_{bias} is 1nA, resulting in a total bias current of only 14 nA. The input current I_{in} ranges from 0 to 2 nA. The drains of M_2 and M_3 are loaded by two 500 mV voltage sources. Despite the rather large mismatch, due to the breadboard realization, which causes offset, asymmetry, amplitude, phase and frequency errors, the result is quite reasonable, as is shown by the comparison of the measured output current with a fitted sine function, see Fig. 4.

V Conclusions

Regarding the MOS transistor as a four-terminal device with a front and a back gate, a new translinear circuit topology was derived. This equation structure increases the number of possible designs for a certain function to be realized in translinear technology, and might result in more area-efficient implementations. As an example of the new topology, a sin(x)-circuit was designed. The circuit operates at supply voltages of less than 2 V, with a total bias current of only 14 nA. Measurements were performed which verify the theory, although they suffer from rather large mismatch of the MOSTs due to the breadboard realization.

References

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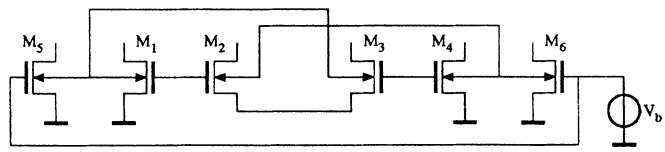

Figure 1: Topology described by equation structure (2).

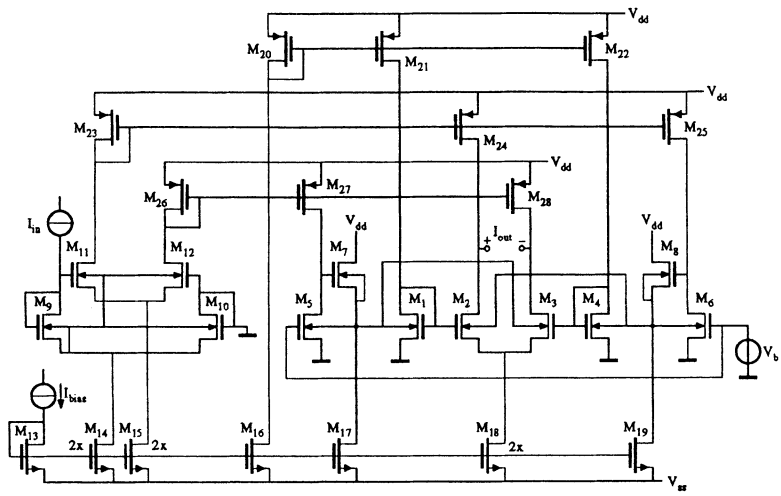

Figure 2: Sin(x)-circuit.

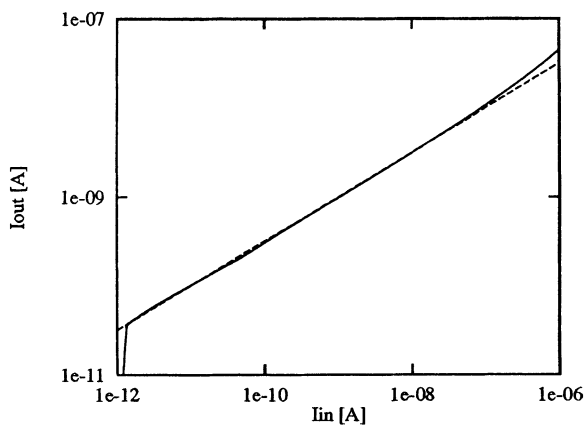

Figure 3: Output current of the square root circuit.

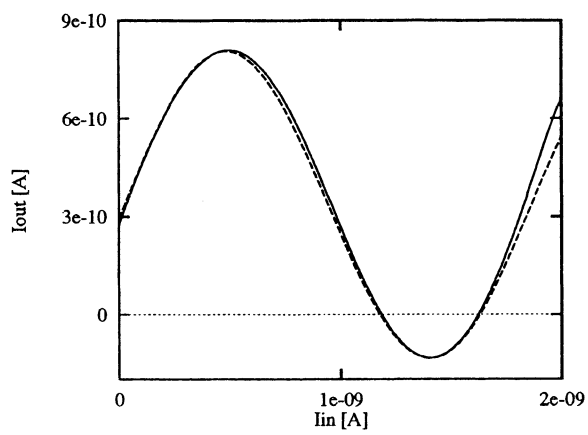

Figure 4: Measured output current (—) of the sin(x)-circuit and a fitted sine function (– –).