A Low-Voltage Low-Power Fully-Integratable Automatic Gain Control for Hearing Instruments

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Abstract

A low-voltage low-power bipolar automatic gain control (A.G.C.) that works in the current domain and operates on a single 1.3-V battery is presented. In this A.G.C. a large time constant (50 ms) is realized on-chip. The A.G.C. consists of a gain cell, a comparator and a voltage follower. The active circuitry of the A.G.C. has been integrated in the DIMES01 process and the total circuit demonstrates operation down to 1 V with 4μW power consumption.

1 Introduction

Apart from pitch, loudness and timbre information in the world of sound is characterized mainly by more or less sudden temporary changes. For someone with hearing impairment these variations do not fit within their dynamic range and therefore there is either the lack of certain parts of the information or the pain limit is regularly exceeded. In this situation an *automatic gain control* (A.G.C.) can offer certain improvement of the (speech) intelligibility.

An A.G.C. is a circuit that automatically controls its gain in such a way that variations of the input signal result in smaller variations of the output signal. This control action is performed by means of a loop in which a large time constant (i.e. several tens of milliseconds) is present. In the past this large time-constant was realized by means of a large (external) capacitor. However, to reduce the size and production costs to a minimum, external components need to be avoided as much as possible. This also holds for the power supply; the use of more than one single zinc-air battery is precluded. This means that the A.G.C. has to operate at 'low-voltage level' (i.e. 1–1.3 V) and consume as little current as possible to ensure long battery life.

In this paper the design of an A.G.C. that meets all the former specifications is presented. Section 2 presents a block diagram of an A.G.C. that operates in the current domain, consisting of three sub-circuits: a *gain cell*, a *comparator* and a *voltage follower*. Their design is presented in section 3. In section 4 the circuit diagram of the complete A.G.C. is presented. As an example the active circuitry was integrated in the DIMES01 process. In section 5 experimental results are given.

2 An A.G.C. in the current domain

In Figure 1 a typical A.G.C. circuit is drawn. The output signal E_l is compared with a reference level E_k (the knee level) by a comparator that determines whether the integrating circuit is charged (by E_{att}) or decharged (by E_{rel}). The output signal of the integrator E_{int} forms the control signal of the controlled amplifier. The operation is as follows: When E_{att} is larger than E_{rel} the amplitude of the output signal E_l is controlled towards the knee level E_k. Amplitude variations of the input signal therefore always result in smaller or equal variations of the output signal. Of course the control action needs some time. This can be described by the expressions *attack time* and *release time*. Because these times are absolutely unphysiological they are hard to choose correctly. However, satisfactory results are obtained by values < 5 ms and 50 ms, respectively.

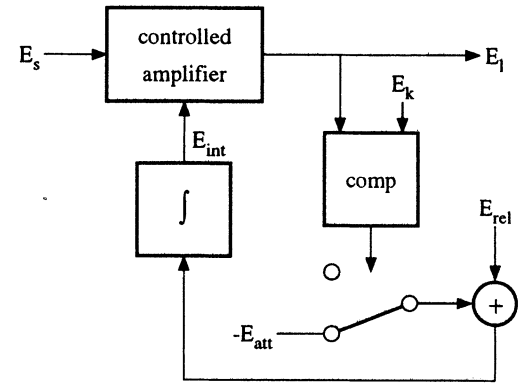

Figure 1: Block diagram of an automatic gain control

Low-voltage low-power circuits preferably operate in the current domain. This leads to the circuit diagram of Figure 2. Apart from E_{int} all signals are now represented by currents. The output of the integrator is a voltage, as the only integratable integrating element is

a capacitance. The capacitance is followed by a voltage follower that generates a low-impedance version of V_C.

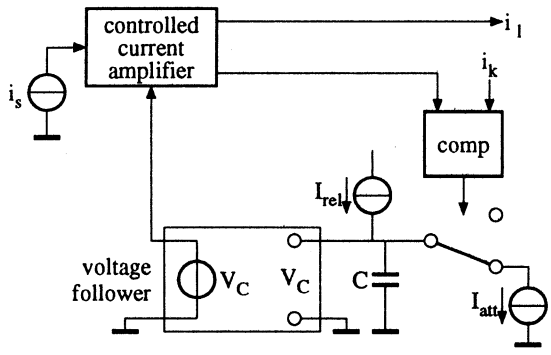

Figure 2: Block diagram of an A.G.C. operating in the current domain

3 Design of the subcircuits

So far the A.G.C. has been designed at *system level*. We now take a closer look at the design of its components: the controlled amplifier, the comparator (including the switch and current source I_{att}) and the voltage follower.

3.1 Design of the controlled amplifier

A suitable controlled amplifier is the symmetrical version of a current mirror, also known as a *Beta-Immune Type 'A' Cell* [1, chapter 2] (Figure 3). This is a controlled current amplifier which gain equals the ratio of the (DC) collector currents I_{C2} and I_{C1}.

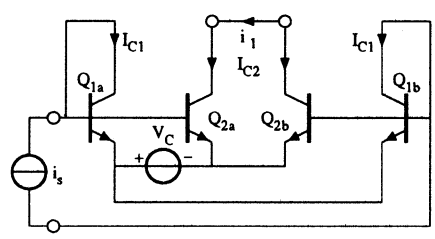

Figure 3: A symmetrical current mirror, also known as a *Beta-Immune Type 'A' Cell*

Another way of controlling the ratio of I_{C2} and I_{C1} is by means of controlling voltage V_C. We now obtain a gain (G) that is proportional to the anti-log of V_C, or:

$$G = i_{C2}/i_{C1} = e^{V_C/V_T} \qquad (1)$$

in which V_T equals the thermal voltage kT/q, approximately 26 mV at 300 K.

This exponential relationship between the gain G and the control voltage V_C enables us to control the gain over a wide range and is also perceptibly the most comfortable. If V_C is made proportional to the absolute temperature, the gain is independent of the temperature as well.

A possible implementation of a voltage-controlled symmetrical current mirror is given in Figure 4. Again the controlling is performed by means of transistors Q_{1a}, Q_{1b}, Q_{2a}, Q_{2b} and voltage source V_C. The circuit also contains a *common-mode loop* [2, 3, 4] for biasing the transistors correctly (Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a} and Q_{6b}). The collector current of both Q_{3a} and Q_{3b}, that equal the collector currents of both Q_{2a} and Q_{2b}, are added and compared with a current $2I$. The error signal controls via Q_4, Q_5, Q_{6a} and Q_{6b} the collector currents of Q_{1a} and Q_{1b}. Because the gain in this loop, the *common-mode loop-gain*, equals the current gain factor B_F of Q_{6a} and Q_{6b}, which is much larger than 1, the error signal is nullified and the symmetrical current mirror is biased correctly. Q_{sa} and Q_{sb} limit the maximum gain of the amplifier to one. Q_{da} and Q_{db} shunt the input and prevent the amplifier from clipping.

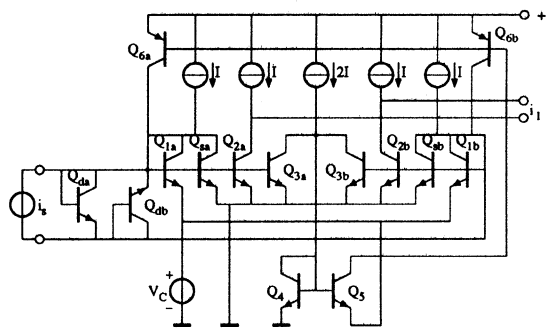

Figure 4: A symmetrical current mirror as used in the controlled amplifier including its biasing circuitry

3.2 Design of the comparator

The comparator is the subcircuit that decides whether the output current of the controlled amplifier is higher or lower than the reference level I_k. For this purpose we can either choose an amplifier with a saturated input-output relation or a cascade connection of a linear amplifier and a non-linear one-port. We have chosen for the latter option.

Using again a symmetrical current mirror for the amplifier and two shunting diodes at the input a possible implementation is given in Figure 5. Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a}, Q_{6b} and Q_{6c} form the common-mode biasing circuitry. In this case the *common-mode loop-gain* is kept sufficiently low (i.e. equals 2) to prevent instability in the comparator. The output current i_l therefore switches between 0 and $\frac{2}{3}I$. The two diode-connected transistors Q_{da} and Q_{db} prevent the amplifier from saturating; the comparator switches faster.

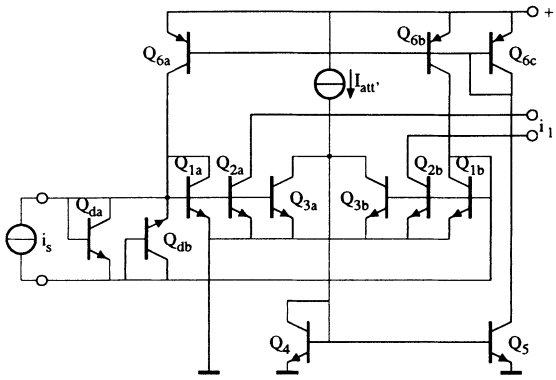

Figure 5: A symmetrical current mirror (type II) used as a comparator. The common-mode loop-gain equals two to prevent instability

3.3 Design of the voltage follower

The voltage follower forms a buffer between the capacitance C and the controlled amplifier. A single Field-Effect transistor (*JFET* or *MOST*) would perform this task very well, but as such devices are not yet well specified for applications in low-voltage circuits a sufficiently high input impedance should be created by means of negative feedback [5]. A two-transistor solution is given in Figure 6. Although it might be confusing to see that the output voltage differs a base-emitter voltage from the input voltage, we have to realize that the voltage follower is part of a loop; the loop will control correctly.

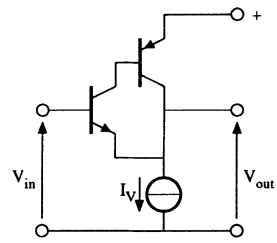

Figure 6: A two-transistor voltage follower

4 Overall design

Now that all the different parts of the A.G.C. have been designed at circuit level all the subcircuits are linked together and we take a closer look at the numerical values and the remaining bias circuitry.

When driving the filter as presented in [6] the maximum output current of the A.G.C. circuit is chosen to be 25 nano-amps (peak value). The reference current I_k (Figure 2) therefore has been chosen to be equal to 25 nA. The current sources I as depicted in Figure 4 have been chosen well above 25 nA and equal 100 nA.

The values of I_{att} and I_{rel} can be derived from the attack time (t_{att}) and the release time (t_{rel}). Some calculation yields:

$$I_{att} = \frac{5.2 V_T C}{t_{att}} - I_{rel} \tag{2}$$

and

$$I_{rel} = \frac{2.6 V_T C}{t_{rel}} \tag{3}$$

For $I_{att'}$ (Figure 5) it follows:

$$I_{att'} = \frac{3}{2} I_{att} = \frac{7.8 V_T C}{t_{att}} - \frac{3}{2} I_{rel} \tag{4}$$

With t_{att}, t_{rel} and C equal to 4 ms, 50 ms and 400 pF, respectively, this results in 20 nA and 540 pA for $I_{att'}$ and I_{rel}.

The current source I_v (Figure 6) supplies the collector current of the PNP transistor in the voltage follower and is chosen to be equal to 1 μA.

All these current sources can be derived from a single current by means of current mirrors with multiple outputs and convenient scaling factors. The scaling factor can be obtained by choosing either a proper emitter area ratio or by means of resistors. The latter solution yields either a *Widlar mirror* or a *gm-compensated mirror* [1, chapter 6].

The total circuit diagram of the A.G.C. is depicted in Figure 7. Two voltage sources (V_1 and V_2) have been added to prevent the current sources I_v and I_k from saturation.

In case of (common-mode) instability a capacitance C_{comp} can be added.

5 Experimental results

The active circuitry of the circuit shown in Figure 7 was integrated in the DIMES01 process (5 GHz, 2μm) fabricated at the Delft Institute of Microelectronics and Submicron Technology. Figure 8 shows a microphotograph of the chip. Experiments proved the correct operation of the A.G.C. Table 1 gives the measurement results. No instability occurred. The relatively large value of the release time is caused by the base current of the first stage of the voltage follower.

Table 1: Measurement results of the A.G.C.

Parameter	Value	Unit
Compression range	38	dB
Attack time, i_s=1 μA_p, 1 kHz	4.2	ms
Release time, i_s=10 nA_p, 1 kHz	58	ms
Dynamic Range, G=1, B=10 kHz	62	dB
Bandwidth	>100	kHz
Min. supply voltage	1	V
Supply current, G=1	4	μA

References

[1] C. Toumazou, F.J. Lidgey and D.G. Haigh (editors): *Analogue IC Design: the current-mode approach*, Peter Peregrinus Ltd., London, 1990.

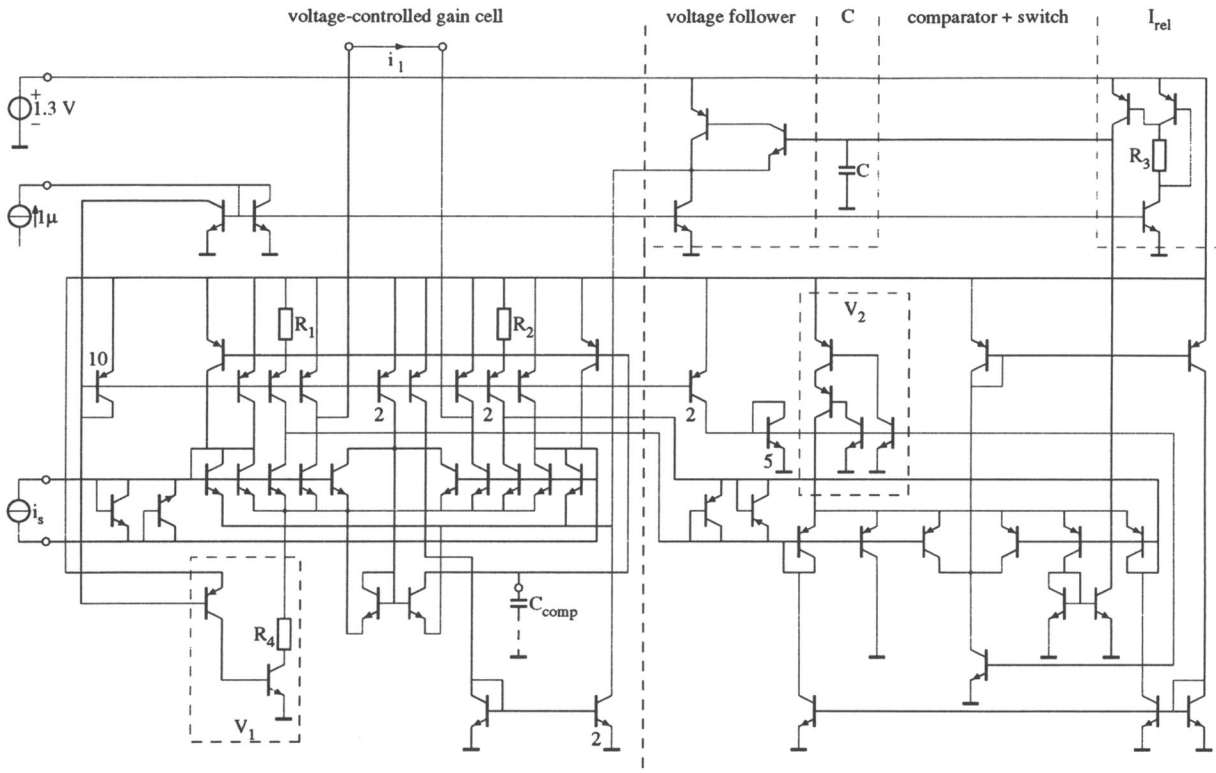

Figure 7: The total automatic gain control. Instability may be counteracted by C_{comp}

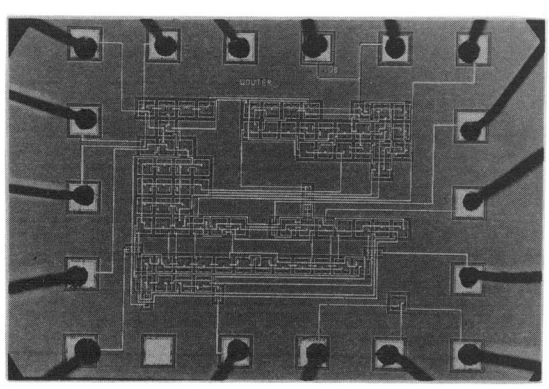

Figure 8: Photograph of the integrated circuit

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