35th Annual International Conference of the IEEE EMBS
Osaka, Japan, 3 - 7 July, 2013

An improved system approach towards future cochlear implants.*

N. S. Lawand, W. Ngamkham, G. Nazarian, P. J. French, W. A. Serdijn, G. N. Gaydadjiev,
J. J. Briaire, and J. H. M. Frijns.

Abstract — **Cochlear implants (CIs) have been used for many years to restore hearing for deaf patients. Unfortunately, today's CIs are still bulky devices and uncomfortable to wear. In this paper we present three innovations that ultimately should pave the way to a fully implantable bionic ear. First a microfabrication process used to fabricate the polymer metal microelectrode array for auditory nerve stimulation is discussed. Subsequently, a compact biphasic programmable stimulator chip to be used along with this electrode array is presented. By using a double loop feedback circuit topology, the circuit provides a precise stimulation current while requiring only little voltage headroom. The resulting low power consumption and reduced chip area allow for integration of the electronic circuitry onto the electrode array. Finally, as reliability and data transmission rate are two of the most critical issues in CI devices, we propose a software method to improve both data rate and reliability of transmitting digital data from the external part of the CI to the internal part with negligible power consumption.**

I. Introduction

Cochlear implants (CIs) are commonly accepted as therapeutic devices for clinical use and have restored hearing to more than 230,000 profoundly deaf people. CI devices consist of an external part that comprises a speech processor (DSP) and a microphone which together receive and convert the sound into a digital data stream using a speech processing strategy. The digital data is then transferred via an RF link to the internal part, viz. the receiver-stimulator package, which receives power and decodes the instructions for controlling the electrical stimulation via a multichannel electrode array placed inside the cochlea, giving an as rich and as natural perception of sound as possible. See Fig. 1 [1]. Users can have normal conversation in a relatively clean sound environment, but their hearing performance drops in complex environments, causing poor appreciation of music and inability to converse in crowded rooms (cocktail-party effect). Furthermore, the surgical placement of the device remains complex. The bottleneck is delivering more sound detail than is currently possible with the intra-cochlear electrodes used today. These are based on classic technology consisting of wires and platinum contacts in a silicone carrier. Because of the manual manufacturing process the number of stimulation contacts is limited (to about 20) and thus too small compared to the number of neural stimulation sites (+/- 3000). Moreover, the size of the electrode array is still too big to fit conveniently in the cochlea.

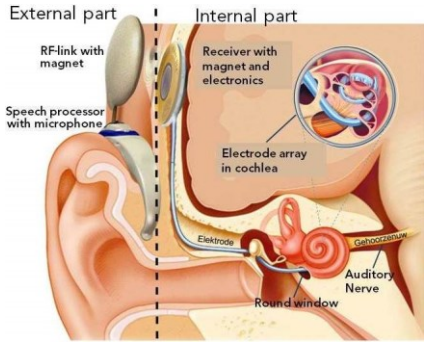

Figure 1. Cochlear implant with microphone, transmission coil, receiver-stimulator and electrode array fitted inside the cochlea [1]. (*Picture courtesy of Advanced Bionics ™, California, USA*).

For the receiver-stimulator package implanted inside the body there is a need to shrink the device size. This precludes the use of external components and requires the power consumption to be as small as possible to avoid the need for big batteries or capacitors. In addition to this, in order to deliver more sound details from the external to the internal part, software optimization on the algorithms running in the DSP can be used to generate reliable compressed digital data. In this paper, we present the progress made in the SMAC-It (Smart cochlear implants) project of Delft University of Technology and Leiden University Medical Center on three different topics a) flexible microelectrode array fabrication b) a charge balanced stimulator circuit and c) software optimization for reliable compressed digital data generation.

II. System Overview

In order to improve the functionality of CIs and simplify their surgical placement, a multi-disciplinary approach is required that takes into account reliability, biological interaction, power limitations and re-configurability and that spans both hardware and software related disciplines. The goal of the SMAC-It project is to research and develop technologies to address the above mentioned drawbacks in the following ways:

- By greatly increasing the number of electrodes using different biocompatible materials with their combined manufacturing possibilities.
- By greatly reducing the size and power consumption of the neurostimulator unit.
- By optimizing the software for reliable data transmission from the external part to the internal part of the device.

* This work was supported by the Dutch Technology Foundation STW with project title Smart Cochlear Implants (SMAC-It), Project Code: 10056.

N. S. Lawand, W. Ngamkham and G. Nazarian are with Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands. (e-mails: n.s.lawand@tudelft.nl; w.ngamkham@tudelft.nl; g.nazarian@tudelft.nl).

P.J. French, W. A. Serdijn & G. N. Gaydadjiev are with Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands. (e-mails: p.j.french@tudelft.nl; w.a.serdijn@tudelft.nl; g.n.gaydadjiev@tudelft.nl).

J.J. Briaire and J. H. M. Frijns are with the Leiden University Medical Centre (LUMC), P.O. Box 9600, 2300 RC Leiden, The Netherlands. (e-mails: j.j.briaire@lumc.nl; j.h.m.frijns@lumc.nl).

Each of the above related topics are discussed in the following subsections.

A. Microelectrode array fabrication

The CI electrode array is an important component of the implant and is in close proximity of the auditory neurons passing the external auditory information to the auditory cortex. Over the past decades, the design of these electrodes has developed from simple single channel devices to multiple site arrays consisting of 12 to 22 stimulation sites fabricated using metallic wires made of different materials for neural applications [2]. These are limited in electrode count due to the large size of the electrodes with respect to the size of the scala tympani (ST). Also the current design has restrictions for deeper insertion in the ST thus depriving access to the low frequency auditory neurons. Microfabrication using photolithographic and silicon micromachining techniques permits high volume, batch production of reliable microelectrode arrays with microscale dimensions. Such arrays can be used for highly localized stimulation and recording of neural tissue. Here we present the microfabrication of a flexible microelectrode array intended for in vitro and in vivo experiments thus displaying the fabrication capabilities for CI microelectrode arrays.

The fabrication took place in a class 100 cleanroom using 4 inch wafers as carriers. The P type wafers (<100>) were single side polished with low resistivity (2 – 5 Ωcm) and 525 ± 15 µm thickness. By thermal oxidation of the wafers a 1 µm thick inorganic Silicon Oxide (SiO_2) layer was first grown on both sides of the wafer at 1000^0C. Then on the front side pure Aluminium (Al) of 200 nm was sputtered by DC magnetron sputtering (Sigma 204 SPTS deposition system) at 25^0C and was patterned by standard lithography techniques. See Fig. 2-(1). This layer acts as an sacrificial layer to release the devices. After patterning, a 20 µm thick polyimide (Biomedical grade PI A115) is spun and was subsequently patterned by using a positive photoresist (AZ9260). An adhesion promoter (primer VM 562) is applied before PI spinning in order to achieve good adhesion between the oxide and the PI layer. After solvent evaporation (110^0C for 2 minutes) the PI layer was then cured for 2 hours at 400^0C in a Nitrogen environment. Its thickness was reduced to approximately 10 to 12 µm. See Fig. 2-(2). A metal stack (Ti-TiN-Al) (see Fig. 2-(3)) is then deposited by a DC magnetron sputtering machine. Titanium (Ti) of 40 nm is used as an adhesion layer between PI and the Titanium Nitride (TiN) of 200 nm, which is sputtered above Ti. TiN is the microelectrode material used for stimulating the auditory nerve fibres. Al (1.5 µm) is sputtered and patterned above TiN and is used as bond pads to connect the circuitry with the stimulation sites See Fig. 2-(4). The whole metal stack is deposited in one go by the puttering machine at 25^0C with pre-sputtering of the Ti target after each TiN deposition. After dry patterning of the metal stack the 2nd PI layer is deposited in a similar manner to achieve a thickness of 10 to 12 µm after curing. See Fig. 2-(5,6). The whole Pi layer (20 to 24 µm thick) is then patterned in oxygen plasma by using 200 nm of Al as a hard mask Fig. 2-(7). Later, the wet Al etching process gets rid of the hard mask and the underneath sacrificial layer. A freeze drying process after this sublimates the water between the PI and the underneath oxide layer to avoid stiction. The devices (Fig. 3) are released at the end by cutting of the PI strings attached as supports to the device. See Fig. 2-(9).

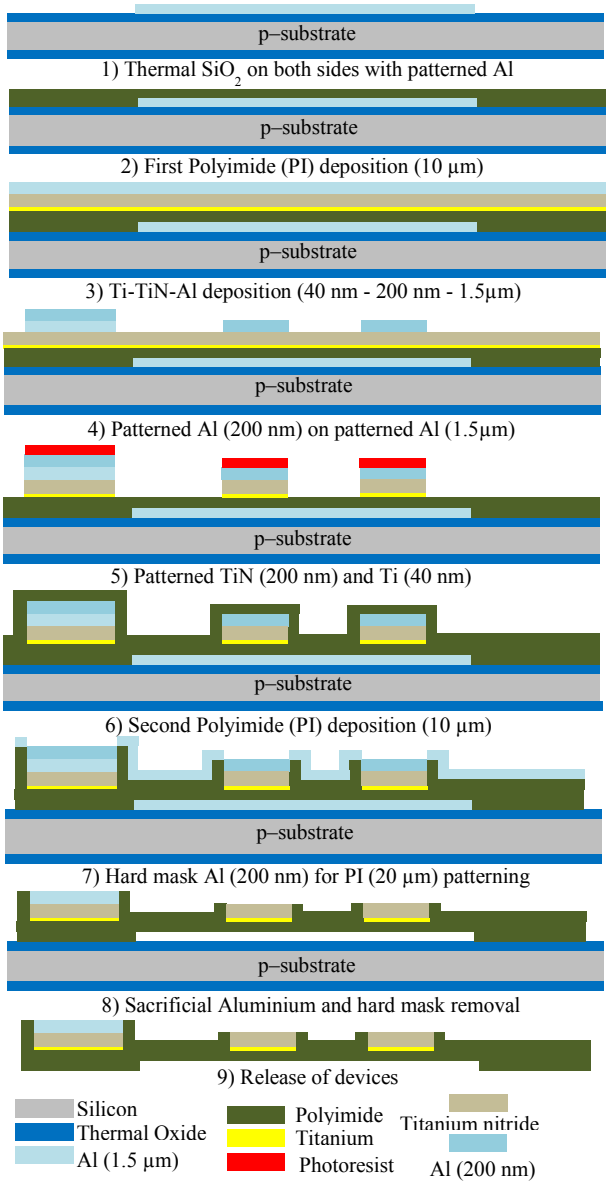

Figure 2. Process flow chart for flexible microelectrode array.

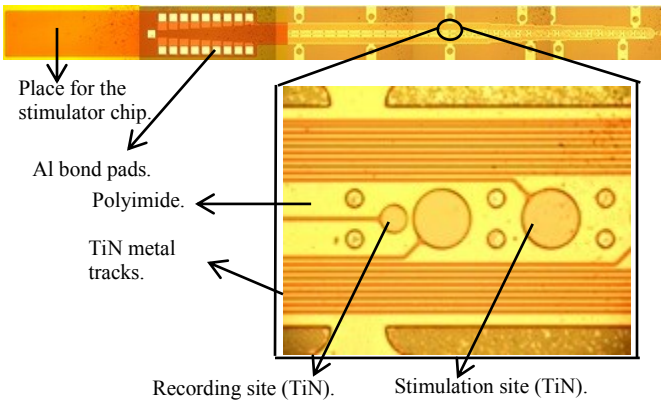

Figure 3. Fabricated flexible device with closer view of stimulation site.

B. *Charge balanced stimulator*

To support the flexible electrode array described in the previous sub-section a constant current mode, biphasic neural stimulator has been designed [3]. It features a small size and low power consumption. Moreover, it does not require a bulky coupling capacitor to guarantee charge balancing and thereby to prevent the tissue damage.

The stimulator circuit is shown in Fig. 4 and uses a single power supply to avoid the need for two accurate matched stimulation current sources [4]. It employs a double loop negative feedback topology [5] to increase the output impedance of the MOS current source and thereby increase the available voltage headroom for the load. The first internal feedback loop (comprising amplifier A_v and M3) is used for high precision scaling with a factor m of the stimulation current I_{stim} by making the drain voltages of M1 and M2 equal. This realizes a high output impedance of the current source without sacrificing voltage headroom (which is now reduced to only one effective V_{ds} of M2). The second feedback loop (comprising amplifier Z_m) accurately sets I_f (and thereby I_{stim}) equal to $n \cdot I_{ref}$ by forcing the error current $I_e = 0$. It is possible to adjust I_{stim} by controlling the factors m and n. Both current mirrors are implemented using a 7 bit binary weighted DAC scheme. The two feedback loops described above now give the relationship:

$$I_{stim} = m \cdot n \cdot I_{ref} = \sum_{u=0}^{2} a_u 2^u \cdot \sum_{l=0}^{3} a_l 2^l \cdot I_{ref}, \qquad (1)$$

in which u and l are the bit numbers and a_u and a_l are 0 or1 to disable or enable the corresponding bit.

A high voltage supply (>10V) is needed to accommodate the maximum current through the maximum load (electrode and tissue) impedance. This requires high-voltage (HV) transistors (indicated by the thick drain terminal) combined with low-voltage (LV) transistors. To minimize the chip area occupied by the circuit, the number of HV transistors applied should be as small as possible. The switch array (S_1, S_2 and S_3) is used in order to control the direction of the current injection into the electrode.

To verify the performance of the stimulator circuit AMS' 0.18µm HV process was used to implement the circuit shown in Fig. 4. The supply voltage was set at 18V in order to have enough voltage headroom across the load (1.05mA through R_L=10kΩ, while C_L=10nF is charging). Fig. 5. shows the layout and a die photo of the chip. The active area equals 200µm × 212µm, which is very small and can fit at the base of the electrode array prototype described in the previous sub-section. Fig. 6 shows the stimulation current in both positive and negative directions as a function of the applied digital code. For the same code the currents in both directions are almost identical. Fig. 7 a) shows the output voltage for the maximum load impedance, 10kΩ+10nF, at various stimulation currents. Fig. 7 b) shows the output voltage when using a CI electrode array in a saline solution as load. As can be seen from both figures the circuit works as expected. At the end of the stimulation cycle the output signal goes back to zero which means that proper charge balancing has been achieved. The worst case residue charge error is only 7.4 pC at 500 µA stimulation current tested with the 10kΩ+10nF load, 600µs stimulation cycle and 50µs stimulation pulses, a value well below any safety limits.

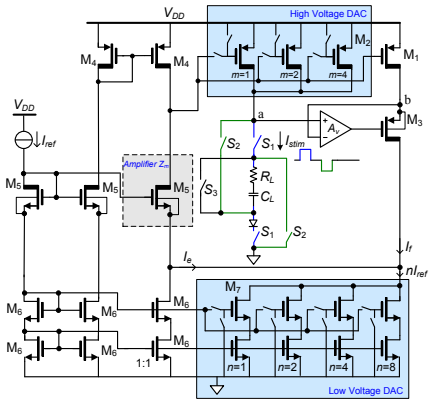

Figure 4. Principal circuit diagram of the implemented stimulator circuit.

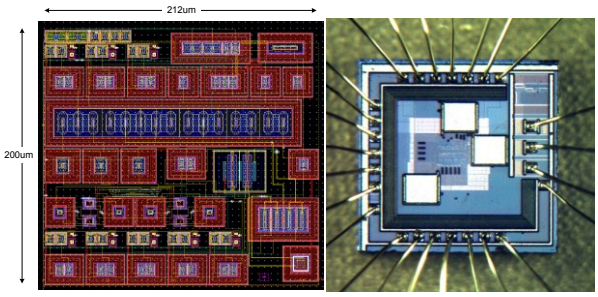

Figure 5. Layout and die photo of the stimulator circuit.

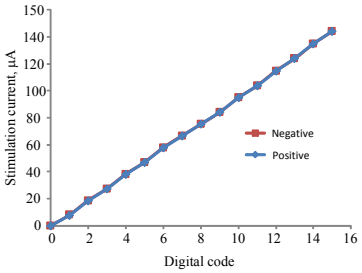

Figure 6. Stimulation current in both positive and negative directions.

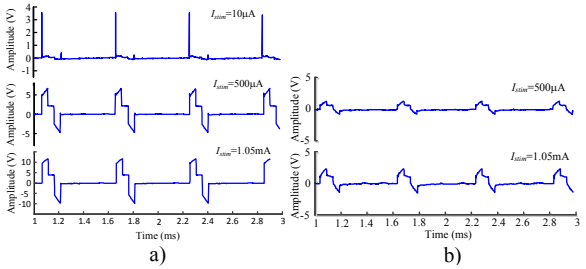

Figure 7. Output load voltages for a) a 10 kΩ+10 nF load and b) for a CI electrode load in saline solution.

C. *Software solution for compressed reliable digital data generation.*

A CI is an instance of a microelectronic implant and has the generic requirements of these devices as reported in the literature [6]. In the SMAC-It project we have tackled two essential requirements using pure software solutions. These requirements are that: **(1)** collected data (digital data of sound

features generated in the DSP) should be saved for later telemetry, thus data **compression** is required for higher transmission rate; **(2)** the data must be transmitted **securely** and **reliably**. An effective method to satisfy these requirements is by using dedicated software running on the DSP. This approach does not require any extra hardware. We use a program called Finish (Fin) (also included in ImpBench [7] - an ultra-low power biomedical benchmark suite) for **data compression** of the DSP data. For the **encryption** of the data and **securing** the transmission we use RC6. For guarding the data integrity for the above two programs Checksum and CRC32 are used.

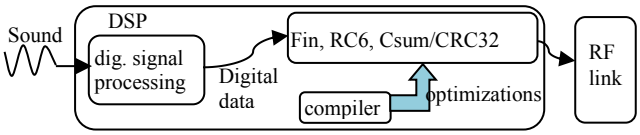

Figure 8. Reliable and compressed digital data generation.

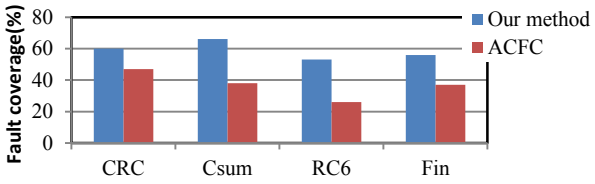

Figure 9. Fault coverage comparison.

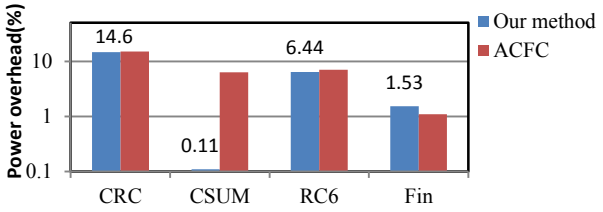

Figure 10. Power consumption overhead.

The overall result of the above programs (Fin, RC6, Checksum and CRC32) on the digital data as input is a compressed and encrypted data with integrated integrity checks. In order to improve the system reliability and make the processor resistant to transient faults (temporary faults caused by environmental effects) we have optimized the compiler of the processor. The optimized compiler automatically adds check assertions into the critical parts of the executable binaries. Fig. 8 depicts an overview of our setup for compressed reliable data generation. The assertions inspect the correct control flow of the program during execution. The optimization mechanism is as follows: first, the possible control-flow paths in the executable code are identified; second, check assertions are added at the end of each identified control-flow path; third, in case a check assertion detects a control-flow error a special register of the processor is set to "1" and the program is re-executed from the beginning to recover from the transient error.

Our optimized compiler generates executable binaries able to detect a very high percentage of the control-flow errors with minimal overheads (power-consumption overhead being the most important in battery operated devices such as CI). Compared to the previously proposed compiler optimization with minimal overhead named Assertion based Control Flow Check, ACFC [8], our optimization has on average 17% higher fault coverage with 2.75% reduction in power consumption overhead. We have obtained the fault coverage results by executing each program 1000 times and injecting a control-flow error (by changing the correct destination of branch instructions in the executable under test) using the Synopsys Processor-Designer simulator [9]. For each execution run the **special register** is checked to identify if an error has occurred or not. Fig. 9 shows the fault coverage of our proposal compared to ACFC and Fig. 10 shows the corresponding power-consumption overheads of both methods.

III. Conclusions

To pave the way to the development of future fully implantable CIs, three innovations are presented in this paper: 1) flexible microelectrode array fabrication abilities using different biocompatible materials and strategies outperforming classical technology; 2) a charge balanced stimulator chip, producing a residue charge unbalance well below the safety limits; 3) improvement of the digital data transmission rate by customized software optimization able to generate reliable compressed data in the DSP.

Acknowledgment

The authors acknowledge the Dutch Technical Foundation (STW) (Project no. 10056) and Advanced Bionics™, USA for their support to this project.

References

[1] Figure from Advanced Bionics™: http://www.advancedbionics.com.
[2] D. J. Anderson , K. Najafi, K. D. Wise, "Batch-Fabricated Thin-film Electrodes for Stimulation of the Central Auditory System," *IEEE Trans on Biomedical Engg.* Vol. 36, No. 7, July 1989, pp. 693-704.
[3] W. Ngamkham, C. Sawigun, and W. A. Serdijn, "Biphasic Stimulator Circuit for a Wide Range of Electrode-Tissue Impedance Dedicated to Cochlear Implants," *Proc. IEEE International Symposium on Circuits and Systems*, Seoul, Korea, May 20 - 23, 2012.
[4] J. J. Sit, and R. Sarpeshkar, "A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6nA DC error for 1-mA full-scale stimulator," *IEEE Tran. Biomedical Circuits Syst.*, vol. 1, no. 3, pp.172-183, Sep. 2007.
[5] C. Sawigun, W. Ngamkham and W. Serdijn, "A least-voltage drop high output resistance current Source for Neural Stimulation," *IEEE BioCAS*, Paphos, Cyprus, Nov. 3-5, 2010.
[6] C. Strydis, G.N. Gaydadjiev, "The Case for a Generic Implant Processor," *30th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC 2008),* 21-23 August 2008, Vancouver, Canada.
[7] C. Strydis, C. Kachris, G.N. Gaydadjiev, "ImpBench: A novel benchmark suite for biomedical, microelectronic implants," *International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (IC-SAMOS 2008),* 21-24 July 2008, Samos, Greece.
[8] R. Venkatasubramanian, J. P. Hayes, and B. T. Murray, "Low-cost online fault detection using control flow assertions," in 9th *IEEE On-Line Testing Symposium. IEEE*, July 2003, pp. 137–143.
[9] Synopsys processor designer. [Online]. Available: http://www.synopsys.com/Systems/BlockDesign/processorDev/Pages/default.aspx.