Fig. 5 shows the eye diagrams of light signals during 156Mbit/s NRZ, zero-bias modulation. Feedforward control for both the drive current and its pulsewidth was carried out for a 1.3μm wavelength, low-threshold LD. The rise and fall times were 50 and 280ps, respectively. The average optical power was −1.4dBm at 0°C and −1.3dBm at 70°C. The pulsewidth was 99.5% at both temperatures. Thus, a small deviation of the light output power (<±0.1dB) and the pulsewidth (<±0.1%) over a wide temperature range was obtained. These results suggest that APC-free burst-mode transmitters are practical using this LD driver IC.

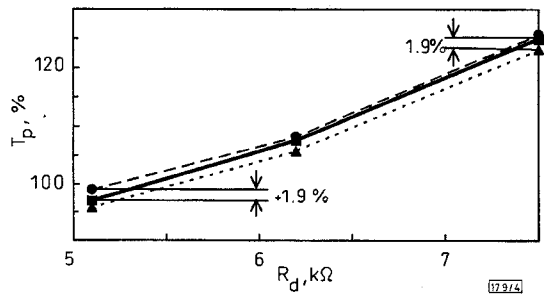

Fig. 4 *Pulsewidth during 156Mbit/s NRZ modulation when T_a is between 0 and 70°C*

V_{dd} is +3.3V ± 10%, and I_p is 38mA
● maximum
■ T_a = 25°C, V_{dd} = +3.3V
▲ minimum

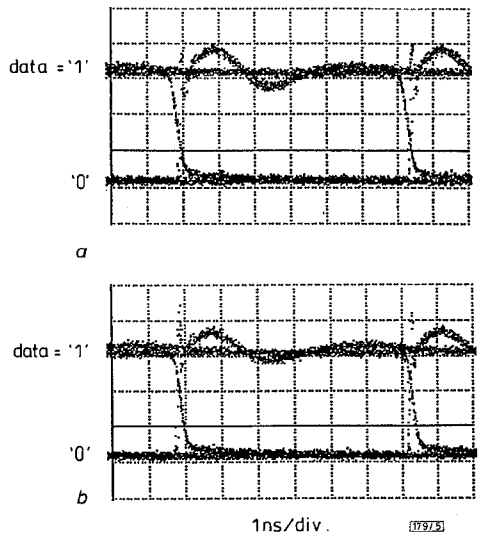

Fig. 5 *Eye diagrams during 156Mbit/s NRZ, APC-free modulation at zero-bias when V_{dd} is +3.3V*

a T_a = 0°C
b T_a = 70°C

Conclusions: A burst-mode CMOS LD driver IC for 156Mbit/s transmission has been developed. By introducing a precise drive current controller and a novel pulsewidth controller into an APC-free LD driver IC, we obtained a wide range of control for the drive current and pulsewidth, with a small deviation of <±2%. Using this IC, small deviations of the light output power (<±0.1dB) and its pulsewidth (<±0.1%) were achieved with an APC-free, zero-bias modulation.

4 February 1997
Electronics Letters Online No: 19970548

T. Inoue, H. Nobuhara, S. Ide, K. Nakajima, T. Ikeuchi and K. Wakao (*Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi Kanagawa 243-01, Japan*)

K. Tsubaki and N. Ueno (*Fujitsu Limited, 4-1-1 Kamikodanaka, Nakahara-ku, Kawaski 211, Japan*)

A. Hayakawa (*Fujitsu VLSI Ltd., 2-1844-2 Kouzouji-cho, Kasugai, Aichi 487, Japan*)

E-mail: tinoue@flab.fujitsu.co.jp

References

1 NAKAMURA, M., FURUYAMA, H., and KUROBE, A.: '1Gbit/s automatic-power-control free zero-bias modulation of very-low threshold MQW laser diodes', *Electron. Lett.*, 1987, **23**, (25), pp. 1352–1353
2 IKEUCHI, T., MORI, K., NOBUHARA, H., TANAKA, K., and FUJIMOTO, N.: 'High-speed APC-free modulation for burst-mode transmitter'. Optoelectronics Commun. Conf. (OECC'96) Tech. Dig., 1996, pp. 236–237
3 KIMURA, M., YANAGISAWA, H., YOKOMIZO, M., HONMA, Y., and TAMURA, T.: '156Mbit/s burst mode optical transmitter module'. Proc. 1995 Commun. Soc. Conf. IEICE, 1995, Vol. B-663, p. 330 (in Japanese)
4 FUJIMOTO, N., WAKAO, K., and YANO, M.: 'Intelligent parallel optical link – Parallel optical transmission system and LSIs', *Fujitsu, Sci. Tech. J.*, 1994, **30**, (2), pp. 214–223 Japan,

Current-efficient CMOS transconductor for continuous-time g_m-C filters

W.A. Serdijn, J.C. Kuenen, J. Mulder, M. van de Gevel, A.C. van der Woerd and A.H.M. van Roermund

Indexing terms: Continuous time filters, CMOS integrated circuits

The authors present a CMOS transconductor, based on a new two-transistor single-ended differential pair, that is able to process signals from rail to rail. It has a low noise factor, a large bandwidth, is very current efficient and is easily biased and tuned by only one current.

Introduction: At present there is a growing interest in low-power and low-voltage IC designs. This is mainly caused by the increasing commercial importance of portable battery-operated systems. Electronic filters are important building blocks in electronic systems for the separation of desired signals from unwanted signals and noise, by using the differences in their energy-frequency spectra. Since every filter can be considered to consist of a network of integrators, the overall filter performance is strongly related to the individual integrator performances [2]. Good quality filters therefore require good quality integrators. The major quality aspects of continuous-time integrators are: distortion, noise production, phase response, power consumption and tunability.

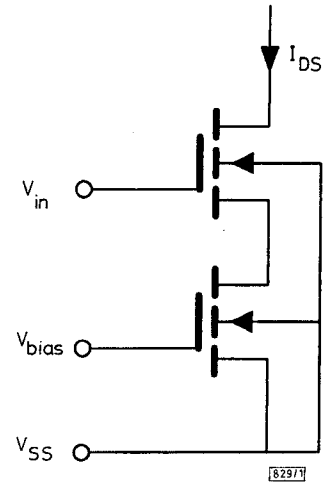

Fig. 1 *Basic circuit principle*

Upper transistor operates in saturation region, lower operates in triode region. Output current corresponds with that of conventional single-ended differential pair

Traditionally, two methods have been used to realise integrators: one is known as the opamp-R-C method; the other is the transconductor-C (or g_m-C) method. The latter is widely used in

high frequency and/or medium/low precision filter applications [3]. With respect to the above quality aspects, g_m-C integrators should thus preferably be able to process the signals linearly from rail to rail, have a noise factor which is close to unity [2], be insensitive to parasitic capacitances, be current efficient and be easily tunable.

In this Letter we present a CMOS transconductor, the g_m part of the integrator, based on a novel single-ended differential pair, that fulfills all these requirements. In the following Sections, attention is paid to its principle of operation, the biasing/tuning circuitry and the experimental results.

Principle of operation: The principle of operation of the proposed circuit is best explained from the basic circuit depicted in Fig. 1 [1]. The upper transistor operates in the saturation region ($V_S \gg V_D$) and the lower transistor in the triode region ($V_S \simeq V_D$). In weak inversion, the drain current I_{DS} of a single transistor, with the bulk connected to ground, is given by [4]

$$I_{DS} = I_0 \exp\left(\frac{V_G}{\kappa V_T}\right)\left(\exp\left(\frac{-V_S}{V_T}\right) - \exp\left(\frac{-V_D}{V_T}\right)\right) \quad (1)$$

I_0 being the zero-bias current, κ the subthreshold slope factor, V_T the thermal voltage kT/q and V_G, V_D and V_S the gate, drain and source voltages, respectively, referenced to the substrate.

In strong inversion, the drain current is given by [4]

$$I_{DS} = \frac{W}{L}\frac{\beta}{2}((V_G - V_S - V_{th})^2 - (V_G - V_D - V_{th})^2) \quad (2)$$

W, L, β and V_{th} being the width, length, transconductance factor and the threshold voltage, respectively.

Both expressions are valid in both the triode region and the saturation region. Hence, for a series connection of two transistors according to Fig. 1, the drain current of both transistors, I_{DS}, is given by

$$I_{DS} = \frac{I_{bias}}{2}\left(1 + \tanh\left(\frac{V_{in}}{2\kappa V_T}\right)\right) \quad (3)$$

with $I_{bias} = I_0\exp(V_{bias}/\kappa V_T)$, in weak inversion, and

$$I_{DS} = \frac{I_{bias}}{2} - \frac{W}{L}\frac{\beta}{2}V_{in}\sqrt{\frac{L}{\beta W}I_{bias} - \left(\frac{V_{in}}{2}\right)^2} \quad (4)$$

with $I_{bias} = [W/L][\beta/2](V_{bias}-V_{th})^2$, in strong inversion. V_{in} is the input voltage, referenced to V_{bias}. The above drain currents are exactly the same as those of one of the transistors of a conventional differential pair, its tail current being equal to I_{bias}. The analogy goes even further: when both sources are degenerated by means of a series resistor, the circuit corresponds to the conventional degenerated differential pair with a source-degenerated tail current source.

The circuit of Fig. 1 has two important advantages over the conventional differential pair. First, since the lower transistor operates in its triode region, the output voltage swing can be almost as large as the supply voltage. This is especially advantageous in a low-voltage enviroment. Secondly, the total current consumption is no more than the output current. This yields an average current saving of 50% with respect to the conventional differential pair.

As is the case with all single-ended differential pairs, this differential pair also has a noise factor of 2. Apart from this, an additional bias current source is necessary to provide the drain current. This current source limits the available output voltage swing of the transconductor and adds noise. These problems can be overcome by connecting two transconductors in anti-parallel (at both input and output) for their signal behaviour, and in series for their biasing. The resulting circuit diagram is depicted in Fig. 2. The noise factor now equals unity again.

Although this circuit shows some resemblance to that presented by Nauta [5], the distortion of the circuit in Fig. 2 does not depend on the matching of two complementary transistors, but of two that are identical. As a result, the distortion of the transconductor can be rather small over its complete output voltage range.

From Fig. 2 it can also be deduced that, in a filter network, the influence of parasitic capacitances will be small, since these are either connected in parallel with the integrator capacitors or shunted by small resistances. For the integrator, this yields a 90° phase shift over a very wide frequency range.

Biasing/tuning circuitry: The biasing/tuning circuit of the proposed transconductor is depicted in Fig. 3. The biasing/tuning current I_{bias} flows through diode-connected transistor pairs MN3/MN4 and MP3/MP4 and generates a voltage at the source of MP3. A voltage follower (transistors MN5, MN6, MP5, MP6 and MP7) generates a buffered version of this voltage, V_{pos}. The voltage follower bias current is delivered by transistors MN7 and MN8. V_{bias1} and V_{bias2} are lowpass filtered versions of the gate voltages of MN3

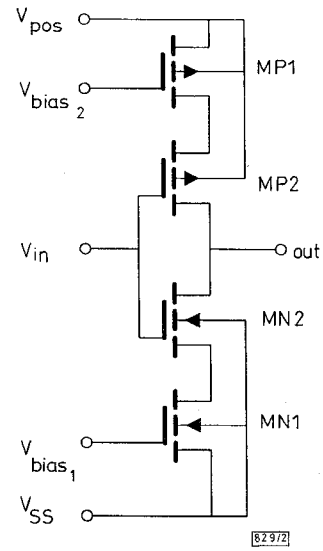

Fig. 2 *Circuit diagram of proposed transconductor*

and MP3, respectively. Both lowpass filters consist of two anti-parallel diode-connected transistors, acting as large resistances, and a capacitor. Thus, noise generated in the biasing/tuning circuit will not appear at terminals V_{bias1} and V_{bias2}. The current consumption of the circuit can be made sufficiently small, at the expense of a larger noise contribution, by choosing different transistor geometries. Whether or not this noise contribution is tolerable depends on the complete filter structure. Note that in a filter network with only one tuning parameter, e.g. the cutoff frequency, only one biasing/tuning circuit is necessary for the complete filter.

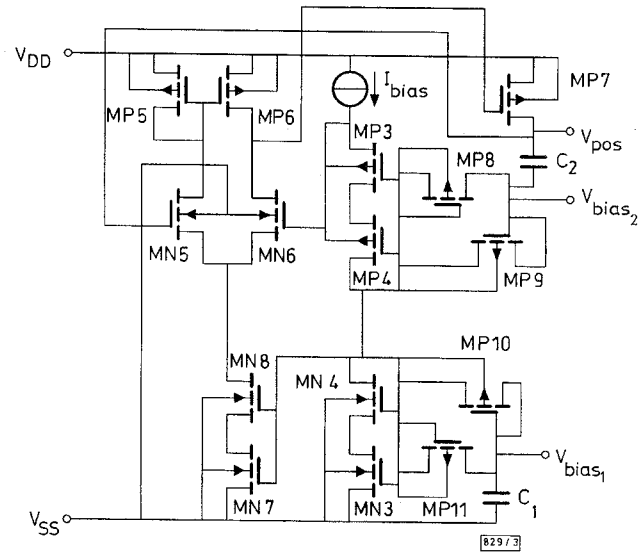

Fig. 3 *Biasing/tuning circuitry*

Experimental results: The proposed transconductor and its biasing/tuning circuitry were implemented in a breadboard realisation, using transistor arrays from a standard 2.5μm process. Typical values of the threshold voltages are 0.75 and –1V, for the NMOS and the PMOS devices, respectively. The aspect ratios of the transistors used are W/L = 108/7 for the NMOS devices and W/L = 108/7.5 for the PMOS devices, respectively. The circuit operated correctly for values of the biasing/tuning current I_{bias} up to 0.2mA, using a 3.3V supply. For larger supply voltages or larger W/L ratios, this current range can be further extended. DC measurements proved the equivalence with a conventional single-ended

differential pair, the tail current being 4 (!) × I_{bias}, and the circuit's rail-to-rail capability. AC measurements, using a 10mV input sine wave, showed a similar correspondence for the transconductance factor. The noise contribution of the proposed transconductor is 6dB smaller than that of the conventional single-ended differential pair, its tail current being equal to I_{bias}, indicating a noise factor of 1. As a result of the breadboard realisation, no high frequency measurements were possible. Simulations of the proposed transconductor revealed that its bandwidth (–3dB) equals that of the conventional single-ended differential pair, with its tail current again being equal to I_{bias}.

Conclusions: A current-efficient CMOS transconductor for continuous-time g_m-C filters has been introduced, which can easily be implemented in a standard CMOS process. The transconductor combines a rail-to-rail voltage swing with a wide bandwidth, an excellent dynamic range and good tunability.

Acknowledgments: The authors would like to thank R. van Beijnhem for the bread-board realisation of the proposed circuit. This research was financially supported by the Dutch Technology Foundation (STW), project DEL33.3251.

16 January 1997
Electronics Letters Online No: 19970552

W.A. Serdijn, J.C. Kuenen, J. Mulder, M. van de Gevel, A.C. van der Woerd and A.H.M. van Roermund (*Delft University of Technology, Faculty of Electrical Engineering/DIMES, Mekelweg 4, 2628 CD Delft, The Netherlands*)

E-mail: W.A.Serdijn@et.tudelft.nl

References

1 MULDER, J., VAN DE GEVEL, M., and VAN ROERMUND, A.H.M.: 'A reduced area low-power low-voltage single-ended differential pair', *IEEE J. Solid-State Circuits,* 1997, pp. 254–257
2 GROENEWOLD, G.: 'Optimal dynamic range integrators', *IEEE Trans. Circuits Syst. I,* 1992, **39**, (8), pp. 614–627
3 CASTELLO, R., MONTECCHI, F., REZZI, F., and BASCHIROTTO, A.: 'Low-voltage analog filters', *IEEE Trans. Circuits Syst. I,* 1995, **42**, (11), pp. 827–840
4 TSIVIDIS, Y.P.: 'Operation and modelling of the MOS transistor' (McGraw-Hill, 1987)
5 NAUTA, B.: 'A CMOS transconductance-C filter technique for very high frequencies', *IEEE J. Solid-State Circuits,* 1992, **27**, (2), pp. 142–153

Silicon bipolar 2V 2GHz quadrature demodulator without any adjustment

K. Shiojima, T. Tsukahara and M. Ishikawa

Indexing terms: Demodulators, Bipolar integrated circuits

A Si-bipolar direct-conversion quadrature demodulator with a flip-flop phase shifter achieves both low amplitude imbalance of ±0.1dB and a phase error of ±2° over a wide carrier frequency range between 0.1 and 2GHz, without any adjustment at a low power-supply voltage of 2V. The double-balanced mixer makes sure that the third-order input-referred intercept point is –3dBm and the second-order distortion is below the measurement noise level.

Introduction: Recent progress in portable equipment such as cellular phones, digital cordless phones, and wireless LANs has resulted in a growing demand for inexpensive, lightweight, and low-power equipment. Reducing the power-supply voltage is an effective way to meet this demand because such equipment is battery operated. Moreover, it has been shown that a direct conversion method eliminates the need for the IF bandpass filter, the upconverter, and downconverter, and one of the local oscillators for the intermediate frequency [1, 2]. Conversely, cost-effective Si bipolar technologies have resulted in improved high frequency performance up to the quasimicrowave range. We have demonstrated 2GHz Si bipolar direct-conversion quadrature modulators with power supplies as low as 2V [3]. Recent wireless systems require both very low phase error and low amplitude imbalance: within 3° and < 0.3dB for example in π/4-shift quaternary phase shift keying [4]. This accuracy is based on the performance of a 90° phase shifter. A conventional RC/CR 90° phase shifter provides less phase error, but manual adjustment is necessary to reduce amplitude imbalance. For the next advancement towards microwave monolithic integrated circuits, elimination of manual adjustment is strongly desired.

This Letter describes a 2V, 2GHz quadrature demodulator (QDEM) that needs no manual adjustment because it includes a flip-flop (FF) 1/2 divider as a 90° phase shifter. A Si-bipolar process technology whose transition frequency is as high as 40GHz enables the FF phase shifter to operate at a 4GHz frequency, twice as high as the local oscillator (LO) frequency. In this frequency range, however, in-phase (I) and quadrature-phase (Q) LO signals could leak through a Si substrate and couple. To overcome these problems, we enhanced the symmetry of the circuit layout and the isolation between elements. Additionally, all the signals were transmitted as differential signals in order to suppress the second-order harmonic distortion (IM2).

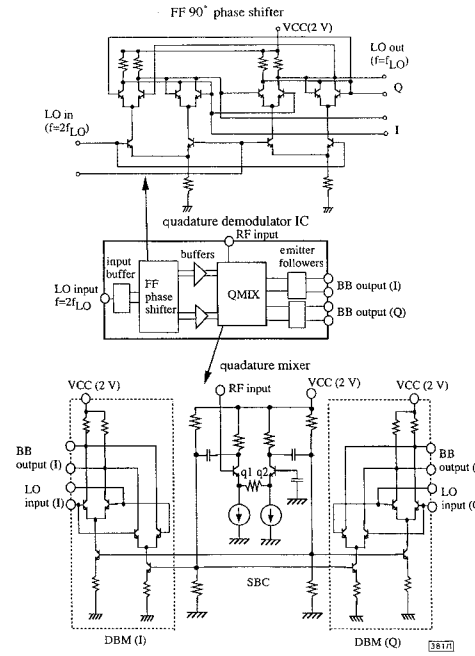

Fig. 1 *Block diagram of quadrature demodulator IC*

Circuit design and layout: Fig. 1 is a block diagram of a QDEM IC, consisting of an input buffer, a FF 90° phase shifter, two buffer amplifiers, a quadrature mixer (QMIX), and two output buffers. A single-ended signal generated by a synthesiser, whose frequency is twice that of a LO signal, is fed to the input buffer. The signal is converted to a differential signal in the input buffer and flows to the phase shifter so that the differential LO signal provides high phase and amplitude accuracy. The phase shifter divides the signal frequency in half, and outputs I and Q differential LO signals to the QMIX, via the buffer amplifiers. The large driving power from these buffers placed before and after the phase shifter is also effective in improving accuracy. Because a two-stacked-transistor configuration is necessary to keep the supply voltage down to 2V, resistors are used as current sources in the phase shifter. A single-balance converter (SBC) and a double-balanced mixer (DBM) core are connected by a capacitor in the QMIX. A single-ended radio-frequency (RF) signal is supplied to the SBC consisting of Q1 and Q2. The RF signal converted to a differential signal drives both the I and Q DBM cores through the coupling capacitors. The differential signal transmission has the advantage of suppressing IM2. Moreover, the coupling capacitors block the IM2 components resulting from the SBC. Conversely, the combination of one SBC and two DBM cores provides a higher demodulation accuracy than the combination of two SBCs and two DBM cores, because of the deferences in the gain and phase shift between the two SBCs. Demodulated baseband (BB) signals are output through the emitter-followers.